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Energy-Efficient CMOS Ring Oscillator for Sustainable 5G Communication System: A Comprehensive Literature Review

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Abstract: The rapid deployment of fifth-generation (5G) wireless communication systems has significantly increased the demand for compact, high-frequency, low-power and energy-efficient radio-frequency integrated circuits. Frequency generation is one of the most critical functions in a 5G transceiver because phase-locked loops (PLLs), frequency synthesizers, clock generators and local oscillators directly influence system power consumption, phase noise, frequency stability and communication performance. Conventional LC-tank voltage-controlled oscillators (LC-VCOs) provide excellent phase-noise performance but suffer from large silicon area, limited frequency tuning flexibility and relatively high implementation complexity. CMOS ring oscillators and ring-based voltage-controlled oscillators (RO-VCOs), in contrast, provide attractive advantages in terms of compact area, wide tuning range, digital compatibility and low power consumption.

Recent IEEE research has demonstrated substantial progress in ring-oscillator-based frequency generation for wireless communication, PLLs, digital frequency synthesizers and high-speed interfaces. However, the intrinsic phase-noise and jitter limitations of ring oscillators remain important challenges for 5G applications. Recent approaches include current-starved delay cells, pseudo-differential architectures, digitally controlled ring oscillators, injection locking, multi-phase generation, adaptive tuning, supply-noise suppression and advanced CMOS/FinFET technologies. This paper systematically reviews these developments and analyzes the trade-offs among power consumption, oscillation frequency, tuning range, phase noise, jitter, area and figure of merit (FoM).

Particular attention is given to the relationship between oscillator energy efficiency and sustainable 5G communication. A comparative analysis of recent IEEE publications is presented, followed by a taxonomy of CMOS ring-oscillator architectures and identification of important research gaps. The review indicates that future energy-efficient 5G/6G ring oscillators should combine adaptive power management, low-voltage operation, digitally assisted calibration, improved phase-noise suppression and technology-aware delay-cell optimization.

Index Terms: CMOS, ring oscillator, ring VCO, voltage-controlled oscillator, low power, energy efficiency, 5G, 6G, PLL, phase noise, jitter, frequency synthesizer, sustainable communication, VLSI.

I. INTRODUCTION

The evolution of wireless communication from fourth-generation (4G) systems toward 5G has resulted in substantial increases in data rate, spectral efficiency, connectivity density and network intelligence. 5G communication systems employ sophisticated transceiver architectures incorporating massive multiple-input multiple-output (MIMO), carrier aggregation, beamforming, millimeter-wave communication and highly integrated RF front ends. These techniques require accurate and energy-efficient frequency-generation circuits.

The frequency synthesizer is one of the most power-sensitive blocks in a wireless transceiver. A typical synthesizer incorporates a phase detector or phase-frequency detector, charge pump, loop filter, voltage-controlled oscillator (VCO), divider and associated digital circuitry. Among these components, the VCO frequently represents a significant contributor to the power and noise characteristics of the PLL.

The conventional LC-VCO provides excellent phase-noise characteristics because of its high quality factor and resonant operation. However, inductors consume considerable silicon area and are difficult to scale efficiently in advanced CMOS processes. Ring oscillators provide an alternative architecture based on cascaded delay cells rather than inductive resonance. Consequently, ring oscillators offer smaller area, potentially lower power, wider tuning range and easier integration with digital CMOS circuitry.

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The basic oscillation frequency of an N-stage ring oscillator is approximately:

$f_{osc} = 1 / (2 N t_d)$

where N is the number of inverter stages and t_d is the propagation delay of an individual stage.
The delay of a CMOS inverter is strongly dependent on transistor current, load capacitance and supply voltage. Thus:

$t_d \propto C_L V_{DD} / I_{drive}$

and consequently:

$f_{osc} \propto I_{drive} / (N C_L V_{DD})$

These relationships demonstrate why transistor sizing, supply voltage, load capacitance and current-control mechanisms are fundamental design parameters in an energy-efficient ring oscillator.
Recent IEEE research has increasingly investigated ring oscillators for PLLs and wireless systems. A 2022 IEEE ISSCC work demonstrated a 5.2-GHz ring-DCO-based fractional-N digital PLL and emphasized that ring oscillators are attractive for area-efficient PLL implementations in advanced wireless systems, including 5G transceivers. More recent research continues to improve ring-based oscillator architectures through low-power delay cells, multiphase generation, injection locking and adaptive calibration.
The central research question is therefore: how can the energy-efficiency and compactness advantages of CMOS ring oscillators be maintained while achieving the phase-noise and jitter performance required by 5G communication systems?

II. FUNDAMENTALS OF CMOS RING OSCILLATORS

A. Principle of Operation

A ring oscillator consists of an odd number of inverting delay stages connected in a closed loop. The output transition of each stage propagates through the ring, and the total propagation delay determines the oscillation period.
$T_{osc} = 2 N t_d$
$f_{osc} = 1 / (2 N t_d)$
The fundamental oscillation condition is obtained when the loop provides sufficient gain and the accumulated phase shift satisfies the oscillation condition.

B. Conventional CMOS Ring Oscillator

The conventional CMOS ring oscillator uses CMOS inverter stages. Its principal advantages are simple topology, small silicon area, wide frequency tuning capability, standard-CMOS compatibility, natural multiphase generation and potentially low power consumption. Its main limitation is relatively poor phase noise compared with LC-based oscillators.

C. Current-Starved Ring Oscillator

The current-starved architecture introduces additional transistors to control the current available to each inverter stage. An approximate relationship is:
$f_{osc} \approx I_{ctrl} / (2 N C_L V_{swing})$
where I_{ctrl} is the controlled bias current. This architecture provides effective voltage-controlled frequency tuning and power management, although additional devices introduce headroom and area penalties.

III. RING OSCILLATORS FOR 5G COMMUNICATION

5G transceivers require frequency-generation circuits capable of operating across a wide range of frequencies, including sub-6-GHz and millimeter-wave bands. Ring oscillators are attractive because their frequency can be tuned over a wide range, multiple phases can be generated naturally, they integrate well with digital PLLs, and their power can be reduced through current scaling and low-voltage operation.
The primary challenge is the power-noise-frequency trade-off. Increasing transistor current generally increases oscillation frequency and may improve timing behavior, but increases power. Reducing current improves energy efficiency but increases delay and may degrade phase noise and frequency stability.

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IV. REVIEW OF RECENT IEEE RESEARCH

A. Ring-DCO-Based Digital PLLs

A 2022 IEEE ISSCC work reported a 5.2-GHz ring-DCO-based fractional-N digital PLL. The design achieved 188-fs rms jitter and a reported jitter FoM of approximately −243 dB. The work is important because it demonstrates that ring-oscillator-based DPLLs can support demanding wireless frequency-synthesis applications while highlighting ring-oscillator jitter as a fundamental limitation.

B. Low-Power Ring Oscillators for Frequency Synthesizers

A 2024 IEEE ICICM publication presented a low-power frequency synthesizer employing an energy-efficient ring oscillator. The architecture generated multiphase outputs and used frequency tripling, illustrating how the oscillator and frequency-generation blocks can be co-designed to reduce system power.

C. High-Frequency Ring/VCO Architectures

A 2024 ICCIT study compared CMOS stage ring VCO, current-starved VCO, NMOS-sink current-starved VCO, diode-connected PMOS-load VCO and parallel-PMOS-load architectures. The reported parallel-PMOS-load design reached 29.48 GHz at 2 V while consuming 1.12 mW, with a tuning range of 9.56–29.62 GHz and reported phase noise of −55.79 dBc/Hz at 1-MHz offset.

D. Ring Oscillator-Based High-Speed Clock Generation

A 2025 IEEE CICC paper presented a 0.3–10.1-GHz hybrid injection-locked eight-phase clock generator in 28-nm CMOS. The design reported 33.8-fs rms jitter and used adaptive mismatch cancellation. Although targeted at high-speed links rather than directly at 5G RF, the techniques are relevant to low-jitter multiphase timing generation.

E. Ring Oscillators in Low-Power Wireless Systems

An IEEE Journal of Solid-State Circuits work on an ultra-low-power Bluetooth Low Energy transmitter used an f_RF/4 ring oscillator inside an all-digital PLL and a 4-frequency edge combiner. Fabricated in 40-nm CMOS, the system demonstrated a 486-µW low-power mode. The work illustrates the value of co-designing oscillator, PLL and frequency multiplication circuitry.

V. COMPARATIVE LITERATURE ANALYSIS

Ref.	Year	Architecture	Technology	Frequency	Power	Main Contribution
[1]	2022	Ring-DCO Fractional-N PLL	CMOS	5.2 GHz	System dependent	Low-jitter ring-DCO PLL
[2]	2024/25	Parallel-PMOS-load VCO	CMOS	29.48 GHz	1.12 mW	Wide tuning/high frequency
[3]	2024	Energy-efficient ring-VCO synthesizer	CMOS	RF range	Low	Multiphase generation/frequency tripling
[4]	2024	Current-starved RO	18-nm FinFET	High speed	Low power	Advanced-node implementation
[5]	2025	Injection-locked RO clock generator	28-nm CMOS	0.3–10.1 GHz	—	33.8-fs rms jitter
[6]	2019	Ring-RO ADPLL transmitter	40-nm CMOS	BLE RF	486 µW	Ultra-low-power wireless transmitter

VI. TAXONOMY OF ENERGY-EFFICIENT RING OSCILLATORS

1. Conventional CMOS Ring Oscillators

Simple inverter-stage topology offering minimum area and low complexity, but relatively poor phase-noise performance.

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2. Current-Starved Ring Oscillators
Use current-control transistors to regulate delay-cell current and provide frequency and power control.

3. Differential/Pseudo-Differential Ring Oscillators
Improve common-mode rejection, signal integrity and phase accuracy, at the expense of circuit complexity.

4. Digitally Controlled Ring Oscillators
Use digitally controlled current or capacitance banks for calibration, tuning and digital-PLL compatibility.

5. Injection-Locked Ring Oscillators
Synchronize the oscillator to an injected reference to improve timing and enable multiphase generation.

6. Advanced-Node Ring Oscillators
Use FinFET or advanced CMOS technologies for higher speed, lower voltage and reduced parasitic capacitance.

VII. ENERGY-EFFICIENCY CONSIDERATIONS

Energy efficiency should be evaluated using more than static power. A useful metric is energy per oscillation cycle:

$E_{cycle} = P / f_{osc}$

Dynamic power can be approximated as $P_{dynamic} \approx \alpha C_L V_{DD}^2 f$. This relationship shows that reducing supply voltage and effective switched capacitance can provide significant energy savings. A sustainable oscillator should therefore target low power, high frequency, low phase noise, wide tuning range, small area, low supply voltage, PVT robustness and low energy per cycle.

VIII. MAJOR RESEARCH CHALLENGES

A. Phase Noise
Ring oscillators generally exhibit higher phase noise than high-Q LC-VCOs because noise from individual delay cells perturbs the oscillation phase.

B. Power–Frequency Trade-off
Higher current improves drive strength and frequency but increases power consumption; aggressive current reduction can degrade phase noise and startup.

C. Supply Sensitivity
Supply fluctuations directly affect propagation delay and therefore cause frequency variation and modulation.

D. Process, Voltage and Temperature Variation
Device variations can produce significant frequency deviation from the nominal design point.

E. Tuning Linearity
Nonlinear frequency-control characteristics complicate PLL loop design and calibration.

F. Phase Mismatch
Multiphase ring oscillators are sensitive to delay mismatch; adaptive calibration and injection-locking techniques can reduce phase errors.

IX. IDENTIFIED RESEARCH GAPS

Research Gap 1: Power and Phase Noise Are Often Optimized Separately
A unified architecture simultaneously optimizing power, frequency, phase noise, jitter and FoM remains desirable.

Research Gap 2: Limited Sustainable-Communication Perspective
Most oscillator studies report circuit-level power but do not quantify the oscillator's contribution to total 5G transceiver energy.

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Research Gap 3: Insufficient Adaptive Power Management
Many designs use fixed bias current; dynamic current scaling could reduce energy when maximum performance is unnecessary.

Research Gap 4: PVT Robustness Versus Energy Efficiency
Additional calibration improves robustness but increases area and power, motivating low-overhead compensation.

Research Gap 5: Sub-Threshold/Near-Threshold Operation
Very-low-voltage operation offers large energy savings but creates startup, frequency-stability and phase-noise challenges.

Research Gap 6: Lack of Co-Optimization With 5G PLL Architecture
The ring VCO, divider, PLL, multiplier and clock-distribution network should be optimized as a complete frequency-generation subsystem.

X. PROPOSED RESEARCH DIRECTION

Based on the reviewed literature, an energy-efficient CMOS ring oscillator for sustainable 5G communication can combine a low-voltage delay cell, current-starved/adaptive bias control, a differential or pseudo-differential ring, digitally controlled frequency banks, PVT calibration and multiphase outputs.

Recommended architecture flow:
Low-Voltage CMOS Delay Cell → Adaptive Bias Control → Multi-Stage Ring → Digital Frequency Bank → PVT Calibration → Multi-Phase Output → 5G PLL/Frequency Synthesizer

- Reduced supply voltage.
- Minimum practical transistor count.
- Adaptive current control.
- Reduced parasitic capacitance.
- Differential or pseudo-differential operation.
- Digital frequency calibration.
- Multiphase generation.
- PVT compensation.
- Low-energy startup.
- Compatibility with PLL-based 5G frequency synthesis.

XI. RECOMMENDED PERFORMANCE TARGETS

Parameter	Recommended Research Target
CMOS technology	28/45/65 nm
Supply voltage	0.5–1.0 V
Frequency	2–10 GHz
Tuning range	>50%
Power	<1 mW desirable
Phase noise @ 1 MHz	< −90 dBc/Hz desirable
PVT compensation	Yes
Multiphase output	4/8 phases
Energy per cycle	Minimize
Application	5G PLL/RF synthesizer

XII. FUTURE RESEARCH DIRECTIONS

1. AI-Assisted Oscillator Optimization
Machine-learning-based transistor sizing can optimize dimensions, bias currents and delay-cell topology.

2. Adaptive Energy Management
Dynamic bias scaling can reduce power according to instantaneous frequency requirements.

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3. Digitally Assisted Calibration
Background calibration can compensate PVT variations with limited overhead.

4. Injection-Locked Energy-Efficient Ring Oscillators
Injection locking can be combined with current-starved architectures to improve jitter while maintaining low power.

5. FinFET/GAA Implementation
Advanced transistor architectures can be evaluated for improved frequency and energy per cycle.

6. 6G and Sub-THz Applications
Ring-based frequency generation can be extended toward future mm-wave and sub-THz systems.

7. Sustainable RFIC Design
Future evaluation should include energy per transmitted bit, energy per synthesized frequency, area efficiency and thermal contribution.

XIII. CONCLUSION

This literature review examined recent developments in energy-efficient CMOS ring oscillators and their application to wireless communication systems. The literature demonstrates that ring oscillators provide important advantages over LC-based oscillators in terms of silicon area, tuning range, digital compatibility and potential energy efficiency. Recent IEEE research has demonstrated multi-GHz ring-DCOs, current-starved ring oscillators, injection-locked ring architectures and high-frequency ring-VCOs suitable for advanced communication systems.

Nevertheless, phase noise, jitter, PVT sensitivity, supply sensitivity and the power-frequency trade-off continue to limit widespread replacement of LC-VCOs in demanding RF applications. The principal research opportunity is therefore the development of a low-voltage, adaptive, PVT-tolerant and digitally assisted CMOS ring oscillator that achieves a favorable balance among power, frequency, phase noise, tuning range and area.

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