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Energy-Efficient 32-Bit RISC-V Processors Design in 45nm

Bhoomika J[1], Manjunatha V[2], Chandan B[3], Dr. Chaitra A S[4]

Dept. of Electronics Engineering – VLSI Design and Technology, SKIT, Bengaluru, India

Associate Professor, Dept. of Electronics Engineering – VLSI Design and Technology, SKIT, Bengaluru, India

Abstract: Energy efficiency represents a foundational design metric for modern embedded microcontrollers, edge artificial intelligence accelerators, biomedical wearables, and autonomous Internet-of-Things (IoT) sensor nodes. In these constrained deployments, stringent thermal limits, sub-milliwatt power budgets, and silicon area restrictions dictate processor microarchitecture. The open-standard RISC-V Instruction Set Architecture (ISA), particularly the unprivileged 32-bit integer base profile (RV32I) and its modular extensions (RV32IMC), has emerged as the premier open ecosystem for researching energy-optimal compute engines without the impediments of proprietary licensing. While modern industrial trends emphasize sub-10-nm FinFET nodes or FPGA-based prototyping, a standard 45-nm bulk CMOS ASIC design flow remains an indispensable, highly reproducible academic and industrial benchmark for characterizing fundamental switching dynamics, standard-cell leakage, dynamic interconnect capacitance, and clock-network parasitics. This paper provides an extensive, comprehensive literature review of contemporary IEEE advancements spanning 2020 through 2026. Furthermore, it details an end-to-end, multi-stage reference implementation methodology—spanning synthesis-friendly SystemVerilog/Verilog RTL modeling, architectural hazard mitigation, datapath operand isolation, multi-level integrated clock gating (ICG), logic synthesis, static timing analysis (STA), clock tree synthesis (CTS), and post-layout parasitic extraction (SPEF). Systematic comparative metrics across critical path delay, total equivalent gate count, leakage power, switching energy per instruction, and Energy-Delay Product (EDP) are formulated to establish a definitive reference framework for academic VLSI engineering.

Index Terms: RISC-V, RV32I, RV32IMC, Low-Power VLSI, Energy Efficiency, 45-nm CMOS, Standard-Cell ASIC, Clock Tree Synthesis (CTS), Operand Isolation, Clock Gating, Energy-Delay Product (EDP), Static Timing Analysis.

I. INTRODUCTION AND MOTIVATION

The exponential growth of edge computing paradigms, remote environmental telemetry, industrial cyber-physical systems, and ultra-low-power biomedical sensor nodes has catalyzed a fundamental paradigm shift in digital processor microarchitecture. Historically, microarchitecture research prioritized raw compute throughput and peak clock frequency. However, modern embedded systems operate under strict thermal dissipation limits and finite electrochemical battery capacities, establishing energy efficiency—conventionally quantified as energy consumed per useful operation (pJ/cycle or pJ/instruction)—as the primary figure of merit.

In standard complementary metal-oxide-semiconductor (CMOS) digital integrated circuits, total power consumption comprises dynamic switching power, short-circuit current dissipation, and static sub-threshold/gate leakage. Dynamic power is dominated by capacitive charging and discharging of sequential and combinational nodes across clock cycles, whereas static leakage represents parasitic conduction paths in inactive transistors. Mitigating these dissipation sources requires a holistic, cross-layer co-design approach spanning the instruction set architecture, microarchitectural pipeline depth, execution-unit switching activity, clock network synthesis, and standard-cell library mapping.

The RISC-V ISA, introduced as an open standard, provides an ideal platform for energy-aware microarchitectures. Unlike traditional closed commercial ISAs, RISC-V offers a clean, unencumbered base integer specification (RV32I) comprised of only 47 fundamental instructions. This lean baseline can be systematically extended with standardized modular extensions—such as integer multiplication/division (M), atomic operations (A), single-precision floating-point (F), and compressed 16-bit instructions (C)—or augmented with proprietary application-specific functional accelerators.

While cutting-edge industrial systems-on-chip (SoCs) utilize 7-nm, 5-nm, or 3-nm Gate-All-Around (GAA) FinFET nodes, the 45-nm bulk CMOS technology node maintains paramount significance in academic research and commercial mixed-signal/analog-adjacent microcontrollers. The 45-nm node represents a fully matured planar CMOS technology with reliable, well-characterized standard-cell design kits, predictable wire interconnect parasitic scaling, and established electronic design automation (EDA) flows. Consequently, conducting a systematic RV32 processor implementation in

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45-nm CMOS provides an authentic, standard, and highly reproducible baseline for isolating microarchitectural optimizations from process variations.

II. REVIEW METHODOLOGY AND TAXONOMICAL CLASSIFICATION

To establish a thorough foundation, this review systematically aggregates and synthesizes recent high-impact IEEE Xplore publications (2020–2026). The survey focuses specifically on hardware-level architectural and circuit innovations targeting low-power RV32 cores. The collected literature is organized into six functional taxonomical categories: (1) Energy-Efficient RV32 Microcontrollers, (2) Ultra-Low-Power Edge Compute Engines, (3) Microarchitectural Pipeline Trade-off Studies, (4) Low-Switching Datapath & Arithmetic Design, (5) Advanced Asynchronous & Resilient Topologies, and (6) Automated Workload-Specific Customization.

III. THE RISC-V ISA ARCHITECTURE AS A LOW-POWER ENGINE

The RISC-V base integer specification is inherently engineered for hardware simplicity. The base RV32I architecture enforces fixed 32-bit instruction words with consistent source (rs1, rs2) and destination (rd) register field locations. This regularity minimizes combinational decoding logic depth, eliminating unnecessary switching and reducing the critical path between the instruction register and the register file decode logic.

A. Base RV32I vs. Extended RV32IMC Architectures

Selecting the optimal set of ISA extensions represents the earliest and most critical design decision in energy-constrained VLSI engineering:

- Base Integer (RV32I): Contains 32 general-purpose registers (x0–x31) with x0 hardwired to zero. It relies on software emulation routines for multiplication and division. While this minimizes silicon area and static leakage, compute-intensive workloads suffer from extended cycle latency, increasing total energy per task.
- Standard Compressed Extension (RVC / RV32C): Introduces 16-bit compressed instruction encodings that map directly to common 32-bit instructions. Compressed instructions reduce static code footprint by 25%–35%. Crucially, this dramatically decreases the frequency of external instruction memory fetches, reducing high-capacitance bus switching and I/O buffer power dissipation, which typically dominates processor datapath energy.
- Standard Multiplication/Division (RVM / RV32M): Adds hardware integer multiplication and division. While dedicated hardware arrays increase total cell area and potential leakage, they execute multiplication in 1 to 3 clock cycles compared to 30–50 cycles for software loops. For arithmetic-heavy workloads, this yields an immense reduction in total energy consumption.

IV. LOW-POWER DATAPATH & ALU OPTIMIZATION

The ALU is the primary switching hub within the integer core. Optimization techniques include:

- Operand Isolation: Utilizing transparent latches or logic gating at the inputs of high-capacitance execution units (e.g., barrel shifters, multipliers) prevents spurious toggling when unselected.
- Adder Selection: Ripple Carry Adders minimize area and leakage for low-frequency (<50 MHz) applications, while Carry-Lookahead or Carry-Select adders provide fast timing closure at moderate power.
- Booth Multipliers: Radix-4 Booth arrays with Wallace tree reduction halve partial products, drastically reducing switching activity.

V. CLOCK GATING AND SWITCHING POWER REDUCTION

Dynamic switching power is governed by $P_{dyn} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f_{clk}$. In synchronous digital processors, clock distribution accounts for 35% to 45% of total dynamic power. Multi-level Integrated Clock Gating (ICG) is applied hierarchically: (1) Module-Level Architectural Gating to disable entire idle accelerators, and (2) Register-Level Gating to halt pipeline registers during stalls.

VI. COMPREHENSIVE LITERATURE SYNTHESIS

Table I provides a detailed structured comparison of representative IEEE studies, comparing architectural focus, technological novelty, and relevance to 45-nm standard-cell flows.

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Ref.	Year	Architecture	Primary Research Contribution	Key Relevance to 45-nm ASIC Flow
[1]	2020	RV32IMAC	Periodic sensing MCU optimized for burst execution.	Power gating & duty-cycle baseline for sensor nodes.
[2]	2023	Ultra-Low RV32	Sub-milliwatt core for real-time anomaly detection.	Validates energy-per-task metrics over raw frequency.
[3]	2023	RV32I Cores	Multi-pipeline comparative study (1, 2, 3, 5 stages).	Empirical criteria for pipeline selection and EDP.
[4]	2024	RV32 ALU	ALU operand isolation and low-switching adders.	Directly transferable to 45-nm combinational datapath.
[5]	2024	RV32 Compute	End-to-end YOLOv8 edge vision implementation.	Demonstrates datapath customization for compute kernels.
[6]	2026	Asynchronous	Clockless microarchitecture in Intel 3 Process.	Shows theoretical limits of clock network removal.
[7]	2026	Resilient RV32	Temporal lockstep fault mitigation for low-cost reliability.	Energy vs. fault tolerance trade-offs in mission-critical chips.
[8]	2026	RV32 Steel	Compact 32-bit MCU core verification & implementation.	Reference for clean, modular synthesizable RTL.
[9]	2022	Ecosystem	Survey of RISC-V software toolchain & compiler support.	Establishes software benchmarking compilation flow.
[10]	2026	ARVIS	Automated profiling framework for core stripping.	Validates removing unused functional units at synthesis.

VII. DETAILED MICROARCHITECTURAL TRADE-OFF ANALYSIS

The microarchitectural pipeline organization represents the most consequential structural choice affecting the Energy-Delay Product (EDP). Processor pipeline stages dictate register overhead, hazard resolution multiplexing, and combinational path lengths.

- Single-Cycle Architectures: In a single-cycle implementation, an entire instruction completes within one clock period. While control logic is minimal, the critical path equals the sum of delays across all stages, severely restricting operating frequency and degrading EDP.
- 2-Stage & 3-Stage Pipelines: Partitioning the datapath into shallow pipelines yields an optimal balance. A 2-stage pipeline (Fetch | Execute) isolates fetch latency, while a 3-stage pipeline (Fetch | Decode/Execute | Memory/WB) provides high throughput with minimal sequential register overhead and low clock-tree capacitive load.
- Deep Pipelines (5-Stage+): Deep pipelines maximize peak frequency but suffer from branch penalty bubbles and a 200%+ increase in sequential clock power, making them suboptimal for sub-milliwatt edge nodes.

VIII. CLOCK GATING AND SWITCHING POWER REDUCTION

Dynamic switching power is governed by $P_{dyn} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f_{clk}$. In synchronous digital processors, clock distribution accounts for 35% to 45% of total dynamic power. Multi-level Integrated Clock Gating (ICG) is applied hierarchically: (1) Module-Level Architectural Gating to disable entire idle accelerators, and (2) Register-Level Gating to halt pipeline registers during stalls.

IX. STANDARD-CELL ASIC IMPLEMENTATION METHODOLOGY IN 45-nm CMOS

A standardized, reproducible 5-phase ASIC implementation flow is established:

1. Parameterized RTL Modeling: Synthesizable SystemVerilog with configurable pipeline depth and extension macros.
2. Functional & Compliance Verification: Executing official RISC-V compliance suites and generating switching activity files (VCD/SAIF) under CoreMark and Dhrystone workloads.
3. Logic Synthesis & Technology Mapping: Targeting a generic 45-nm bulk CMOS standard-cell library across Typical (1.1V, 25°C) and Worst-Case (0.95V, 125°C) PVT corners with Multi-Vt cell optimization.
4. Physical Implementation & CTS: Floorplanning, power-grid IR-drop mitigation, standard-cell placement, symmetrical H-tree CTS, detailed routing, and SPEF parasitic extraction.
5. Sign-Off Timing & Power Analysis: Multi-corner Static Timing Analysis (STA) and gate-level power simulation with back-annotated parasitics.

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X. RESEARCH Gaps, FUTURE DIRECTIONS, AND CONCLUSION

While contemporary research explores exotic nodes, open baseline data for 45-nm planar CMOS remains crucial. Future directions involve Dynamic Voltage and Frequency Scaling (DVFS), multi-power sleep domains, and approximate computing datapaths. In conclusion, combining modular RV32 microarchitecture with shallow pipelining, operand isolation, and hierarchical clock gating achieves an optimal energy-delay-area envelope in 45-nm CMOS technology.

REFERENCES

[1] R. Galluccio, A. Rizzo, G. Patane, S. P. Sabina, and G. De Vita, "An Energy-Efficient RISC-V RV32IMAC Microcontroller for Periodical-Driven Sensing Applications," in Proc. IEEE ISCAS, 2020.
[2] "Developing an Ultra-low Power RISC-V Processor for Anomaly Detection," in Proc. IEEE ISVLSI, 2023.
[3] "Evaluation of Different Microarchitectures for Energy-Efficient RISC-V Cores," in Proc. IEEE ICECS, 2023.
[4] "Design of Low Power ALU for RISC-V ISA," in Proc. IEEE ICEET, 2024.
[5] "A Power-efficient End-to-end Implementation of YOLOv8 Based on RISC-V," in Proc. IEEE AICAS, 2024.
[6] "Mount Sisyphus: Energy-Efficient Asynchronous RISC-V Microcontroller in Intel 3 Process," in Proc. IEEE ISSCC, 2026.
[7] R. Tedeschi et al., "Temporal Lockstep: Low-Cost Resilient Design for RISC-V," IEEE Trans. VLSI Syst., 2026.
[8] "Implementation of a Compact and Resource-Efficient 32-bit Microcontroller Using the RISC-V Steel 32-bit Processor," IEEE Access, 2026.
[9] B. W. Mezger et al., "A Survey of the RISC-V Architecture Software Support," IEEE Access, 2022.
[10] P. Fidalgo et al., "ARVIS: Automated RISC-V Workload-Specific Specialization," IEEE Micro, 2026.

