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LITERATURE REVIEW
A Sustainable Approach to Low-Power Real-Time PLL Design Using Current-Starved VCO in 45-nm CMOS Technology

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Abstract: Phase-Locked Loops (PLLs) are essential mixed-signal circuits for clock generation, frequency synthesis, synchronization, timing recovery, wireless communication, and energy-constrained embedded systems. As semiconductor technology scales, PLL designers must simultaneously address power consumption, phase noise, jitter, lock time, tuning range, supply sensitivity, process-voltage-temperature (PVT) variations, and implementation area. The voltage-controlled oscillator (VCO) is particularly important because its delay, current, gain, and noise directly influence the closed-loop behavior of the PLL. Current-starved voltage-controlled oscillators (CSVCOs) are attractive for low-power operation because the bias current of the delay stages can be controlled through the tuning voltage. This literature review examines 15 representative publications covering low-power PLLs, current-starved VCOs, 45-nm CMOS implementations, PVT-tolerant oscillator techniques, charge-pump design, ring-VCO PLLs, and recent supply-noise-insensitive PLL research. Particular attention is given to IEEE publications and recent work from 2024–2025. The review identifies a gap in the joint optimization of a complete 45-nm CSVCO-based PLL for low power, real-time locking, wide tuning, low phase noise, and robustness. The findings provide the technical basis for the proposed sustainable PLL design using Cadence Virtuoso.

Index Terms: Phase-Locked Loop (PLL), Current-Starved VCO (CSVCO), ring oscillator, 45-nm CMOS, low power, real-time locking, phase noise, jitter, charge pump, PVT variation, supply-noise immunity.

I. INTRODUCTION

A PLL is a feedback-based frequency and phase synchronization system normally consisting of a phase-frequency detector (PFD), charge pump (CP), loop filter (LF), VCO, and frequency divider. In a conventional charge-pump PLL, the PFD detects phase/frequency error between the reference and divided feedback signals. The charge pump converts this error into current, the loop filter generates the VCO control voltage, and the VCO produces the controlled oscillation frequency. The divider closes the feedback path. The design of these blocks is strongly coupled: increasing loop bandwidth can improve acquisition speed but can also increase reference-noise transfer; increasing VCO current can improve speed and reduce some noise mechanisms but raises power; and aggressive transistor scaling can increase leakage and PVT sensitivity.

The literature shows that low-power PLL design has progressed from isolated VCO optimization toward complete architectures with improved charge pumps, PFDs, loop filters, frequency dividers, and noise-management techniques. A recent IEEE Access review surveys PLL architectures and compares power, phase noise, frequency, area, figure of merit, and lock time, emphasizing the need for multi-parameter evaluation. [15]

For a sustainable low-power design, power should not be considered independently. A PLL that consumes very little power but has poor phase noise, excessive lock time, inadequate tuning range, or severe supply sensitivity may not be suitable for a real application. Therefore, this review treats power efficiency, real-time response, spectral purity, tuning capability, and robustness as interconnected design objectives.

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II. FUNDAMENTALS RELEVANT TO THE PROPOSED WORK

A. Current-Starved VCO

A current-starved ring VCO is formed by placing current-limiting transistors around the inverter stages of a ring oscillator. The control voltage regulates the available current, which changes the propagation delay of each stage and hence the oscillation frequency. In an idealized ring oscillator, the oscillation frequency can be represented as fosc ≈ 1/(2Ntd), where N is the number of delay stages and td is the average stage delay. Current-starving increases controllability of td and provides a convenient way to trade frequency against power. The topology is therefore attractive for compact CMOS PLLs without on-chip inductors.

B. PLL Power Components

PLL power is distributed among the PFD/CP, loop filter, VCO, divider, buffers, and leakage paths. Dynamic power is approximately proportional to switching activity, capacitance, frequency, and supply-voltage squared. Consequently, supply reduction, transistor sizing, reduced switching capacitance, and low-current biasing are common approaches. However, reducing supply voltage or current too aggressively can reduce voltage swing, slow the loop, increase sensitivity to mismatch, and degrade phase noise or lock time.

C. Real-Time Locking

Lock time is the time required for the PLL output to enter and remain within a specified frequency or phase-error tolerance after a change in reference, divider ratio, or initial condition. It depends on loop bandwidth, damping, VCO gain, charge-pump current, loop-filter parameters, divider ratio, and the magnitude of the frequency step. For the proposed work, transient analysis should report both acquisition and settling behavior using an explicitly stated lock criterion.

D. Sustainable Design Perspective

The sustainability objective is interpreted as achieving the required frequency-generation function with minimum energy and hardware overhead while maintaining reliable operation. In this context, a low-power CSVCO, efficient charge pump, compact divider, reduced supply voltage, and PVT-aware design can reduce energy demand and silicon resources. The final design should therefore report energy per lock/acquisition event where practical, in addition to steady-state power.

III. DETAILED LITERATURE REVIEW

1) Saw and Nath – Low-Power Low-Noise Current-Starved CMOS VCO

Saw and Nath proposed an ultra-low-power, low-phase-noise CSVCO specifically targeting PLL applications. The design was implemented in Cadence Virtuoso using a 45-nm gpdk CMOS technology and a 1-V supply. Their simulation reported approximately −104 dBc/Hz phase noise at 1-MHz offset. The study is highly relevant to the present project because it directly establishes the feasibility of a 45-nm current-starved VCO for low-power PLL applications. However, the work concentrates on the oscillator rather than presenting a complete closed-loop PLL optimization. The results therefore motivate extending CSVCO optimization into a full PLL architecture. [1]

2) Nagpara – 45-nm CSVCO for Digital PLL

Nagpara analyzed tuning range, phase noise, and jitter of a current-starved VCO for a digital PLL using a 45-nm CMOS process. The reported tuning range was approximately 3.24 MHz to 178.42 MHz, with a center-frequency power of about 1.30 µW and reported jitter of 244.5 ps at 100 MHz. This work demonstrates the very low power possible with current-starved operation at moderate frequencies. It also highlights the important trade-off among tuning range, phase noise, and jitter. [2]

3) Optimization of 45-nm CSVCO for High-Frequency PLL

Md. Sallah et al. optimized a three-stage single-ended current-starved ring VCO for high-frequency PLL applications using 45-nm CMOS and Cadence Virtuoso. Different transistor dimensions were investigated. The selected configuration achieved a tuning range of approximately 9.94–10.25 GHz, 120.7 µW power at 0.6-V control voltage, and approximately −81.7 dBc/Hz phase noise at 1-MHz offset. The study is one of the strongest recent direct references for a 45-nm CSVCO. Its principal limitation for the present research is that the evaluation is VCO-centered rather than a complete low-power real-time PLL. [3]

4) Sivasakthi and Radhika – PVT-Tolerant Hybrid CSVCO

Sivasakthi and Radhika proposed two current-starved ring-VCO approaches, including a current-starved pull-up sleepy-ring VCO and a hybrid current-starved ring VCO with a bulk-driven keeper technique. The designs were evaluated in

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45-nm gpdk using Cadence Virtuoso, including process corners, parametric analysis, and Monte-Carlo simulations. The work is important because it moves beyond nominal performance and addresses robustness against PVT variation. For a real-time PLL, this is significant because frequency drift in the VCO directly changes the loop operating point. [4]

5) Sharanya et al. – 45-nm Charge-Pump PLL with CSVCO

Sharanya et al. developed a complete charge-pump PLL in 45-nm CMOS for sub-6-GHz operation. The design uses a combinational PFD with transmission gates and a three-stage current-starved VCO. Reported results include approximately 8.05 mW power at 0.75 V, a 2.5-GHz VCO center frequency, −127 dBc/Hz phase noise at 1-MHz offset, and about 13.5-ns lock time. This paper is particularly valuable because it connects the CSVCO to a complete PLL and provides a strong benchmark for lock time and phase noise. Its relatively high power compared with ultra-low-power VCO studies leaves an opportunity for further power reduction. [5]

6) Srivastava and Chauhan – Power-Efficient PFD and CSVCO

Srivastava and Chauhan investigated a power-efficient PFD, charge pump, and current-starved VCO for PLL applications in 45-nm CMOS. The proposed PFD reduces transistor count compared with a conventional implementation and uses pass-transistor logic to reduce reset-related complexity. This approach is relevant to sustainable PLL design because the PFD and charge pump also contribute to power and delay. The paper supports the idea that system-level power reduction requires optimization of more than the VCO alone. [6]

7) Hemavathi and Sindhu – CSVCO Implementation in 45-nm CMOS

Hemavathi and Sindhu presented an implementation of a current-starved VCO in 45-nm CMOS and examined frequency and power behavior. The work reinforces the basic design principle that current control in the inverter stages can regulate oscillation frequency while maintaining a compact ring architecture. Although the study is not a complete PLL, it provides implementation-level guidance for a 45-nm CSVCO schematic and simulation flow. [7]

8) Yadav et al. – Digital PLL with Current-Starved Ring VCO

Yadav and co-authors investigated an optimal digital PLL using a current-starved ring VCO. The study emphasizes the suitability of the current-starved topology for low-power and high-speed operation. It demonstrates the broader applicability of CSVCOs beyond analog charge-pump PLLs and supports their use in digitally assisted frequency-synthesis systems. [8]

9) Yun, Kim, and Kwon – Low-Spur CMOS PLL

Yun, Kim, and Kwon investigated low-spur CMOS PLLs using LC-VCO and ring-VCO approaches. The ring-VCO PLL operated approximately from 1.2 to 2.04 GHz and reported about −95 dBc/Hz phase noise at 1-MHz offset. The work demonstrates the relevance of differential compensation and feedback techniques to spur suppression. For the proposed CSVCO PLL, spur and reference-feedthrough behavior should be considered alongside power and lock time. [9]

10) Design of Charge Pump for Low-Power Wide-Range PLL in 65-nm CMOS

An IEEE conference study on charge-pump design for a low-power, wide-range PLL in 65-nm CMOS focuses on the charge pump as a major contributor to PLL performance. The work is relevant because charge-pump mismatch, current accuracy, output compliance, and switching behavior influence static phase error, reference spurs, loop stability, and power. Although the process differs from the proposed 45-nm implementation, its design principles can be transferred to a scaled-node PLL. [10]

11) Low-Power Wide-Frequency-Range PLL

A 2024 study reported a low-power, low-phase-noise, wide-frequency-range PLL for WLAN/Wi-Fi transceivers using a 65-nm CMOS differential-inductor VCO, an improved PFD, and a programmable low-mismatch charge pump. The reported tuning range was approximately 4.6–6 GHz, power was about 7.14 mW, and lock time was around 9 µs. The work shows how improving the PFD and charge pump can stabilize PLL behavior across reference-frequency conditions. It also demonstrates that a complete PLL may achieve low phase noise at the cost of more power than a simple CSVCO. [11]

12) Low-Power 2.1-GHz PLL in 45-nm CMOS

Tafhim et al. reported a low-power 2.1-GHz charge-pump PLL in 45-nm CMOS in the 2025 IEEE ICCIT conference. The architecture includes a PFD, charge pump, loop filter, VCO, and integer-N divider. A current-steering charge pump was used to improve sourcing/sinking symmetry and lock stability. Post-layout simulations reported approximately 11.1 mW dynamic power. This is a recent and directly relevant 45-nm complete-PLL benchmark. It demonstrates that post-

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layout power can be considerably higher than the power of an isolated VCO, reinforcing the need for system-level optimization. [12]

13) 2025 IEEE APCCAS – Supply-Noise-Insensitive Low-Power PLL

Tran-Dinh et al. presented a 2025 IEEE APCCAS paper on a low-power PLL with a supply-noise-insensitive VCO in 65-nm CMOS. The paper is the most recent directly relevant IEEE publication identified in the present search. Its key contribution is the combination of low-power PLL operation with improved VCO immunity to supply disturbances. Although it uses 65-nm CMOS rather than 45-nm CMOS and does not focus specifically on a current-starved VCO, it reflects the current research direction toward robust low-power PLLs. [13]

14) Low-Power Differential Ring VCO for PLL Clocking

A 2025 IEEE conference study reported a four-stage differential ring VCO in 65-nm CMOS for PLL and clocking applications. The design targeted 2.5–4.5 GHz operation and reported approximately 4.5 mW core power with phase noise around −90.3 dBc/Hz at 1-MHz offset. Differential operation improves common-mode noise rejection compared with simple single-ended ring structures. This work provides a useful alternative topology for comparison against a 45-nm single-ended CSVCO. [14]

15) Comprehensive IEEE Review of PLL Architectures

Dutta et al. published an IEEE Access review of PLL architectures, comparing different PLL categories according to power consumption, phase noise, frequency, area, figure of merit, and lock time. The review provides a broad framework for judging PLL performance and supports the use of multi-dimensional performance metrics rather than selecting a design solely on power. This is particularly important for the present sustainable PLL proposal because low power must be achieved without unacceptable degradation of timing and spectral performance. [15]

IV. COMPARATIVE ANALYSIS

Ref.	Year	Node	Architecture / Focus	Key reported result	Relevance
[1]	2015	45 nm	Low-power CSVCO	−104 dBc/Hz @ 1 MHz	Very high
[2]	2015	45 nm	CSVCO for DPLL	1.30 µW; 3.24–178.42 MHz	Very high
[3]	2024	45 nm	Optimized CSVCO	120.7 µW; 9.94–10.25 GHz	Very high
[4]	2024	45 nm	PVT-tolerant CSVCO	PVT + Monte-Carlo evaluation	Very high
[5]	2024	45 nm	Complete CPPLL + CSVCO	8.05 mW; 13.5 ns lock	Very high
[6]	2022	45 nm	PFD + CP + CSVCO	Power-efficient PLL blocks	High
[7]	2024	45 nm	CSVCO implementation	Power/frequency study	High
[8]	2021	CMOS	DPLL + ring CSVCO	Low-power/high-speed focus	Medium
[9]	2012	45/65 nm	Low-spur PLL	Ring PLL 1.2–2.04 GHz	Medium
[10]	2023	65 nm	Low-power CP	Wide-range PLL CP	Medium
[11]	2024	65 nm	Wide-range CPPLL	4.6–6 GHz; 7.14 mW	Medium
[12]	2025	45 nm	2.1-GHz CPPLL	11.1 mW post-layout	Very high
[13]	2025	65 nm	Supply-noise-insensitive PLL	Low-power + noise robustness	Very high
[14]	2025	65 nm	Differential ring VCO	2.5–4.5 GHz; 4.5 mW	High
[15]	2024	Multiple	IEEE PLL review	Multi-metric survey	High

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V. RESEARCH TRENDS IDENTIFIED

1) Shift from isolated VCO optimization to complete PLL optimization: Recent work shows that PFD, charge pump, loop filter, divider, and VCO must be co-designed because the total PLL power and lock behavior are system-level properties.
2) Increasing importance of robustness: PVT analysis, Monte-Carlo simulation, and supply-noise immunity are becoming important because advanced CMOS processes are more sensitive to variation and reduced voltage headroom.
3) Current-starved VCO remains attractive: CSVCOs offer a compact inductor-less implementation and direct current control, making them suitable for low-power clocking and frequency synthesis.
4) Power versus spectral quality: Reducing VCO current can lower power but may worsen phase noise, waveform swing, frequency range, or startup reliability. Therefore, power must be optimized together with phase noise and jitter.
5) Faster real-time locking: Recent PLL work increasingly reports nanosecond-to-microsecond lock behavior. The exact lock criterion must be specified before comparing values across papers.
6) Technology scaling: 45-nm CMOS provides a useful compromise between speed, integration density, and supply voltage. The literature shows that process scaling alone does not guarantee low total PLL power because leakage, interconnect capacitance, and divider switching can dominate.

VI. RESEARCH GAP

Although the literature contains several low-power CSVCO designs and several complete PLL designs, comparatively fewer studies combine all of the following objectives in one 45-nm CMOS implementation: ultra-low power, real-time/nanosecond-scale locking, adequate tuning range, low phase noise and jitter, supply-noise tolerance, and PVT robustness. The recent 2025 IEEE APCCAS study addresses low-power PLL operation and supply-noise-insensitive VCO behavior, but it uses 65-nm CMOS and a different VCO strategy. The 2025 IEEE ICCIT study provides a direct 45-nm PLL benchmark but reports approximately 11.1 mW post-layout dynamic power. Meanwhile, the 2024 45-nm CSVCO study achieves only 120.7 μW at the VCO level, demonstrating that substantial system-level power optimization remains possible. These observations create a clear research opportunity for a complete 45-nm CSVCO-based PLL optimized for low energy, fast locking, and robust operation.

VII. PROPOSED METHODOLOGY BASED ON THE LITERATURE

1) Define system specifications: reference frequency, target output frequency, division ratio, supply voltage, tuning range, maximum power, lock criterion, and allowable phase noise/jitter.
2) Design the CSVCO: select the number of stages, current-starving devices, transistor dimensions, control-voltage range, and bias conditions. Optimize frequency, power, phase noise, and startup.
3) Design the PFD and charge pump: minimize transistor count and switching power while maintaining matched UP/DOWN currents, adequate output compliance, and low dead zone.
4) Design the loop filter: select charge-pump current and filter components to achieve the required bandwidth and damping factor while maintaining stable closed-loop operation.
5) Design the frequency divider: use a low-power divider architecture compatible with the VCO output frequency and required division ratio.
6) Integrate the PLL in Cadence Virtuoso and perform transient locking simulations. Report lock time using a clearly defined frequency/phase error window.
7) Perform AC/noise analysis, phase-noise analysis, and jitter estimation. Evaluate the influence of VCO gain and loop bandwidth.
8) Perform PVT corners and Monte-Carlo simulations to evaluate frequency spread, lock behavior, and power variation.
9) Compare the proposed design with the literature using normalized metrics such as power, tuning range, lock time, phase noise, jitter, and figure of merit.
10) Evaluate sustainability through total power, energy per locking event where applicable, circuit area, and the possibility of operation at reduced supply voltage.

VIII. EXPECTED CONTRIBUTION OF THE PROPOSED WORK

The proposed research is expected to contribute a systematic low-power design methodology for a 45-nm CMOS charge-pump PLL centered on a current-starved VCO. The principal contribution is not merely the use of a CSVCO, but the joint optimization of the oscillator and the complete PLL loop. The design will target a practical balance between low power and real-time performance, with special attention to lock time, tuning range, phase noise/jitter, and PVT

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robustness. The resulting architecture can be positioned for energy-constrained clock generation and frequency-synthesis applications such as IoT nodes, wearable electronics, wireless sensor interfaces, and compact SoC systems.

IX. CONCLUSION

The reviewed literature confirms that CSVCO-based architectures are promising for low-power PLL design, particularly in 45-nm CMOS where compact ring structures can provide high oscillation frequency without the area and power overhead of integrated inductors. The most directly relevant 45-nm studies demonstrate strong VCO-level power and phase-noise performance, while complete PLL studies show that PFD, charge pump, divider, and loop-filter power can substantially increase total consumption. Recent 2025 IEEE publications further indicate a shift toward supply-noise immunity and complete low-power PLL optimization. Consequently, the proposed sustainable PLL should be evaluated as a complete closed-loop system rather than as a VCO alone. A 45-nm CSVCO combined with low-power PFD/charge-pump and divider design, stable loop-filter selection, and PVT/noise analysis provides a technically justified direction for achieving low energy consumption with fast and reliable real-time locking.

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Note on Literature Selection

The review has been expanded to 15 papers, with emphasis on direct 45-nm CSVCO/PLL relevance and recent IEEE work. The 2025 APCCAS paper is the most recent directly relevant IEEE paper identified in the present search. Bibliographic metadata and final page numbers should be verified in IEEE Xplore or the publisher database immediately before thesis submission. Some non-IEEE papers are intentionally included because they provide technically useful 45-nm CSVCO and PVT data that strengthen the literature review.