IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 8, August 2026

DOI: 10.17148/IJIREEICE.2026.14812

A Survey on Recent Research Trends Towards A Comprehensive Review of Energy-Efficient FIR Filters on FPGA

Anooshka G[1], Dhrriti Shree D[2], Sri lakshmi BM[3], Mrs. N S Mythreye [4]

Dept. of EE-VLSI Design and Technology, SKIT, Bengaluru, India[1,2,3]

Assistant Professor, Dept. of ECE, SKIT, Bengaluru, India[4]

Abstract: Digital Signal Processing (DSP) is an important technology in modern communications, biomedical, audio, and image processing systems. The Finite Impulse Response (FIR) filter is widely used in digital signal processing due to its inherent stability, linear-phase characteristics, and efficient hardware implementation. FPGA-based implementations of FIR filters offer advantages such as high-speed operation and design flexibility; however, they often encounter challenges related to increased power consumption and hardware complexity. The paper provides a comprehensive review of recent low-power FPGA implementations of low-pass FIR filters, focusing on advanced optimization methods, including DA, CSD encoding, multiplier-less architectures, pipelining, coefficient optimization, and clock gating. It also compares the performance of these techniques in terms of power efficiency, latency, and hardware complexity, and discusses emerging challenges, research gaps, and future research opportunities.

Keywords: Digital Signal Processing, Energy Efficiency, Low-Pass Filter, FPGA, Finite Impulse Response, Hardware Optimization, Low-Power Design, Verilog HDL

I. INTRODUCTION

Digital Signal Processing (DSP) is one of the most important technologies in modern electronic systems because of its ability to process, analyze, and manipulate digital signals with high accuracy and reliability. It is widely used in communication systems, biomedical, instruments, consumer electronics, radar systems, image processing, speech recognition, wireless networks, and so on. Due to the increasing need for high-speed, real-time signal processing, digital filters are indispensable for enhancing signal quality by eliminating unwanted noise and interference while preserving useful information.

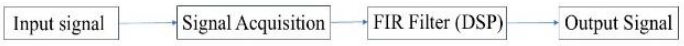

Fig. 1. Basic Digital Signal Processing System

One of the most widely used classes of digital filters is the low-pass FIR filter. These filters allow the low-frequency components of an input signal to pass, and attenuate the higher components, which usually correspond to unwanted noise. These features make low-pass FIR filters popular in audio enhancement, biomedical signal processing, image processing, wireless communication, instrumentation, and industrial automation. The ideal frequency response of a FIR low-pass filter is as shown in Fig. 2.[6]

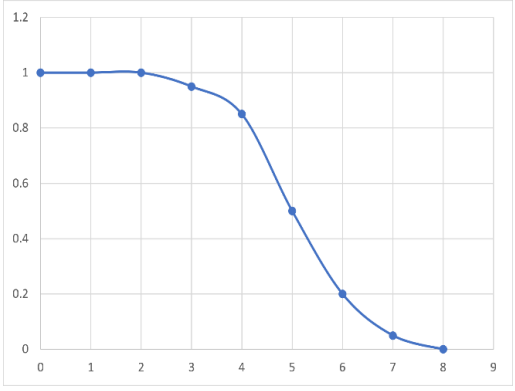

Fig. 2. Ideal Frequency Response of a Low-Pass FIR Filter

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 8, August 2026

DOI: 10.17148/IJIREEICE.2026.14812

Field Programmable Gate Arrays (FPGAs) have emerged as an efficient platform for implementing FIR filters due to their parallel processing capability, reconfigurability, and high computational speed. Compared to software-based implementations, FPGA-based designs offer improved performance and support real-time signal processing applications. However, implementing FIR filters on FPGA requires multiple multipliers, adders, and delay elements, which increase power consumption, hardware complexity, and resource utilization. The basic architecture of an FPGA is illustrated in Fig.3. [2]

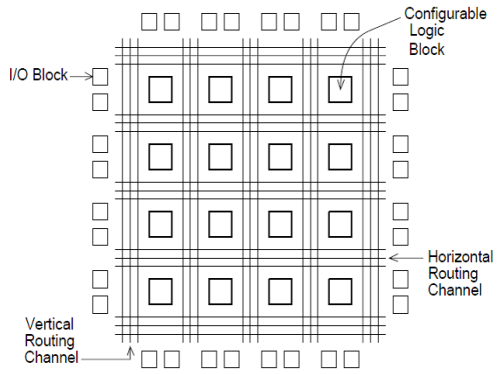

Fig.3. Basic FPGA Architecture

However, there are several challenges in implementing FIR filters in FPGA platforms despite these advantages. Conventional FIR filter architectures require multiple multipliers, adders, and delay elements to perform convolution operations, resulting in increased power consumption, higher hardware resource utilization, and higher propagation delay. In modern applications, the proliferation of portable and battery-powered electronic devices has made power consumption reduction a major design objective, without compromising computational performance.[4]

To address these problems, researchers have proposed a number of optimization techniques to improve the energy efficiency of FPGA-based FIR filters. Several techniques like Distributed Arithmetic (DA), Canonical Signed Digit (CSD) representation, multiplier-less architectures, pipelining, coefficient optimization, and clock gating have been extensively explored to minimize power consumption, reduce delay, and enhance hardware utilization at the same time retaining the performance of the filter.[2]

Parameter	FIR Filter	IIR Filter
Stability	Always Stable	May Become Unstable
Phase Response	Linear	Non - Linear
Feedback	Not Required	Required
Computational Complexity	Higher	Lower
Applications	Audio, Biomedical, Communication	Control Systems, Speech Processing

Table I. Comparison between FIR and IIR Filters

This review paper gives an in-depth survey of energy-efficient low-pass FIR filter architectures implemented on FPGA. This paper critically reviews the recent optimization techniques and compares their performance in terms of power consumption, delay, hardware utilization, and computational efficiency. The research gaps are identified, and future research opportunities are discussed in the design of low-power FPGA-based FIR filters for the next generation of digital signal processing systems.[2]

II. FUNDAMENTALS OF FIR FILTERS

2.1 Digital Filters

Digital filters are fundamental components in Digital Signal Processing (DSP) systems that manipulate digital signals to enhance desired information and suppress unwanted noise or interference. They perform mathematical operations on sampled input signals to modify their frequency characteristics according to application requirements. Digital filters are widely used in communication systems, biomedical instrumentation, image processing, audio enhancement, radar, and control systems due to their high accuracy, reliability, and flexibility.

Based on their impulse response, digital filters are classified into two major categories: **Finite Impulse Response (FIR)** filters and **Infinite Impulse Response (IIR)** filters. FIR filters are preferred in applications requiring linear phase response and guaranteed stability.[2]

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 8, August 2026

DOI: 10.17148/IJIREEICE.2026.14812

2.2 Finite Impulse Response (FIR) Filters

A Finite Impulse Response or FIR filter is a digital filter that has an impulse response that decays to zero in a finite number of input samples. Since there is no feedback in FIR filters, the output is a function only of the present and past input samples. This means that FIR filters are inherently stable and less sensitive to numerical errors. These properties make FIR filters highly suitable for applications that require high signal accuracy as well as predictable behavior.[5]

The mathematical representation of an N-tap FIR filter is:

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k)$$

where:

- **x(n)** = Input signal
- **y(n)** = Output signal
- **h(k)** = Filter coefficients
- **N** = Number of filter taps

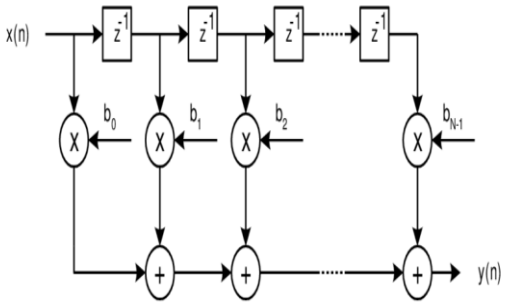

Fig. 4. Basic FIR Filter Architecture [2]

2.3 Low-Pass FIR Filters

A low-pass FIR filter lets low-frequency parts of a signal pass through while reducing high-frequency parts beyond a certain cut-off frequency. These filters are often used to eliminate unwanted noise and improve signal quality in many DSP applications. The filter coefficients set the frequency response and directly affect how well the filter works. Low-pass FIR filters are commonly used in audio processing, biomedical signal conditioning, wireless communication systems, sensor data collection, and image smoothing because they preserve useful information while effectively cutting down noise.[6]

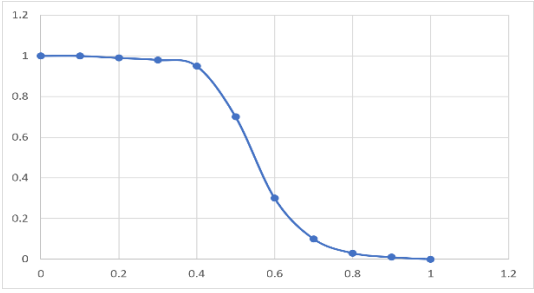

Fig. 5. Frequency Response of a Low-Pass FIR Filter.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 8, August 2026

DOI: 10.17148/IJIREEICE.2026.14812

2.4 FPGA Technology for FIR Filter Implementation

Field Programmable Gate Arrays (FPGAs) are integrated circuits that can be customized for a particular application after they are manufactured. These devices are comprised of configurable logic elements, programmable routing resources, I/O blocks, memory resources, and dedicated DSP blocks. Designers can program these elements to create nearly any digital circuit imaginable, without the need for custom hardware.

FPGAs are well-suited for FIR filter implementation for several reasons. Their parallel processing capabilities provide high operating speeds; they offer high levels of design flexibility, as filters can be easily reprogrammed; the FPGA architecture facilitates a relatively short development time; and the dedicated DSP blocks and embedded memory resources are used in implementing many of the arithmetic operations required to form a digital filter. Based on these factors, FPGA implementations are popular for many real-time signal processing applications.

Despite the advantages of FPGAs, implementing an FIR filter on such devices is not without its drawbacks. Resource usage (including hardware elements such as LUTs, flip-flops, BRAMs, DSP elements, etc.), power consumption, and the designer's effort in optimizing the implemented circuit can all increase. This is why numerous techniques that optimize an implemented FIR filter to minimize energy consumption while retaining processing performance have been reported. These techniques are reviewed in subsequent sections.[2]

III. ENERGY-EFFICIENT FPGA IMPLEMENTATION TECHNIQUES

Energy consumption has been a growing concern in the design of portable and battery-powered electronic products that rely on high-performance digital processing. Conventional implementations of the FIR digital filter may result in very large power consumption and an increase in logic element count and propagation delay. These implementations require numerous multipliers, adders, and delay components.[4]

Overcoming these limitations leads to increased design efficiency by implementing optimized multipliers with fewer logic element counts and improved delay. Researchers have addressed these limitations with numerous techniques aimed at reducing energy consumption while optimizing speed and resource utilization in the implementation of FIR digital filters. Out of these, the most efficient techniques are summarized below.

3.1 Distributed Arithmetic (DA)

Distributed Arithmetic (DA) is a frequently utilized technique for the implementation of an FIR digital filter on FPGAs. Instead of utilizing discrete multipliers that require considerable hardware cost, DA implements an arithmetic function through the use of Look-Up Tables (LUTs), which may pre-compute and store results, thus transforming arithmetic shifts and adds to replace many multiplications. The logic associated with DA provides much the same outcome as conventional filters but with less hardware. [2]

Modern FPGAs with many embedded LUT blocks make this one of the best approaches for FPGAs to balance speed, power, and resource usage. The large size of an FPGA allows researchers to implement this with a smaller number of BRAMs; as the coefficient becomes greater, the size of the LUT also will become greater, resulting in usage of more memory [2].

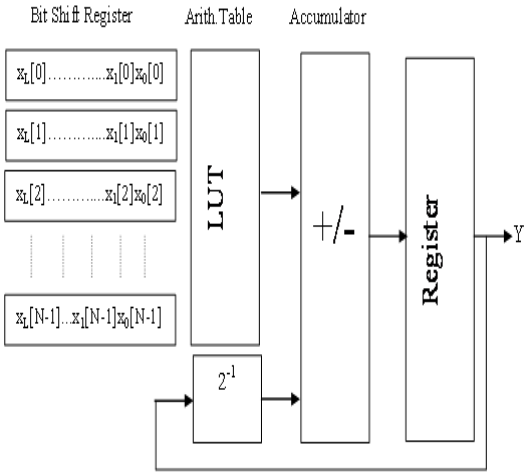

Fig. 6. Block Diagram of Distributed Arithmetic-Based FIR Filter.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 8, August 2026

DOI: 10.17148/IJIREEICE.2026.14812

3.2 Canonical Signed Digit (CSD) Representation

Canonical Signed Digit (CSD) representation is one of the optimization approaches that can be used for reduction of the number of operational bits. In CSD number representation, non-zero binary bits should be present at limited places, thereby minimizing multiplication, which reduces power, delay, and logic elements. This method helps to minimize multiplications for the coefficient with non-zero digits.[2]

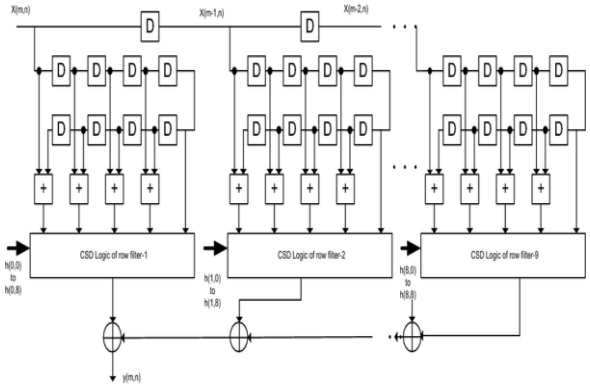

Fig. 7. Example of CSD Representation

3.3 Multiplier-less FIR Architectures

To minimize hardware usage as well as energy consumption, some multipliers may be removed entirely and replaced with operations of shift-adds, which are easier to implement on hardware as they do not require as much logic or dissipate as much power as full multipliers. The approach works best with filters of a reduced coefficient range. This is a preferred low-power strategy when the number of coefficients and the available logic resources are constraints.[4]

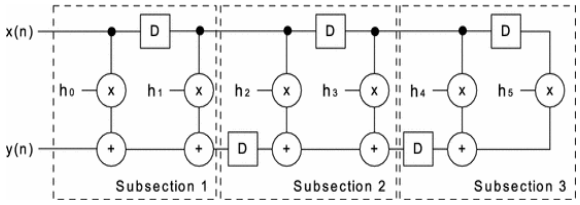

Fig. 8. Multiplier-less FIR Architecture

3.4 Pipelining Technique

Pipelining is a method of restructuring operations to enable a greater degree of parallelism within and between such operations to produce new outcomes for given results and subsequent operations to start as early as possible. It reduces the critical path length to improve efficiency in speed for FPGA-based digital systems. Although a pipelined filter structure utilizes more Flip-flops (FFs), which increase power Consumption, it drastically increases performance in real-time applications due to the removal of the dependence of the throughput on this critical path delay.[3]

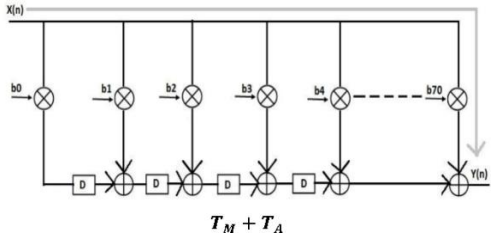

Fig. 9. Pipelined FIR Filter Architecture

3.5 Clock Gating

Clock gating is an active technique that significantly reduces the dynamic power dissipation of the FIR filters realized on FPGA. In this method, the clock is disabled for active design cells that are temporarily in sleep mode; this eliminates spurious switching and thus reduces the overall switching power dissipation of FIR filters. This makes clock gating a

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 8, August 2026
DOI: 10.17148/IJIREEICE.2026.14812

popular low-power technique used in low-power FPGA designs, while its major drawback comes in additional design overhead required for implementing control logic that controls the clock gating technique; however, it can be employed together with techniques like Distributed Arithmetic and Pipelining.[2]

3.6 Coefficient Optimization

The performance of a particular FIR filter is strongly governed by the filter coefficients, and the selection and placement of coefficients are crucial in reducing the hardware implementation area, Power consumption, and speed, and improving computation efficiency by performing a number of possible operations effectively. Coefficient optimization is often applied together with Distributive arithmetic and carry-save adders to give better hardware area and higher speed. Various optimization approaches have evolved.

We have considered various optimization approaches for designing FIR filters on the basis of power consumption, speed, and area. Different approaches include: Distributed arithmetic, Adaptive LMS algorithm, Simulated Annealing Algorithm, clock gating technique, pipelining, and a reduction in the number of multiply/add operations in FIR filter implementation using multiplication optimization of coefficients (as used for DA design with CSAs). In this section, we have considered various Research papers with their discussed application domains.

IV. ANALYSIS OF EXISTING RESEARCH

Research in FPGAs has gone through with a major focus over various optimization techniques like Distributed Arithmetic (DA), Offset Binary Coding (OBC), pipeline, and retiming techniques for better throughput and minimizing hardware utilization, and various approaches like Simulated annealing, heuristic, metaheuristic based for reducing power. In FPGAs, for efficient as per application. Some representative recent research studies have been discussed under the broad categories as:

VIDYA D S et al. (2024) proposed the FIR Filter Design using DA-OBC Architecture. The researchers were able to significantly reduce the area, with better performance in terms of Speed and better power consumption with no loss of coefficient accuracy. This technique was used for FPGA by utilizing VERILOG HDL on XILINX ISE platform; this design has effectively achieved the performance benefit of low power consumption.

PAVITRA Y.J et al. (2023) had put forth the application of Simulated annealing for optimum structure-based implementation on FPGA and ASIC technology; by this means he had attempted to reduce the number of hardware utilizations for multipliers and adders, comparing Wallace and Dadda tree multiplier architecture, thereby optimizing the overall design.

High speed, Low power, and high throughput in implementing FIR filters. Research done on high-throughput and low-power FPGA implementations of FIR filters, using pipelining and retiming to improve computation speed while maintaining the delay and power consumption of the design at an adequate value.

Yamini Shanmugam et al (2021) have presented and implemented a study for designing an adaptive LMS-based approach on FPGA hardware for an energy-efficient FIR filter; their design, based on adaptively update co-efficient with the LMS algorithm, was developed in Verilog-HDL and implemented on the Xilinx Vivado platform. The performance based on Power consumption and area consumption for their design showed better performance in comparison to other basic filter structures. Furthermore, pipelined LMS-based filters provide greater computation speed.

Numerous studies focusing on multiplier optimization strategies have significantly enhanced the performance of FIR filters by targeting reduced switching activity and algorithmic complexity. Techniques including optimized CSA trees, specialized coefficient selection, and the adoption of DA for multiplier implementation have consistently proven beneficial for achieving high energy efficiency in contemporary FPGA-based DSP systems. The integration of these strategies not only decreases power draw but also alleviates resource constraints, thereby promoting broader accessibility and application across a wider spectrum of digital signal processing tasks.

V. RESEARCH GAP

An overview of the literature indicates that substantial progress has been made toward the efficient realization of FIR filters on FPGAs, encompassing a variety of established and emerging optimization techniques. Distributed Arithmetic, adaptive filter algorithms such as LMS, advanced optimization methods like simulated annealing, pipelining, and multiplier design improvements (including DA implementation of multipliers) have all demonstrably contributed to reductions in power consumption, hardware resources, and latency.

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 8, August 2026
DOI: 10.17148/IJIREEICE.2026.14812

While individual optimization strategies demonstrate merit, the following aspects remain open for further investigation: A comprehensive approach focusing on integrating multiple optimization strategies into a holistic system architecture has been relatively underexplored. Many research efforts tend to focus on optimizing one or a few metrics (power, area, throughput) at a time, rather than simultaneously achieving a favorable balance across all desired performance parameters. This lack of an integrated perspective may lead to solutions that are optimal in isolation but suboptimal when considering the overall design objectives. Further, generalization of current research findings is limited, as performance is often reported on specific FPGA devices or application contexts. Evaluating architectures across a broader range of platforms and realistically representative workloads would provide more robust benchmarks for comparative analysis. Moreover, there is scope for research into developing novel hybrid optimization techniques that combine the benefits of diverse existing methods to push the boundaries of energy efficiency and performance for FPGA-based FIR filters.

VI. FUTURE SCOPE

For the efficient Low-pass FIR filter-based FPGA implementation using various optimization techniques, as we reviewed the existing work. There is much more scope for future research to be carried out to bring optimization to a better level. Future direction of this research could be: to explore more hybrid optimization techniques by integrating the listed optimizations (DA, coefficient optimizations, clock gating, pipelining, etc.) to obtain the desired goal.

Implement various Optimization techniques using machine learning or artificial intelligence (AI) based automatic optimization for coefficients or for the entire filter architecture.

In order to take the best out of optimized structures, new optimized FIR designs need to be developed in advanced technologies for new FPGAS such as XILINXARTIX-7 ZYNQ, OR XILINX Vance Architecture, or INTEL FPGA devices to carry out more efficiently by providing ultra-highly efficient designs with high speed and lower clock cycle frequency. Future research may be initiated in designing and implementing advanced types of FPGA which are adaptive and programmable filters for next-generation applications like $5G$, biomedical systems, and Internet of Things (IoT), and so on. We look forward to developing and comparing the optimized performance of adaptive F. I. R. filters compared to their non-adaptive version for their energy efficiencies and hardware cost.

VII. CONCLUSION

This paper has provided an exhaustive and comparative study on different techniques for realizing a power- and area-efficient low-pass FIR filter on FPGA. A wide range of optimizations, ranging from Distributive Arithmetic (DA) based, Adaptive LMS, Pipelining technique, Clock gating technique as well as reduction of multiplier and adder's operations using optimized coefficients for FIR Filters in FPGA's has been reviewed. Through comprehensive analysis and comparison of the research papers discussed, it is found that each of the techniques presented offers specific advantages & limitations, depending on the specific requirements of the application for which it is intended.

For Example, the DA technique provides a solution to the reduction of the number of multipliers.

While pipelining and clock gating can help in improving speed and power consumption, an adaptive filter offers better overall filtering performance for time-varying or unpredictable signals. In overall view of all considered optimization techniques, many advances have been gained. However, a better approach for fully synergistic optimization and thus creating a better balance between power consumption, hardware usage, and performance remains an open issue. It is hoped that further research based on this review can help toward more innovation and efficiency in the next generation of signal processing-based applications on FPGA platforms.

REFERENCES

[1] Vidya D. S. et al. (2024). FIR Filter Design using DA-OBC Architecture. Focuses on implementing an energy-efficient FIR filter using Distributed Arithmetic and Offset Binary Coding, achieving reduced area and power consumption while maintaining coefficient accuracy.
[2] Pavitra Y. J. et al. (2023). Simulated Annealing-Based Optimization for FIR Filter Implementation. Explores simulated annealing-based optimization for FPGA and ASIC implementation to reduce hardware utilization, particularly the number of multipliers and adders.
[3] High-Speed, Low-Power and High-Throughput FIR Filter Implementation. Investigates FPGA-based FIR filter implementation using pipelining and retiming techniques to improve computation speed while maintaining acceptable delay and power consumption.
[4] Yamini Shanmugam et al. (2021). Adaptive LMS-Based Energy-Efficient FIR Filter on FPGA. Presents an adaptive LMS-based FIR filter implemented using Verilog HDL and Xilinx Vivado, focusing on improved power and area performance. The pipelined LMS-based design also provides higher computation speed.