IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026

DOI: 10.17148/IJIREEICE.2026.14707

A novel system for comparing viscosity of two liquids via flow time delays and providing indications about liquid quality, using photo-interrupter sensors and implemented with FPGAs and VHDL

Dr Evangelos I. Dimitriadis[1], Leonidas Dimitriadis[2]

Department of Computer, Informatics and Telecommunications Engineering, International Hellenic University,

End of Magnisias Str, 62124 Serres Greece[1]

Undergraduate student, Department of Information and Electronic Engineering, International Hellenic University,

57400, Sindos Thessaloniki, Greece[2]

Abstract: A novel system which uses FPGAs and VHDL for comparing viscosity of two liquids, with the first one being the standard liquid and the second being the tested one, is presented here. The system monitors flow delay times of both liquids using two corresponding photo-interrupter sensors. If the opaque liquid goes through sensor slot, sensor transits to HIGH state with simultaneous time value storing. Our system is programed to calculate and display in FPGA board's seven-segment displays, the signed time values difference of the two liquids, thus indicating whether standard or tested liquid reaches corresponding photo-interrupter sensor first and also what is the magnitude of viscosity difference of the two liquids. A set of output LEDs is also programed to light up, in order to present the level of the above time difference depended viscosity variance of the two liquids. Our algorithm works fine also with transparent liquids as long as liquid flow tubes are sufficiently thick (several millimeters), in order to prevent infrared radiation passing through the liquid. Our system is cheap to manufacture, easy to use and able to process simultaneously, due to FPGA use, a large number of tested liquids in industrial environments, allowing it to produce valid information for liquid samples by combining it with IoT and AI systems.

Keywords: Viscosity, photo-interrupter sensors, liquid flow, FPGA, VHDL, LEDs.

INTRODUCTION

It is well known that FPGAs have attracted attention of a great number of researchers in the recent years, for industrial as well as for a variety of other applications. [1-15] FPGAs have the main advantage of combining software and hardware, thus enabling hardware programming for a series of applications. The most used languages for FPGAs' programing are VHDL and Verilog and VHDL is the one used in our work.

Although a lot of work has been done concerning implementation of FPGAs in a variety of applications as mentioned above, we found no works dealing with viscosity measurements using FPGAs.

We present here a system which monitors simultaneously, time dependent liquid flow of standard and tested liquids, providing us useful and valid information about time delays of liquid flows and subsequently indicating differences in liquids' viscosities.

It can be useful for checking tested liquid quality, compared with a standard liquid. The use of FPGA board in our system provides us all the advantages of these boards, such as real-time signal processing and control, deterministic latency and high-speed parallelism.

Real time is crucial for dynamic flow profiling and high-frequency analysis, while deterministic latency ensures that measurements are precisely time-stamped and synchronized. The third advantage of parallelism allows simultaneous signal generation, data acquisition, and mathematical modeling without relying on sequential CPU cycles.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026

DOI: 10.17148/IJIREEICE.2026.14707

Consequently our system can also provide information to a central AI based system or send useful data via 5G system to a remote controlling system of an industrial environment in order to achieve large number of simultaneous liquid testing and analyzing, due to large number of FPGA's I/O and GPIO pins.

DESIGN OVERVIEW AND OPERATION OF THE SYSTEM

Figure1 presents device overview and operational units of our system, using FPGA DE10-Lite board, while Figure 2 presents circuit diagram of the system. Subsequent Figure 3a, b presents the implemented viscosity comparing system of this work.

It is obvious from the above figures that our system, except from DE10-Lite FPGA board, contains also some basic circuit parts. It uses two photo-interrupter KY-010 sensor units, acting as main inputs, with their corresponding white LED, acting as output and light up when an opaque object passes through sensor's slot, causing its transition to HIGH state. We can also see two thin tubes used for liquids supply, which are fixed inside the sensor slot, in order to cause sensor's transition to HIGH state as soon as liquid passes through them.

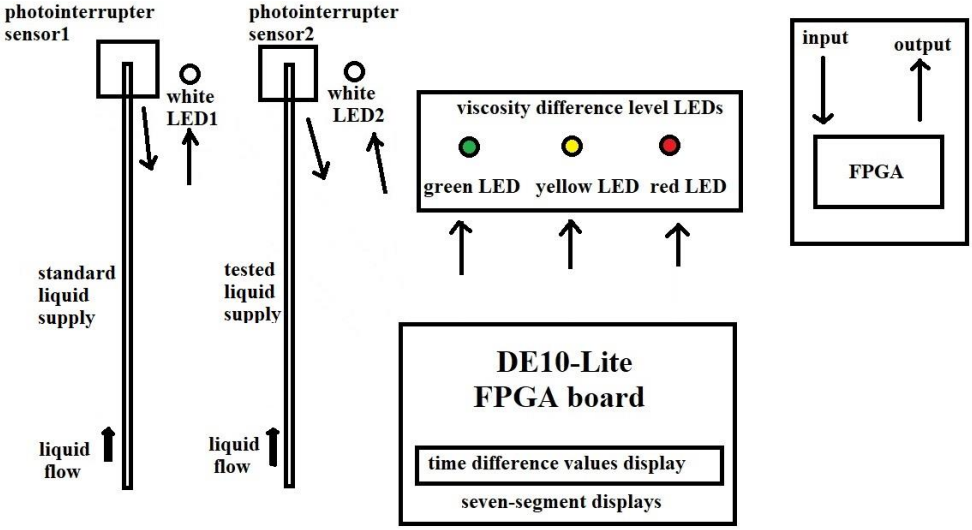


Figure 1: Device overview and operational units of our system.

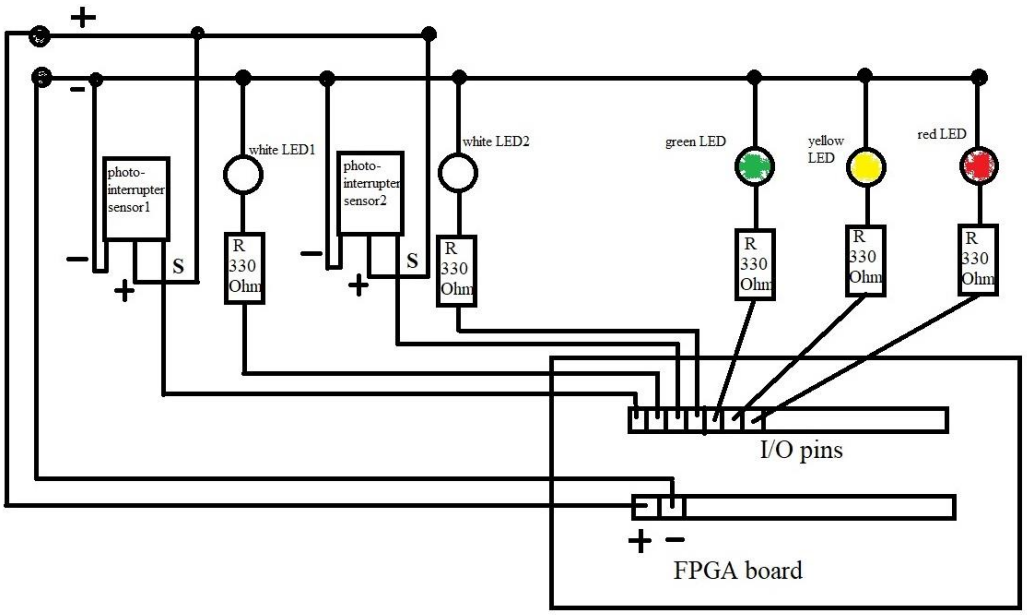


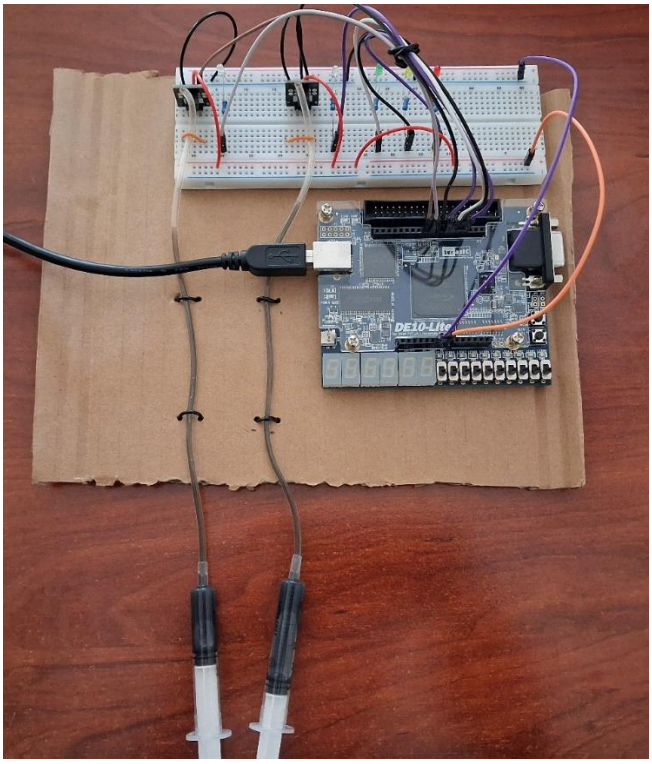
Figure 2: Circuit diagram of our system

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

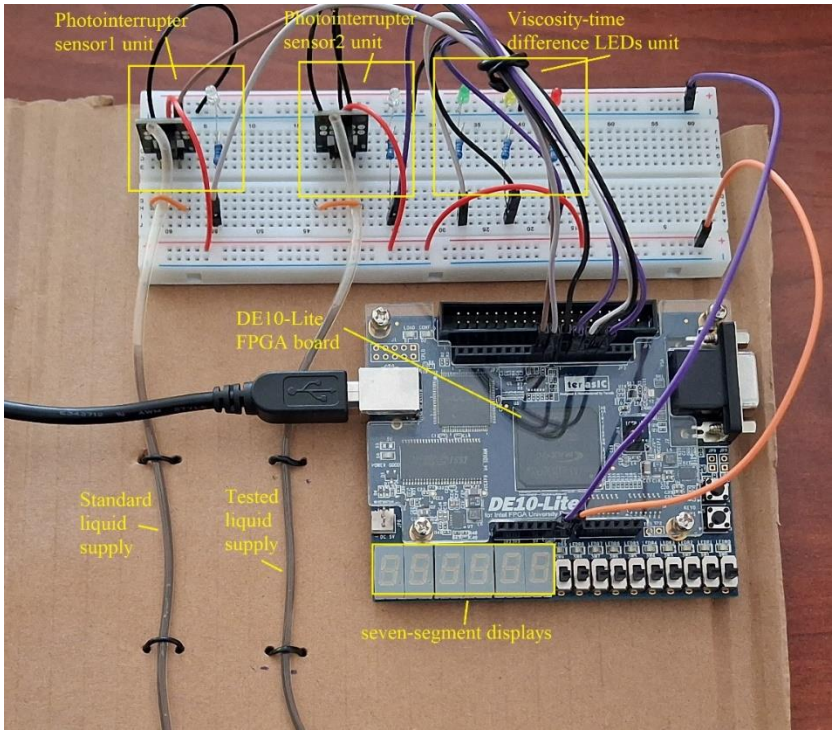
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026

DOI: 10.17148/IJIREEICE.2026.14707



a)



b)

Figure 3a, b: The implemented viscosity comparing system of this work.

It must be mentioned here that KY-010 photo-interrupter sensor has a thin slot of about 2mm, so we were forced to use thin tubes for liquids supply. That is the reason why we used a black colored liquid, in order to achieve sufficiently opaque liquid layer for infrared radiation, in sensors slots. The system is also able to test transparent liquids provided that a thick sensor slot of more than 5mm will be used. In contrast to an industrial application of our system, which

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026
DOI: 10.17148/IJIREEICE.2026.14707

would involve small reservoirs of the fluids under test, here we use two small syringes to manually induce liquid flow through the tubes.

Viscosity and time difference level LEDs unit also exists in our system, containing three LEDs (green, yellow and red) also acting as system's outputs. Time is the other input value used here and it is provided by FPGA's clock.

Our viscosity comparing system starts operating as soon as power supply +5V is applied to the circuits via DE10-Lite appropriate pins and the VHDL program is sent via USB Blaster interface, to FPGA chip. Input values from both photo-interrupter sensor units and FPGA's clock are entered in our system. Time difference value of sensors' upon transition to HIGH state, are calculated and presented in seven-segment displays of the FPGA board.

Figure 4 presents the viscosity comparing system in operation mode. Both sensors are at LOW state because no liquid has entered in sensors' slots, with both corresponding white LEDs of sensor units to OFF state and green LED ON, meaning that no time difference in reaching sensors' slots is detected. Needless to mention that all LEDs used in our system are protected with a 330 Ohm series resistance and they are connected to I/O pins of the FPGA board acting as outputs for our system, as mentioned above.

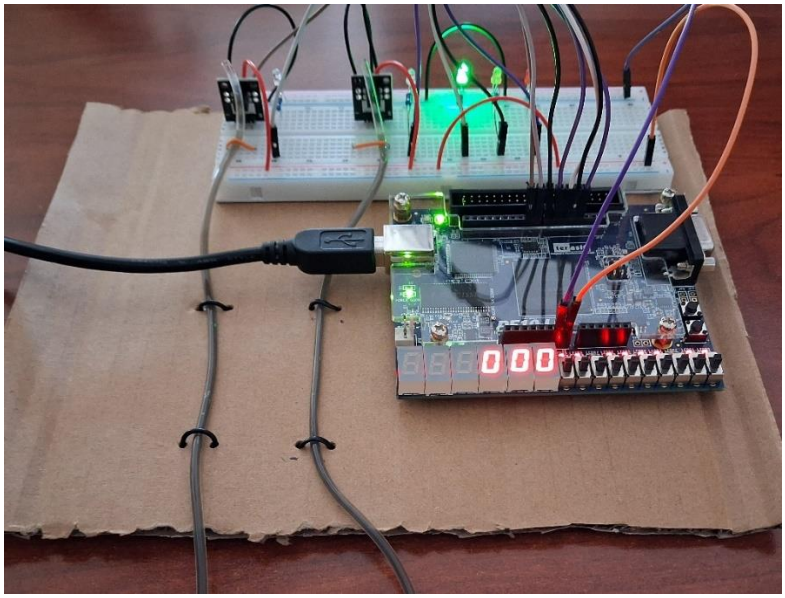


Figure 4: The viscosity comparing system in operation mode. Both sensors are at LOW state with corresponding white LEDs OFF and green LED ON, meaning that no time difference is detected.

The system provides the ability of setting time difference period levels of sensors transition from LOW to HIGH state, as long as it is needed, depending on the application that our system is used. If sensors time difference >0 seconds AND time difference<=3 seconds, then yellow external LED lights up. If time difference >3 seconds then red external LED lights up. Green LED is ON in case that zero time difference is detected. The above limits can be set by the programmer depending on the kind of liquids we are testing.

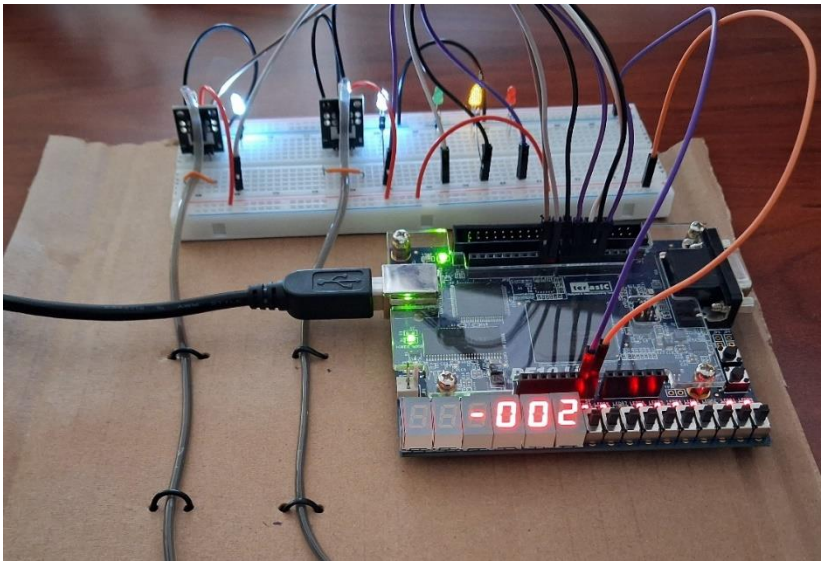
Figure 5 presents the viscosity comparing system in operation mode. In Figure 5a) tested liquid delays 2 seconds for reaching sensor slot, compared to standard one, thus minus sign is shown. Yellow LED lights up because time difference for two liquids is lower than 3 seconds and both sensors' white LEDs are also ON, informing us that both liquids reached sensor slot. In Figure 5b) the delay is 5 seconds so red LED is ON. In both cases of Figure 5 tested liquid has higher viscosity value, compared to standard one.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

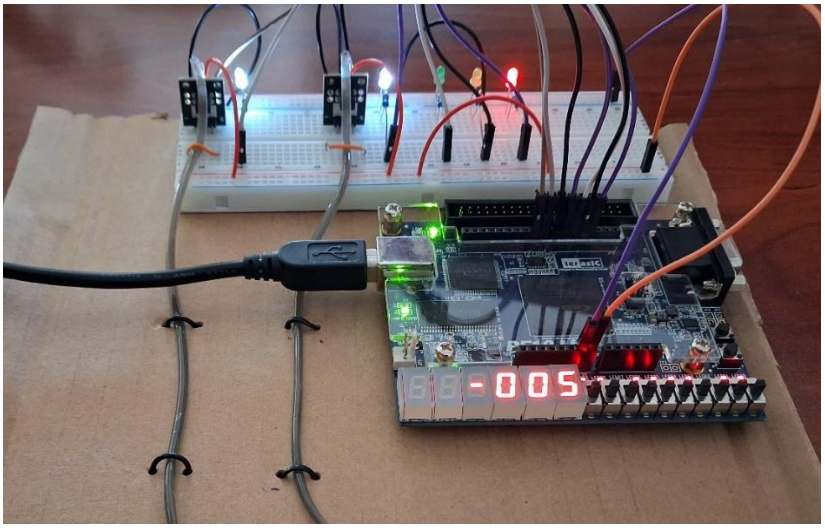
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026

DOI: 10.17148/IJIREEICE.2026.14707



a)



b)

Figure 5a, b: The viscosity comparing system in operation mode. 5a) Tested liquid delays 2 seconds compared to standard one, thus minus sign is shown. Yellow LED lights up and both sensors' white LEDs are also ON, while in 5b) the delay is 5 seconds so red LED is ON.

Poiseuille's law is applied to our system. For a liquid flowing through a cylindrical tube, the average flow velocity u depends on the viscosity according to the mathematical formula:

$$u = \frac{\Delta P \cdot R^2}{8\eta L}$$

ΔP: the pressure difference driving the flow, R: the radius of the tube, η: the viscosity coefficient of the fluid and L: the length of the tube.

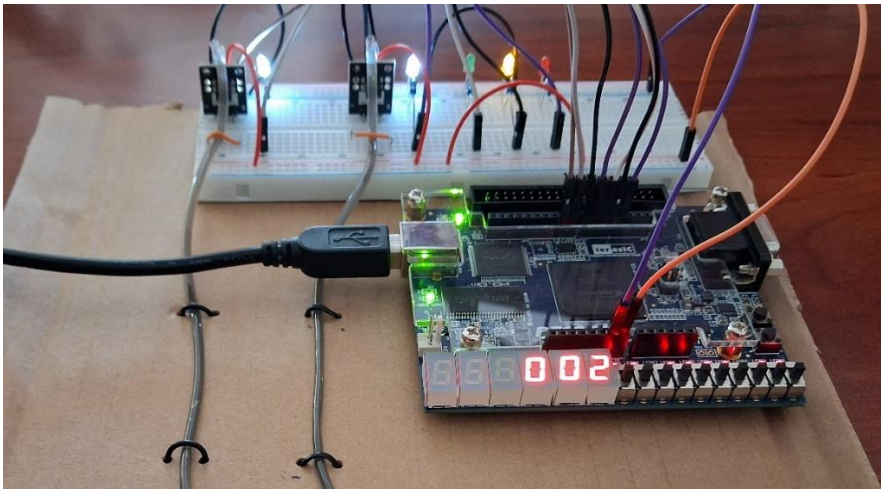
Taking into account that velocity is generally, inversely proportional to time, we conclude that the liquid that achieves lower time value for reaching sensor slot, has lower viscosity value, compared to the other liquid, by a factor equal to time difference.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

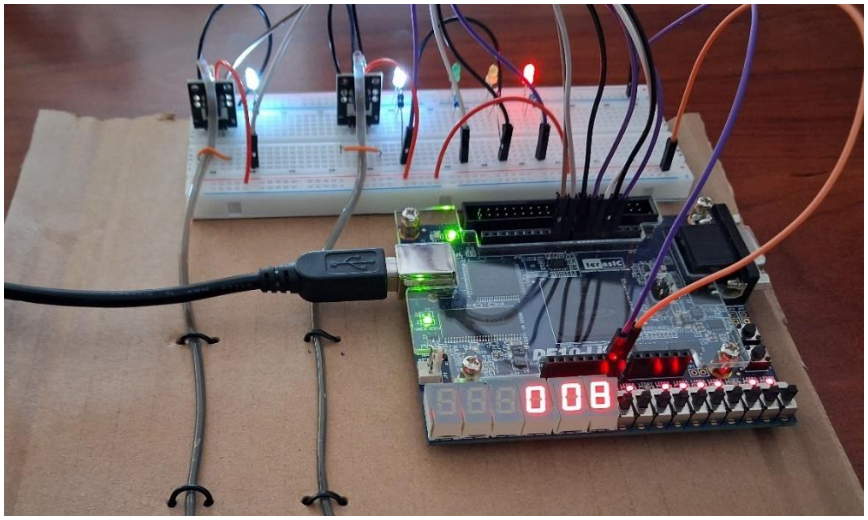
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026

DOI: 10.17148/IJIREEICE.2026.14707



a)



b)

Figure 6a, b: The viscosity comparing system in operation mode. a) Tested liquid precedes 2 seconds compared to standard one, thus no minus sign is shown. Yellow LED lights up and both sensors' white LEDs are also ON, while in b) the precedence of tested liquid over standard liquid is 8 seconds, so red LED is ON.

Figure 6 shows our viscosity comparing system in operation mode. In 6a) tested liquid precedes 2 seconds compared to standard one, thus no minus sign is shown. Yellow LED lights up because time difference is lower than 3 seconds and both sensors' white LEDs are also ON, while in 6b) the precedence of tested liquid over standard liquid is 8 seconds, so red LED is ON. In both cases of Figure 6 tested liquid has lower viscosity value, compared to standard one.

Figure 7 presents the ideal case of both sensors being simultaneously at HIGH state with corresponding white LEDs ON and green LED ON, meaning that no time difference is detected because sensor slots were simultaneously reached by both liquids. In this case both liquids have the same viscosity value.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026

DOI: 10.17148/IJIREEICE.2026.14707

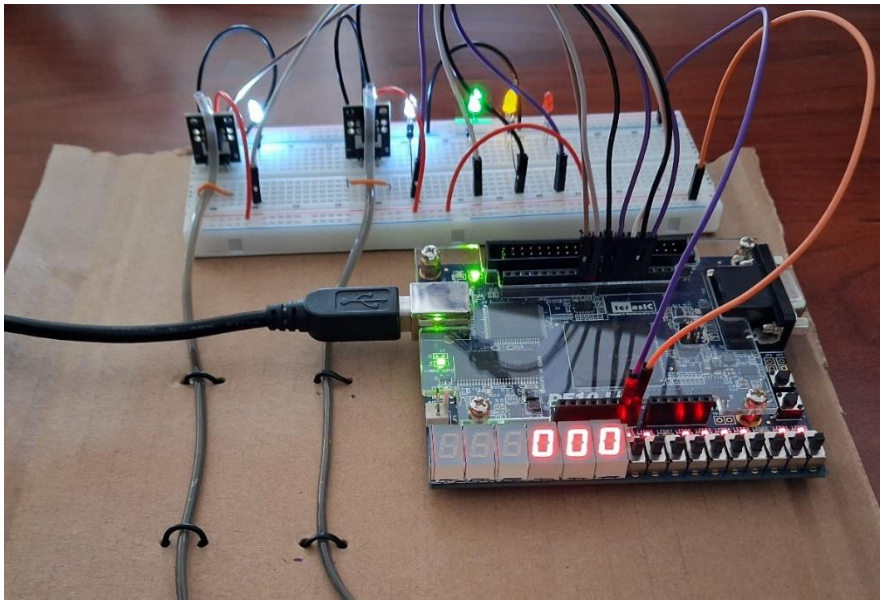


Figure 7: The viscosity comparing system in operation mode and ideal case. Both sensors are simultaneously at HIGH state with corresponding white LEDs ON and green LED ON, meaning that no time difference is detected because sensor slots were simultaneously reached from both liquids.

Finally we must mention that another important fact of our system's design is that it receives input sensor values periodically, ensuring continuous monitoring.

Our viscosity comparing system also offers the advantages of being easy to use and also cheap to manufacture. In case that our system is working simultaneously in 4-5 FPGA boards then hundreds of liquids could be compared to a standard one, giving fast and reliable results about liquid quality, thus avoiding possible liquid adulteration.

PROGRAMING THE SYSTEM

We used Quartus Prime Lite Edition 21.1.1 to create the VHDL programs of our system. It must be mentioned here that before proceeding with the VHDL programming of our system, we had to set a series of parameters controlling the operation of DE10-Lite FPGA's Analog to Digital Converter (ADC). This converter plays a very important role in the whole system operation, since it converts analogue to digital values. The files created by the above ADC parameters setting are imported into the final project of our system.

A flowchart diagram, presenting main functions of our system is presented in Figure 8, while the APPENDIX contains the whole VHDL program.

It is clear that the system operates five basic functions. All of them use processes in VHDL programming language. These processes are running as long as the system is ON. All external LEDs are programmed to work as logic outputs, thus they are at the ON state if they receive binary '1' as logic output. Photo-interrupter sensors are programmed to work as logic inputs of the system.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026
DOI: 10.17148/IJIREEICE.2026.14707

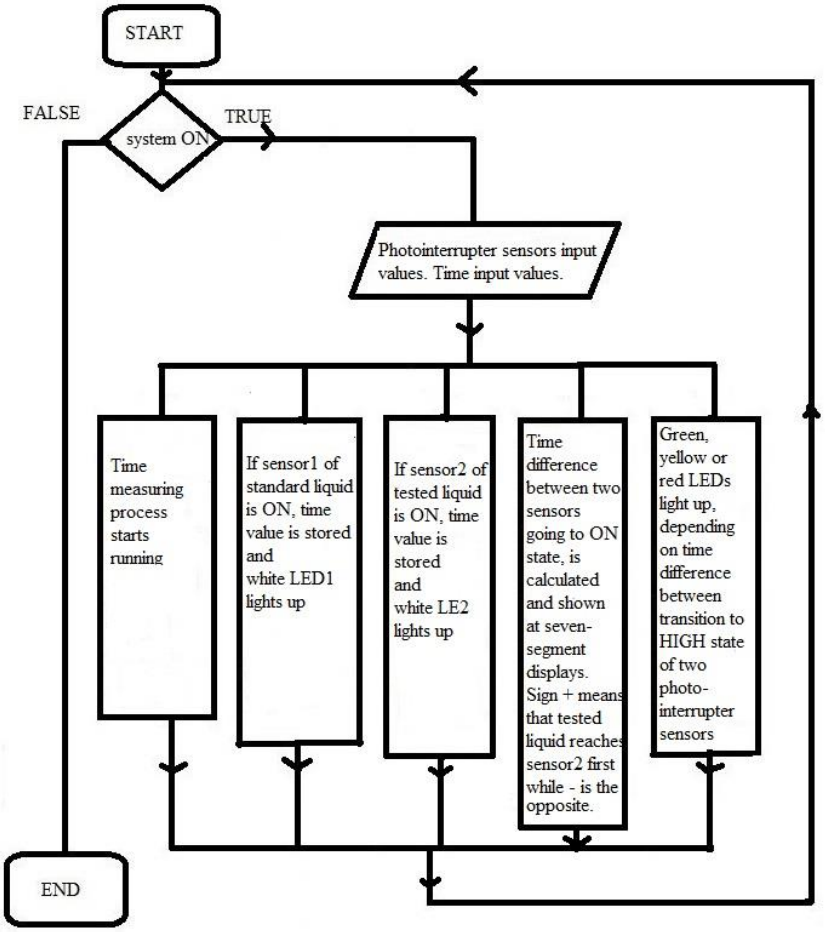


Figure 8: Flowchart diagram, presenting main functions-processes of our system.

First function of Figure 8 playing definitive role in system operation is the process based on FPGA board's clock for time measuring in seconds and is activated upon system's transition to ON state. It is a very important process because time parameter is needed in our system. Time values act as input to our system.

Second and third functions are related to sensor1 and sensor2, respectively. Upon standard liquid reaches sensor1 slot two smaller processes are activated with the first one storing time value t_1 and second one sending logic output '1' to white LED1. Similarly upon tested liquid reaches sensor2 slot, time value t_2 is stored and logic '1' is sent to white LED2.

Fourth function includes three smaller processes. First one calculates time difference between t_1 and t_2 time values mentioned above, while second process displays time difference in seven-segment displays of the FPGA board. Third process calculates the sign of time difference and display it to seven-segment displays. We programmed this process to show no sign, meaning positive difference $t_1 - t_2$ in case that $t_1 >= t_2$ and present to displays minus sign in case that $t_1 < t_2$. Positive time difference means that tested liquid reaches sensor slot faster than standard liquid, thus it has lower viscosity than standard liquid. Negative time difference shows higher viscosity value for tested liquid compared to standard one.

Finally, fifth function of our system is related to time difference level LEDs unit. It uses green, yellow and red external LEDs which are programed to light up, depending on time difference level, set by programmer. In case that both liquids reach simultaneously sensor slots time difference is zero and green LED is ON, indicating same viscosity values for standard and tested liquids. If time difference >0 seconds and time difference <=3 seconds (positive or negative difference) then yellow LED is ON indicating relatively small viscosity difference between standard and tested liquids. In case that time difference>3 seconds then red LED is ON, showing large values of viscosity difference for standard and tested liquids. All the above time difference levels can be set by programmer according to related application.

DOI: 10.17148/IJIREEICE.2026.14707

CONCLUSION

An FPGA-based viscosity comparing system, providing information about tested liquid quality, is presented in this work. Our system is able to monitor simultaneously liquid flows through small tubes, of a standard and tested liquid. The end of tubes is placed and fixed in two corresponding photo-interrupter sensors slots, one for each liquid, with sensors sending logic signal '1' upon liquid reaching the slot, with simultaneous time storing of liquid reaching slot taking place for both liquids. Calculated and presented in seven-segment displays signed time difference value of liquids reaching sensors slots, provides valid and reliable viscosity value information of tested liquid. White external LEDs related to each sensor, optically indicate whether sensors send logic '1' to FPGA board, while green, yellow and red external LEDs show the level of time difference and consequent viscosity difference for standard and tested liquids.

The system is easy to be manufactured, providing also the benefit of low cost. Additionally, time and subsequent viscosity difference level output logic signals, could be sent to an AI system to achieve simultaneous monitor of a large number of tested liquids, especially in the case that more than one FPGA boards are used in an industrial environment.

REFERENCES

[1]. M. Yussup, M.M. Ibrahim, L. Lombigit, N.A.A. Rahman and M.R.M. Zin, "Implementation of data acquisition interface using on-board field-programmable gate array (FPGA) universal serial bus (USB) link", Advanc. in Nuclear Research and Energy Development, AIP Conf. Proc. 1584, 69-72 (2014), doi: 10.1063/1.4866106

[2]. A. Gujar, International Journal of Computer Science and Information Technologies, "Image Encryption using AES Algorithm based on FPGA", vol 5, (5), 2014, 6853-6859

[3]. S. Singh, A.K. Saini, R. Saini, I.J. Image, Graphics and Signal Processing, "Interfacing the Analog Camera with FPGA Board for Real-time Video Acquisition" 2014, 4, 32-38, DOI: 10.5815/ijigsp.2014.04.04

[4]. S. Muthukrishnan and R. Priyadharsini, International Journal of Computer Science and Mobile Computing, "32-Bit RISC and DSP System Design in an FPGA" vol 3, issue 12, Dec. 2014, pg. 361-368

[5]. L. Chen, Y. Chang, L. Yan, IEEE Transactions on Geoscience and Remote Sensing, "On-orbit real-time variational image destriping: FPGA architecture and implementation", 10.1109/tgrs.2022.3140428, 2022, pp. 1-1

[6]. S. Yarlagadda, S. Kaza, A. Tummala, E. Babu, R. Prabhakar, Information Technology in Industry, "The reduction of Crosstalk in VLSI due to parallel bus structure using Data Compression Bus Encoding technique implemented on Artix 7 FPGA Architecture", 10.17762/itii.v9i1.151, 2021, Vol 9 (1), pp. 456-460

[7]. C. Du, Y. Yamaguchi, Electronics, "High-Level Synthesis Design for Stencil Computations on FPGA with High Bandwidth Memory", 2020, 9(8), 1275; https://doi.org/10.3390/electronics9081275

[8]. X. Hao, C. Lin and Q. Wu, Electronics, "A Parallel Timing Synchronization Structure in Real-Time High Transmission Capacity Wireless Communication Systems", 2020, 9(4), 652; https://doi.org/10.3390/electronics9040652

[9]. P. A. Bawiskar, R.K. Agrawal, International Journal of Innovative Research in Science, Engineering and Technology, "FPGA Based Home Security System" vol.4, issue 12, Dec. 2015, p. 12865-12869, DOI: 10.15680/IJIRSET.2015.0412139

[10]. K. Saroch, A. Sharma, IOSR Journal of Electronics and Communication Engineering, "FPGA Based System Login Security Lock Design Using Finite State Machine" vol 5, issue 3, Mar.-Apr. 2013, pp 70-75

[11]. R.S. Parikh, Int. Journal of Engineering Research and Application, "Alarm System Implementation on Field Programmable Gate Array" vol 8, issue 1, Jan. 2018, pp 01-04.

[12]. E. I. Dimitriadis and L. Dimitriadis, "A Simple, Low Cost and Multiple Input Alarm System, Functioning as Finite State Machine (FSM), Using VHDL and FPGAs", Journal of Active and Passive Electronic Devices, vol. 17, pp. 307–315, 2024.

[13]. E. I. Dimitriadis and L. Dimitriadis, "A g-sensor based alarm system, for multiple tilt sensor applications, using VHDL and FPGAs", Journal of Active and Passive Electronic Devices, vol. 18, pp. 119-129, 2024.

[14]. Evangelos I. Dimitriadis, Leonidas Dimitriadis and Aristeidis Grigoriadis, "A touch-sensing system for precise robotic arm control, using force-sensing resistors (FSR), VHDL and FPGAs", International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering, vol. 13, issue 7, pp. 36-50, July 2025.

[15]. Leonidas Dimitriadis and Evangelos I. Dimitriadis, "A Novel System for Monitoring and Controlling Industrial Engine Operation, using Vibration, Magnetic Field, Humidity and Temperature Sensors, Implemented with FPGAs and VHDL", International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering, vol. 14, issue 5, pp. 1-18, May 2026.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026

DOI: 10.17148/IJIREEICE.2026.14707

APPENDIX

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.std_logic_signed.ALL;
use ieee.std_logic_unsigned.ALL;
entity DE10_Lite_viscosity_photo_interrupter is
generic(ClockFrequencyHz : integer:=50000000);
port
(
rst : in std_logic; --SW8
nRst    : in std_logic; -- Negative reset
sensor1 : in std_logic;
sensor2 : in std_logic;
diff : buffer unsigned(31 downto 0);
time_diff : buffer integer;
led_yellow: buffer std_logic;
led_red: buffer std_logic;
led_green: buffer std_logic;
led_yellow_out: out std_logic;
led_red_out: out std_logic;
led_green_out: out std_logic;
led_white1: buffer std_logic;
led_white1_out: out std_logic;
led_white2: buffer std_logic;
led_white2_out: out std_logic;
sign : buffer std_logic;
-- Clocks
ADC_CLK_10: in std_logic;
MAX10_CLK1_50: in std_logic;
MAX10_CLK2_50: in std_logic;
-- KEYs
KEY: in std_logic_vector(1 downto 0);
-- HEX
HEX0: out std_logic_vector(7 downto 0);
HEX1: out std_logic_vector(7 downto 0);
HEX2: out std_logic_vector(7 downto 0);
HEX3: out std_logic_vector(7 downto 0);
ARDUINO_IO: inout std_logic_vector(15 downto 0);
ARDUINO_RESET_N: inout std_logic);
end entity;
architecture DE10_Lite_viscosity_photo_interrupter_Arch of DE10_Lite_viscosity_photo_interrupter is
-- Analog to Digital Converter IP core
component myADC is
port
(
clk_clk: in std_logic := 'X';
modular_adc_0_command_valid: in std_logic := 'X';
modular_adc_0_command_channel: in std_logic_vector(4 downto 0) := (others => 'X');
modular_adc_0_command_startofpacket: in std_logic := 'X';
modular_adc_0_command_endofpacket: in std_logic := 'X';
modular_adc_0_command_ready: out std_logic;
modular_adc_0_response_valid: out std_logic;
modular_adc_0_response_channel: out std_logic_vector(4 downto 0);
modular_adc_0_response_data: out std_logic_vector(11 downto 0);
modular_adc_0_response_startofpacket: out std_logic;
modular_adc_0_response_endofpacket: out std_logic;
```

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026
DOI: 10.17148/IJIREEICE.2026.14707

```
reset_reset_n: in std_logic
);
end component myADC;
signal modular_adc_0_command_valid: std_logic;
signal modular_adc_0_command_channel: std_logic_vector(4 downto 0);
signal modular_adc_0_command_startofpacket: std_logic;
signal modular_adc_0_command_endofpacket: std_logic;
signal modular_adc_0_command_ready: std_logic;
signal modular_adc_0_response_valid: std_logic;
signal modular_adc_0_response_channel: std_logic_vector(4 downto 0);
signal modular_adc_0_response_data: std_logic_vector(11 downto 0);
signal modular_adc_0_response_startofpacket: std_logic;
signal modular_adc_0_response_endofpacket: std_logic;
signal clk_clk: std_logic;
signal reset_reset_n: std_logic;
type state_machines is (sm0,sm1, sm2, sm3, sm4);
signal sm: state_machines;
-- signals to store conversion results
signal ADCIN1,ADCIN4, ADCIN3,ADCIN2: std_logic_vector(11 downto 0);
signal AD1,AD4, AD3,AD2: std_logic_vector(11 downto 0);
-- signal for BCD digits
signal digit2c, digit1c, digit0c: std_logic_vector(3 downto 0);
signal digit2, digit1, digit0: std_logic_vector(3 downto 0);
signal counter : unsigned(31 downto 0) := (others=>'0');
signal t1 : unsigned(31 downto 0) := (others=>'0');
signal t2 : unsigned(31 downto 0) := (others=>'0');
begin
-- ADC port map
adc1: myADC port map
(
modular_adc_0_command_valid => modular_adc_0_command_valid,
modular_adc_0_command_channel => modular_adc_0_command_channel,
modular_adc_0_command_startofpacket => modular_adc_0_command_startofpacket,
modular_adc_0_command_endofpacket => modular_adc_0_command_endofpacket,
modular_adc_0_command_ready => modular_adc_0_command_ready,
modular_adc_0_response_valid => modular_adc_0_response_valid,
modular_adc_0_response_channel => modular_adc_0_response_channel,
modular_adc_0_response_data => modular_adc_0_response_data,
modular_adc_0_response_startofpacket => modular_adc_0_response_startofpacket,
modular_adc_0_response_endofpacket => modular_adc_0_response_endofpacket,
clk_clk => clk_clk,
reset_reset_n => reset_reset_n
);
clk_clk <= MAX10_CLK1_50;
reset_reset_n <= KEY(0);
-- process for reading new samples
p1: process(reset_reset_n, clk_clk)
begin
if reset_reset_n = '0' then
        sm <= sm0;
elsif rising_edge(clk_clk) then
        case sm is
                when sm0 =>
                        sm <= sm1;
                        modular_adc_0_command_valid <= '1';
                        modular_adc_0_command_channel <= "00001";
                when sm1 =>
                        if modular_adc_0_response_valid = '1' then
```

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026
DOI: 10.17148/IJIREEICE.2026.14707

```
                        modular_adc_0_command_channel <= "00010";
                    ADCIN4 <= modular_adc_0_response_data;
                        sm <= sm2;
                    end if;
                when sm2 =>
                    if modular_adc_0_response_valid = '1' then
                        modular_adc_0_command_channel <= "00001";
                        modular_adc_0_command_channel <= "00011";
                        ADCIN1 <= modular_adc_0_response_data;
                        sm <= sm1;
                        sm <= sm3;
                    end if;
                when sm3 =>
                    if modular_adc_0_response_valid = '1' then
                        modular_adc_0_command_channel <= "00100";
                        ADCIN2 <= modular_adc_0_response_data;
                        sm <= sm4;
                    end if;
                when sm4 =>
                    if modular_adc_0_response_valid = '1' then
                        modular_adc_0_command_channel <= "00001";
                        ADCIN3 <= modular_adc_0_response_data;
                        sm <= sm1;
                    end if;
                when others =>
          end case;
end if;
end process;
process(MAX10_CLK1_50)
 begin
      if rising_edge(MAX10_CLK1_50) then
         if rst='1' then
            counter <= (others=>'0');
            t1 <= (others=>'0');
            t2 <= (others=>'0');

         else
            counter <= counter + 1;
            if sensor1='0' then
               t1 <= counter;
            end if;
            if sensor2='0' then
               t2 <= counter;
            end if;
         end if;
      end if;
   end process;
process (t1,t2) -- difference calculation
BEGIN
IF (sensor2='1' AND sensor1='0')    THEN
diff <= t1 - t2;
ELSIF (sensor2='0' AND sensor1='1') THEN
diff <= t2-t1;
END IF;
END PROCESS;
time_diff<= to_integer (diff/50000000);
process(sensor1, led_white1)
begin
```

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026
DOI: 10.17148/IJIREEICE.2026.14707

```
IF sensor1='1' THEN
led_white1<= '1';
ELSE
led_white1<='0';
END IF;
end process;
process(sensor2, led_white2)
begin
IF sensor2='1' THEN
led_white2<= '1';
ELSE
led_white2<='0';
END IF;
end process;
led_white1_out<= led_white1;
led_white2_out<= led_white2;
-- process for measuring and converting time_diff
process(time_diff)
variable d2, d1, d0: integer;
begin

d2 := (time_diff) / 100;
d1 := (time_diff) mod 100 / 10;
d0 := ((time_diff mod 100) mod 10);
digit2c <= std_logic_vector(to_unsigned(d2, 4));
digit1c <= std_logic_vector(to_unsigned(d1, 4));
digit0c <= std_logic_vector(to_unsigned(d0, 4));
end process;
Process(time_diff, led_yellow, led_green, led_red) --difference level LEDs
BEGIN
IF time_diff=0 THEN
led_green<='1';
ELSE
led_green<='0';
END IF;
IF time_diff>0 AND time_diff<=3 THEN
led_yellow<='1';
ELSE
led_yellow<='0';
END IF;
IF time_diff>3 THEN
led_red<='1';
ELSE
led_red<='0';
END IF;
END PROCESS;
led_yellow_out<=led_yellow;
led_red_out<=led_red;
led_green_out<=led_green;
process(sign,t1,t2) -- sign of difference
begin
IF (t1>=t2) THEN
sign<='1';
ELSIF (t1<t2) THEN
sign<='0';
END IF;
IF sign='1' THEN
HEX3 <= "11111111";
```

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 8.021 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 7, July 2026
DOI: 10.17148/IJIREEICE.2026.14707

```
ELSE
HEX3 <= "10111111";
 end if;
end process;
digit2 <= digit2c;--first digit
digit1 <= digit1c;--second digit
digit0 <= digit0c;--third digit
WITH digit2 SELECT
HEX2 <= "11000000" WHEN "0000", -- display 0
"11111001" WHEN "0001", -- display 1
"10100100" WHEN "0010", -- display 2
"10110000" WHEN "0011", -- display 3
"10011001" WHEN "0100", -- display 4
"10010010" WHEN "0101", -- display 5
"10000011" WHEN "0110", -- display 6
"11111000" WHEN "0111", -- display 7
"10000000" WHEN "1000", -- display 8
"10011000" WHEN "1001", -- display 9
"11111111" WHEN OTHERS; -- blank display
WITH digit1 SELECT
HEX1 <= "01000000" WHEN "0000", -- display 0
"11111001" WHEN "0001", -- display 1
"10100100" WHEN "0010", -- display 2
"10110000" WHEN "0011", -- display 3
"10011001" WHEN "0100", -- display 4
"10010010" WHEN "0101", -- display 5
"10000011" WHEN "0110", -- display 6
"11111000" WHEN "0111", -- display 7
"10000000" WHEN "1000", -- display 8
"10011000" WHEN "1001", -- display 9
"11111111" WHEN OTHERS; -- blank display
WITH digit0 SELECT
HEX0 <= "11000000" WHEN "0000", -- display 0
"11111001" WHEN "0001", -- display 1
"10100100" WHEN "0010", -- display 2
"10110000" WHEN "0011", -- display 3
"10011001" WHEN "0100", -- display 4
"10010010" WHEN "0101", -- display 5
"10000011" WHEN "0110", -- display 6
"11111000" WHEN "0111", -- display 7
"10000000" WHEN "1000", -- display 8
"10011000" WHEN "1001", -- display 9
"11111111" WHEN OTHERS; -- blank display
end architecture;
```