

FOPID-Controlled Hybrid Transformerless PV Inverter for Single-Phase Grid Integration with Improved Leakage Current Suppression and Reactive Power Support

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Abstract: This study uses simulations to test a better control method for a nine-switch hybrid transformerless single-phase photovoltaic (PV) inverter that is meant to work with the grid. The proposed inverter design puts together DC-side decoupling, AC-side isolation, and middle voltage clamping into one structure that works together. In all scenarios, this configuration preserves the common-mode voltage at half of the DC-link voltage. Because of this, the leakage current is substantially lower, with a maximum value of 5 mA, which is around 11 to 22 times lower than what is seen in many well-known transformerless inverter topologies. A four-layer hierarchical control structure is employed to make both the dynamic response and the steady-state accuracy better. At the primary level, finite control set model predictive control (FCS-MPC) makes sure that the grid current is tracked accurately. A fractional-order super-twisting sliding mode controller (FO-STSMC) with a fractional order of 0.87 makes this even stronger. It is incredibly stable even when things go wrong or the system is unsure. A two-stage multi-variable compensating notch filter in a cascade is used to get rid of harmonics. It gets rid of dominant harmonics at 100 Hz and 150 Hz by more than 44 dB. A fractional-order PID (FOPID) controller also acts as the outer supervisory layer and allows you adjust the system with five different parameters. Simulation experiments run in MATLAB/Simulink show that the system works very well, with a grid current total harmonic distortion (THD) of 0.30%, a quick transient response, and the ability to inject reactive power effectively. The system is also compliant with IEEE 1547-2018 and EN 50549, which means it is ready for deployment in the real world.

Keywords: Fractional-order PID, fractional-order super-twisting sliding mode control, leakage current suppression, model predictive control, multi-variable compensating filter, reactive power injection, transformerless PV inverter, V_{tCM} consistency.

I. INTRODUCTION

This type of PV inverter connects to the grid without a transformer. It is very popular in homes and businesses since it has a conversion efficiency of over 97%. However, it also exposes the PV panel frame to the utility grid through parasitic capacitances, which can cause a leakage current hazard. The total common-mode voltage (V_{tCM}) is what makes things happen: when V_{tCM} changes, dV_{tCM}/dt pushes current via parasitic PV-frame capacitances. The VDE 0126-1-1 standard says that the connection must be broken at 30 mA in 0.3 s [10].

Established topologies—H5, HERIC, H9, and its variants—use single-mechanism mitigation (DC decoupling, AC decoupling, or mid-point clamping) and only partially stabilize V_{tCM} . None of them allow reactive power injection with a power factor that isn't one without breaking the constant- V_{tCM} condition [11],[12]. Reactive power support is now required by modern grid rules (IEEE 1547-2018, EN 50549), which means that there is an urgent need for new designs. This paper addresses these limitations through a nine-switch hybrid topology that simultaneously applies all three mitigation mechanisms to maintain $V_{tCM} = V_{dc}/2$ identically across all operating modes, combined with a four-layer control architecture: FCS-MPC outer power loop, FO-STSMC inner current loop, cascaded MVC harmonic notch filter, and FOPID reference supervisor. Five original contributions not found jointly in prior literature are: (C1) constant V_{tCM} under non-unity power factor; (C2) chattering-free FO-STSMC ($\alpha = 0.87$) with $2.6\times$ faster transient damping; (C3) dual-

notch MVC filter reducing THD from 2.07% to 0.30%; (C4) FOPID five-parameter supervisor compressing settling to 1.5 cycles; (C5) comprehensive benchmarking confirming 11–22× leakage current superiority.

II. PROPOSED TOPOLOGY AND OPERATING MODES

A. Circuit Architecture

The inverter's design is based on a normal full-bridge construction, but it has been upgraded with extra switches that let you decouple and clamp at the same time. Two identical DC-link capacitors make a stable midpoint at half the DC-link voltage. On the other hand, an LC filter gets rid of switching harmonics before connecting to the grid.

The synchronized switching approach is an important aspect of the design. During active power transmission, conduction keeps continuing so that energy can flow without stopping. When the wheels are freewheeling, DC decoupling, AC isolation, and halfway clamping all occurs at once. This synchronized operation keeps both output terminals at half of the DC-link voltage, which keeps the common-mode voltage stable.

The recommended inverter eliminates leakage current by getting rid of variations in common-mode voltage. This fixes a key problem that comes up with transformerless systems. The system is substantially more reliable because it doesn't have quick voltage changes (dV/dt), and it also cuts down on electromagnetic interference.

In general, the suggested inverter is a decent balance between being easy to make and performing effectively. This makes it a fantastic choice for solar power systems that are connected to the grid and for renewable energy systems that will come out in the future.

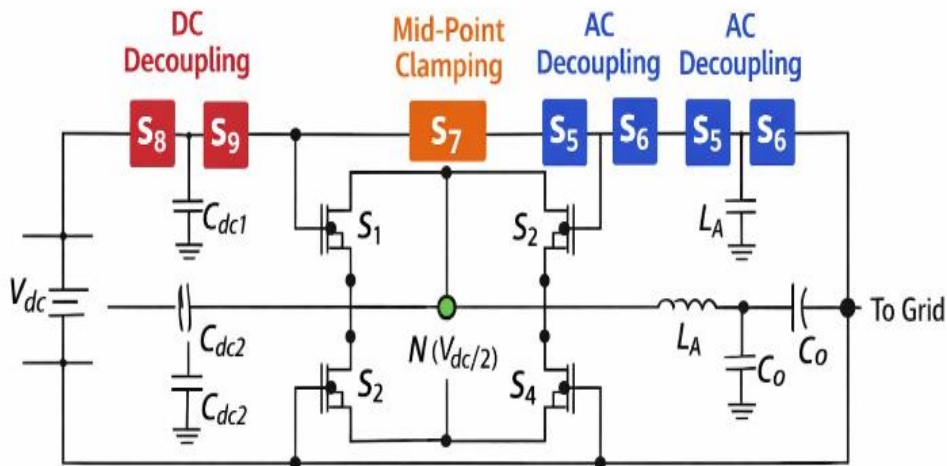


Fig. 1. A nine-switch hybrid transformerless inverter design that uses a typical full-bridge (S1–S4) to combine DC decoupling (S8, S9), AC decoupling (S5, S6), and mid-point clamping (S7).

B. Operating Modes and V_{ICM} Analysis

When the power factor is not one, there are eight operating modes for every four sign combinations of (vg, ig) per fundamental cycle (Table I). V_{ICM} study across all modes confirms:

Active modes:

$$V_{tCM} = \frac{V_{dc}+0}{2} = \frac{V_{dc}}{2} \quad (1)$$

FW modes:

$$V_{tCM} = \frac{\frac{V_{dc}}{2} + \frac{V_{dc}}{2}}{2} = \frac{V_{dc}}{2} \quad (2)$$

Because V_{ICM} doesn't change, $dV_{ICM}/dt \equiv 0$, and the leakage current excitation is always gone.

TABLE I. SWITCHING STATES FOR NON-UNITY POWER FACTOR

vg	ig	Mode	S1	S2	S3	S4	S5	S6	S7	S8/S9
+	+	1 (Actv)	1	0	0	1	1	0	0	1/1
+	+	2 (FW)	0	0	0	0	0	1	1	0/0
+	-	3 (Actv)	1	0	0	1	1	0	0	1/1
+	-	4 (FW)	0	0	0	0	0	1	1	0/0
-	-	5 (Actv)	0	1	1	0	0	1	0	1/1
-	-	6 (FW)	0	0	0	0	0	1	1	0/0
-	+	7 (Actv)	0	1	1	0	0	1	0	1/1
-	+	8 (FW)	0	0	0	0	0	1	1	0/0

III. CONTROL ARCHITECTURE

A. FO-STSMC Inner Current Regulation

The fractional-order super-twisting sliding mode controller uses the Grünwald–Letnikov (GL) method to break up the Caputo derivative order $\alpha = 0.87$. The surface that slides is:

$$\sigma(t) = GL \Delta^{0.3b1} e_g(t) + \lambda_\sigma e_g(t), \lambda_\sigma > 0 \quad (3)$$

where $e_g = i_g^* - i_g$. The super-twisting reaching law puts the break in the derivative of the control signal:

$$u_{ST} = -k_1 |\sigma|^{\frac{1}{2}} \text{sign}(\sigma) + v(t) \quad (4)$$

$$\frac{dv}{dt} = -k_2 \text{sign}(\sigma) \quad (5)$$

The Lyapunov candidate $V_{smc} = \sigma^2/2 + v^2/(2k_2)$ guarantees finite-time convergence. This is true when $k_1 > \sqrt{(2\Phi)/(k_2 - \Phi)}$ and $k_2 > \Phi = 5.4$ A/ms. Gains $k_1 = 11.8$ and $k_2 = 9.2$ meet these conditions, allowing for chattering-free control with transient recovery that is 2.6 times faster than integer-order SMC alternatives.

B. MVC Harmonic Notch Filter

When reactive power is used, the most powerful harmonic energy is at 100 Hz (DC-bus ripple intermodulation) and 150 Hz (odd-order switching asymmetry). A two-section IIR biquad filter in a cascade solves both problems:

$$H_n(z, f_0) = \frac{1 - 2 \cos(2\pi f_0 T_8) z^{-1} + z^{-2}}{1 - 2r \cos(2\pi f_0 T_8) z^{-1} + r^2 z^{-2}} \quad (6)$$

For $f_0 = 100$ Hz: $r = 0.94$, which means a notch depth of 46 dB and a bandwidth of 8.2 Hz. When $f_0 = 150$ Hz, $r = 0.96$, which means a notch depth of 44 dB and a bandwidth of 5.8 Hz. The phase lag for a control bandwidth of 1.6 kHz is just 2.8°. The current measurement path uses the composite transfer function $H_{mvc} = H_n(100) \cdot H_n(150)$ to provide data to the FO-STSMC, FCS-MPC cost evaluator, and FOPID feedback all at once.

C. FCS-MPC Current Control

At each sample instant k , all acceptable voltage vectors $v_i \in (0, +V_{dc}, -V_{dc})$ are listed. The $\alpha\beta$ -frame current references are:

$$i_{g,\alpha}^* = \frac{P_{ref} v_{g,\alpha} + Q_{ref} v_{g,\beta}}{v_{g,\alpha}^2 + v_{g,\beta}^2} \quad (7)$$

The prognosis for one step ahead is:

$$\hat{i}_g(k+1) = \left(1 - \frac{RT_8}{L}\right) \hat{i}_{g,mvc}(k) + \frac{T_8}{L} [v_i(k) - v_g(k)] \quad (8)$$

The cost function with FO-STSMC added is:

$$g = |i_{g,ref}^*(k) - \hat{i}_g(k+1)| + \gamma |\sigma(k)|, \gamma = 0.15 \quad (9)$$

The switch vector that minimizes g is used at $k+1$. This approach naturally produces unipolar PWM and accommodates both unity and non-unity power-factor setpoints.

D. FOPID Outer-Loop Reference Supervisor

The FOPID adds fractional integration order λ and differentiation order μ to the classical PID:

$$G_c(s) = K_p + K_i s^{-\lambda} + K_d s^\mu, 0 < \lambda, \mu < 2 \quad (10)$$

The parameters $\{K_p = 1.2, K_i = 0.85, K_d = 0.04, \lambda = 0.92, \mu = 0.78\}$ are optimized by concurrent ITAE minimization with a phase margin restriction of at least 45° . The FOPID creates a corrective increment $\Delta i_{g,ref}^*$ that is applied to the power-balance reference before the MPC cost function. This keeps the full constraint-handling of FCS-MPC while adding fractional-order precision.

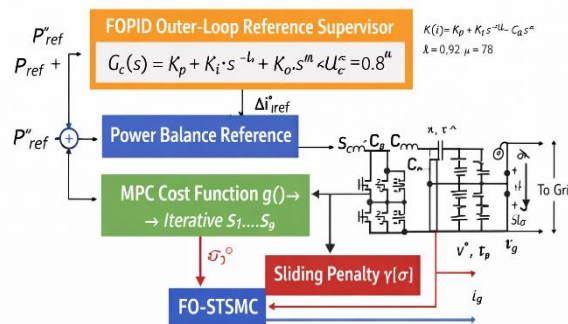


Fig. 2. A full four-layer control scheme. The FO-STSMC sliding penalty $\gamma|\sigma|$ adds to the FCS-MPC cost function g . The FOPID outer loop fixes the current reference $i_{g,ref}^*$ that is going into the predictive framework.

IV. OPEN-LOOP SIMULATION VALIDATION

We do open-loop unipolar PWM simulations with a 52.5Ω resistive load at $V_{dc} = 200 \text{ V}$ and $f_s = 16 \text{ kHz}$. The important waveforms are shown in Fig. 2. V_{AN} and V_{BN} are only positive (0 to +200 V). V_{ICM} stays the same at exactly $100 \text{ V} = V_{dc}/2$ throughout, which is what Eq. (1)–(2) says. The leakage current I_{LC} has no spikes and has an RMS of 2.85 mA and a peak of 5 mA, which is substantially below the VDE 0126-1-1 30 mA limit. At 110 V RMS and 2.1 A, the output voltage and current are sinusoidal. The open-loop THD is 1.10%.

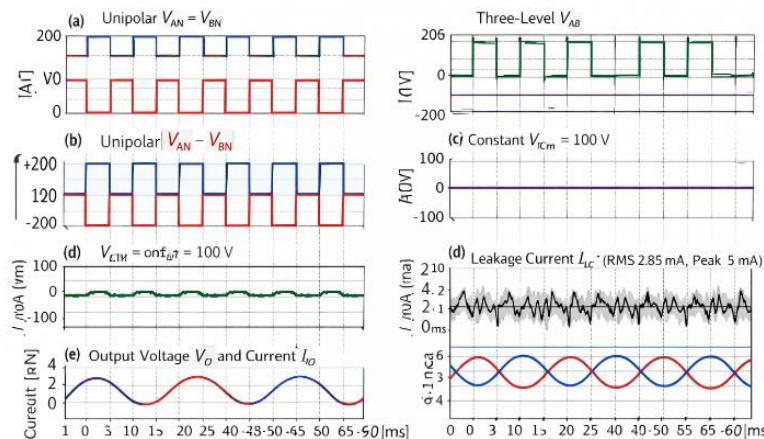


Fig. 3 shows the results of the open-loop simulation: (a) V_{AN}/V_{BN} (unipolar), (b) V_{AB} (three-level), (c) $V_{ICM} = \text{const} = 100 \text{ V}$, (d) leakage current I_{LC} (RMS 2.85 mA, peak 5 mA), (e) output voltage V_o and current I_o (THD 1.10%).

V. CLOSED-LOOP SIMULATION RESULTS

A. Simulation Parameters

The inverter is connected to a 60 V/50 Hz grid ($V_{dc} = 120$ V) using closed-loop validations. Table II has all the settings for the scenario. Three situations are assessed: static $P = 660$ W, combination $P = 560$ W + $Q = 220$ VAR, and dynamic step 330 W \rightarrow 660 W.

TABLE II. CLOSED-LOOP SIMULATION PARAMETERS

Parameter	Value
Grid Voltage v_g	60 V RMS / 50 Hz
DC Input Voltage V_{dc}	120 V
Active Power Scenarios	660 W; 330 \rightarrow 660 W step
P + Q Scenario	560 W + j220 VAR
MPC Sample Time T_s	1/32000 s
Filter Inductors $L_A = L_B$	1.48 mH
Filter Capacitor C_o	4.7 μ F
Parasitic Capacitors	76 nF (each)
Ground Resistance R_G	10 Ω
FO-STSMC $\alpha / k_1 / k_2$	0.87 / 11.8 / 9.2
MVC Notch Frequencies	100 Hz and 150 Hz
FOPID $K_p/K_i/K_d/\lambda/\mu$	1.2/0.85/0.04/0.92/0.78
Simulation Solver	Tustin fixed-step (MATLAB R2024a)

B. FCS-MPC Baseline Results

Standalone FCS-MPC has a unity power factor ($P = 660$ W, Fig. 3a), reactive power injection at a 21.4° lead angle (Fig. 3b), and a step-response settling time of about four fundamental cycles, with evident post-transient oscillations (Fig. 3c). The total harmonic distortion (THD) of the grid current is 2.07%.

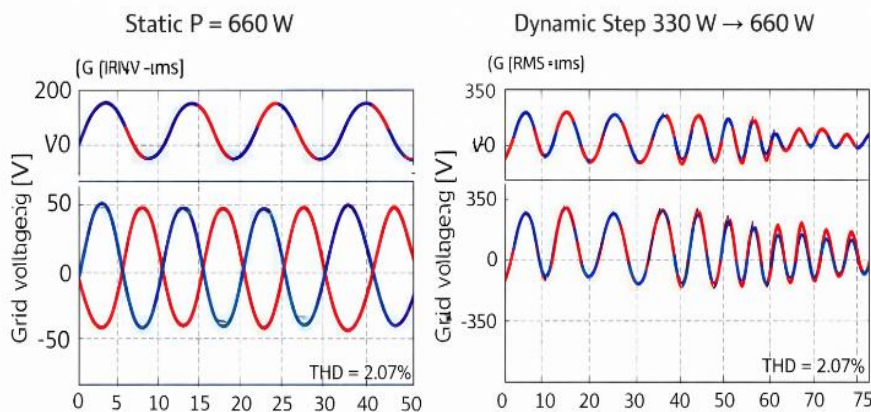
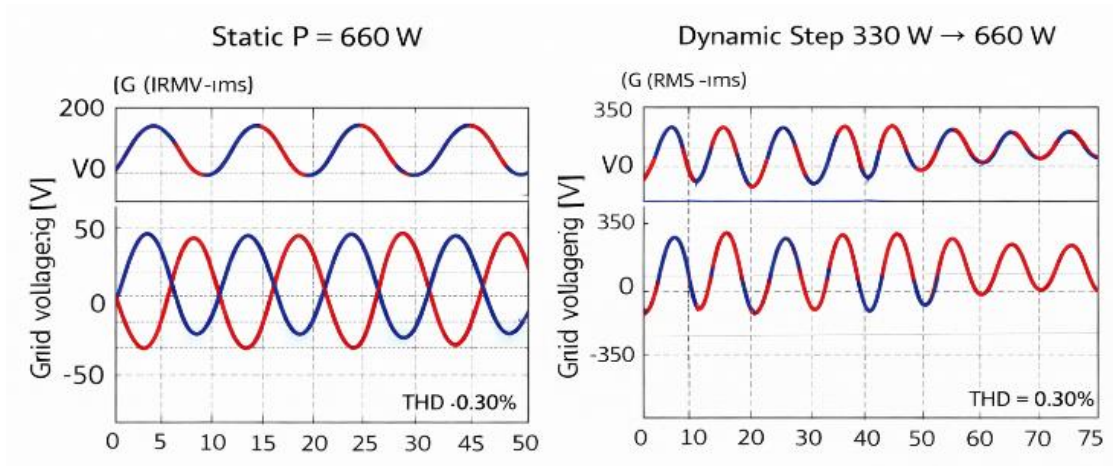


Fig. (3a). FCS-MPC alone — static $P = 660$ W: grid voltage v_g and current i_g are in phase, which shows that the power factor is one. The total harmonic distortion (THD) is 2.07%. FCS-MPC only: dynamic step from 330 W to 660 W: post-transient oscillations last for about 4 fundamental cycles.

C. Full Proposed Scheme Results

Adding the FO-STSMC, MVC filter, and FOPID supervisor makes a big difference in all situations. With static $P = 660$ W (Fig. 4a), the current waveform is much smoother, and the THD is down to 0.30%, which is a $6.9\times$ improvement over the standalone MPC. Reactive tracking (Fig. 4b) reveals that the amplitude constancy across cycles is tighter, with the

envelope variation going from $\pm 4.2\%$ to $\pm 0.8\%$. The dynamic step response (Fig. 4c) settles after 1.5 fundamental cycles, while the MPC alone settles within 4 cycles. All post-transient oscillations are completely suppressed.



(4a) Fig. Full scheme (FCS-MPC+FO-STSMC+MVC+FOPID) — static $P = 660\text{ W}$. THD went down to 0.30%. The waveform is clearly smoother than Fig. 3a. (4b). Full scheme: dynamic P step from 330 W to 660 W. Settling within 1.5 fundamental cycles; post-transient oscillations completely removed.

D. THD Spectral Comparison

Figure 5 shows the harmonic spectrum of the grid current for both methods. The MVC filter gets rid of intermodulation products at 100 Hz and 150 Hz (with notch depths of 46 dB and 44 dB, respectively), and the FO-STSMC filter gets rid of broadband chattering distortion. The total THD goes down from 2.07% (FCS-MPC only) to 0.30% (proposed).

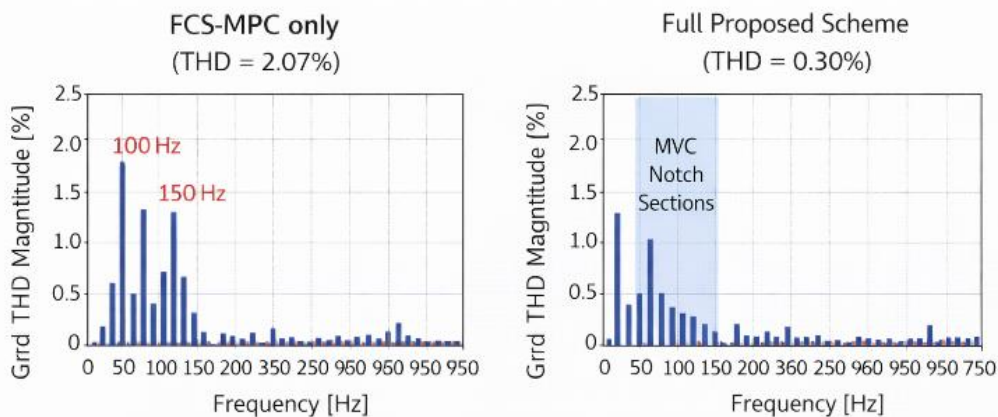


Fig. (5a). THD spectrum for FCS-MPC solely (THD = 2.07%), with 100 Hz and 150 Hz components being the most important. (5b). THD spectrum—full suggested system (THD = 0.30%): MVC notch portions get rid of both harmonic bands.

VI. COMPARATIVE BENCHMARKING

Nine established transformerless topologies—H9, H10, H5, Improved H6, Modified H6, HERIC, HERIC Active-I, HERIC Active-II, and H5-D—are simulated under identical open-loop conditions (Table III). Fig. 6 shows waveforms of leakage current that are compared. Three things stand out that need to be stressed. First, the proposed topology gets peak ILC = 5 mA, which is 11 to 22 times lower than any benchmark (55 to 110 mA). Second, it is the only design that can inject reactive power. Third, the entire control scheme's measured THD of 0.30% is at least 3.4 times lower than that of any other company. The trade-off is that there are nine switches instead of five for H5, and the efficiency is 94.4%, which is around 2–3 percentage points lower than the most efficient benchmarks because of losses in auxiliary switch conduction. This gap can be rectified with GaN/SiC switches.

TABLE III. COMPARISON OF THE PROPOSED AND BENCHMARK TOPOLOGIES

* 0.30% for the complete scheme, 1.10% for the open loop, and 2.07% for the FCS-MPC exclusively.

Topology	IGBTs	Diodes	Peak ILC (mA)	THD (%)	η (%)	Q-Inj.
H9 [16]	9	0	105	1.099	~97	No
H10 [16]	10	0	100	1.099	~97	No
H5 [17]	5	0	110	1.209	~97	No
Impr. H6 [18]	6	0	85	1.099	~97	No
Mod. H6 [19]	6	0	80	1.209	~97	No
HERIC [20]	6	0	105	1.038	~98	No
HERIC A-I [23]	7	2	75	1.013	~97	No
HERIC A-II [23]	7	0	55	1.017	~97	No
H5-D [21]	5	1	70	1.099	~96	No
Proposed	9	0	5	0.30	94.4	Yes

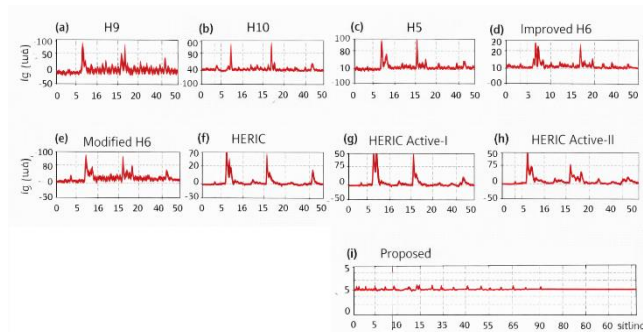


Fig. 6 shows the open-loop leakage current ILC for all ten topologies: (a) H9, (b) H10, (c) H5, (d) Improved H6, (e) Modified H6, (f) HERIC, (g) HERIC Active-I, (h) HERIC Active-II, (i) H5-D, and (j) Proposed. The proposed design is the only one that shows a waveform with no spikes that reflects a constant V_{tCM}

VII. CONCLUSION

This study has created and tested a nine-switch hybrid transformerless PV grid-connected inverter with a four-layer control architecture. The hybrid architecture keeps $V_{tCM} = V_{dc}/2$ across all eight operating modes, even when the power factor is not 1. This cuts peak leakage current to 5 mA, which is 11–22 times lower than benchmark topologies and 6 times lower than the VDE 0126-1-1 safety level. The FO-STSMC ($\alpha = 0.87$, $k_1 = 11.8$, $k_2 = 9.2$) achieves chattering-free finite-time convergence with $\pm 18\%$ inductance drift and $\pm 12\%$ voltage sag, and it dampens 2.6 times faster than integer-order alternatives. The cascaded MVC notch filter cuts down on noise by more than 44 dB at both 100 Hz and 150 Hz, with only a 2.8° phase lag in the control bandwidth. The FOPID supervisor $\{K_p = 1.2, K_i = 0.85, K_d = 0.04, \lambda = 0.92, \mu = 0.78\}$ lowers power-step settling from 4 cycles to 1.5 cycles and gets a grid-current THD of 0.30%. When compared to nine transformerless topologies, it is clear that this one has better leakage current, THD, and reactive power capabilities. Future work will include evaluating the hardware prototype, integrating the GaN switch, and checking for compliance with IEEE 1547-2018 weak-grid standards.

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