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Advances in VLSI and Embedded Systems: FPGA-Based Design, Low-Power Microcontrollers, and Nanowire Growth Technologies A-Review

Nitesh Kumar Vashisht

B.Tech in Electronics and Communication Engineering (ECE), Shoolini University

Abstract: Very-large-scale integration (VLSI) and embedded systems are moving toward heterogeneous designs where speed, energy efficiency, flexibility, and device innovation must work together. This review discusses three important areas: FPGA-based system design, low-power microcontrollers, and semiconductor nanowire growth. FPGAs are valuable for rapid prototyping, parallel processing, hardware acceleration, and hardware/software co-design. Low-power microcontrollers support battery-operated sensing, wireless embedded platforms, TinyML, and always-on edge intelligence. Nanowire growth offers possibilities for future transistor channels, sensitive sensors, and post-planar nanoelectronics devices. The review shows that these topics are often studied separately, although future embedded platforms will need closer cooperation between reconfigurable hardware, efficient control units, and emerging nanoscale devices. FPGAs can provide strong acceleration but may consume more power. Microcontrollers are energy efficient but limited in memory and throughput. Nanowire devices are promising but still face integration and manufacturing challenges. The paper identifies the need for cross-layer co-design methods that connect architecture, firmware, security, power modelling, and device technology for practical future VLSI systems in IoT, healthcare, instrumentation, and edge computing.

Keywords: VLSI; FPGA-Based Design; Low-Power Microcontrollers; Nanowire Electronics

1. INTRODUCTION

Very-large-scale integration (VLSI) and embedded systems continue to shape the development of modern electronic products. Almost every intelligent device, from a simple sensor node to a medical monitoring system or an edge-AI platform, depends on compact electronic hardware that can process information quickly while using limited power. In earlier design approaches, high performance, low power, and device scaling were often treated as separate goals. Today, that separation is becoming less practical because modern embedded systems need all these qualities at the same time.

In this context, three areas are especially important. The first is FPGA-based system design. Field-programmable gate arrays provide reconfigurable logic, parallel processing, fast prototyping, and the ability to create custom hardware accelerators. They are used in signal processing, communication systems, machine learning, instrumentation, healthcare electronics, and many other embedded applications **[1]**, **[5]**. The second area is low-power microcontroller design. Microcontrollers are the foundation of many IoT and portable systems because they combine processing, memory, peripherals, and power-management features in a small and low-cost device **[19]**,**[23]**. The third area is nanowire growth, which is important for future VLSI because nanowires can support new transistor structures, sensitive sensors, and nanoscale electronic devices **[41]**,**[45]**.

Although these areas are connected, they are often studied in separate research communities. FPGA research mainly focuses on acceleration and reconfigurable computing. Microcontroller research gives more attention to energy saving, embedded software, wireless communication, and TinyML. Nanowire research is mostly concerned with growth methods, material properties, and device behaviour. This separation creates a clear research gap because future VLSI and embedded systems are likely to be heterogeneous. They may need nanowire-based sensors, microcontroller-based low-power control, and FPGA-based acceleration in one practical design.

This review therefore brings these three areas together. It discusses their basic concepts, reviews major research trends, compares their strengths and limitations, identifies research gaps, and proposes a future co-design direction. The main argument of this paper is that progress in VLSI and embedded systems will depend not only on improving individual technologies, but also on building stronger links between device technology, architecture, firmware, security, and application-level requirements.

2. BACKGROUND AND CONCEPTUAL FOUNDATIONS

2.1 FPGA-Based System Design

An FPGA is a programmable hardware device comprising of configurable logic blocks, routing resources, memory blocks, digital signal processing, and interface to peripheral devices. Most of today's FPGAs also have built-in processor cores and blocks supporting fast communication. The key characteristic of FPGAs is the fact that their hardware configuration is modifiable after fabrication, which makes them particularly useful in rapid prototyping, designing novel digital structures and implementing custom accelerators without going through the application specific IC fabrication process **[2], [5], [17].**

FPGAs are appropriate in the design of embedded systems, where parallelism, deterministic timing, specific interface, and/or fast data transfer is needed. Typically, FPGA development involves the use of hardware description languages like Verilog and VHDL. But today FPGA development can be achieved even using high-level synthesis, where the designer describes the algorithm in a high-level programming language and gets its automatic conversion into hardware **[2],[4].** That said, proper FPGA design is not a trivial exercise, and it demands thorough consideration of many issues, from memory access to timing and power management.

2.2 Low-Power Microcontrollers

A microcontroller is a small-sized and highly integrated system, which contains a processing unit, storage devices, timers, communication ports, both analog and digital peripheral components, and power regulation capabilities. Low-power microcontrollers have found widespread adoption in IoT nodes, wearables, smart metering, portable medical instruments, environmental sensing, and factory automation applications. The significance of low-power microcontrollers lies in their capability of completing relevant control and computation operations using minimum energy levels **[19],[22].**

Low-power embedded systems cannot be viewed only in terms of hardware design. Other aspects such as firmware architecture, sleep/standby states, wake-up conditions, duty cycling, interrupt processing, wireless communication, and energy-aware scheduling become relevant too. Moreover, dynamic voltage and frequency scaling may be utilized for decreasing the energy footprint in variable load scenarios **[23].** In recent times, TinyML has broadened the scope of microcontrollers by allowing tiny machine learning algorithms to be executed on resource-constrained hardware platforms **[24],[32].**

2.3 Nanowire Growth and Nanoelectronics Devices

Nanowires are nanoscale structures with very small diameters and high length-to-width ratios. Their small dimensions give them electrical, optical, and sensing properties that can be different from bulk materials. In VLSI research, nanowires are important because they may support new field-effect transistor channels, highly sensitive sensors, quantum devices, and future nanoelectronics systems **[41]**, **[42]**, **[53]**.

Nanowires can be grown using different methods, including vapor-liquid-solid growth, catalyst-assisted growth, catalyst-free growth, selective-area growth, and patterned growth techniques **[43]**, **[45]**, **[49]**, **[51]**. Silicon nanowires, III-V nanowires, zinc oxide nanowires, gallium nitride nanowires, and chalcogenide nanowires have all been investigated for electronic and sensing applications **[47],[55]**. However, the practical use of nanowires in mainstream VLSI still faces challenges such as reproducibility, contamination, interface quality, packaging, and compatibility with existing CMOS manufacturing.

2.4 Relationship Between the Three Technology Layers

The three technologies discussed in this review operate at different levels of design. Nanowires belong mainly to the device and material level. Microcontrollers belong to the embedded architecture and firmware level. FPGAs belong to the system-implementation and hardware-acceleration level. A future intelligent embedded platform may combine all three. For example, a nanowire sensor may collect highly sensitive physical information, a microcontroller may manage low-power control and communication, and an FPGA may accelerate signal processing or machine-learning inference. This layered relationship is the reason a cross-domain review is useful.

3. REVIEW METHOD AND SCOPE

This paper uses a narrative review method. Instead of presenting a statistical meta-analysis, it organizes the literature into major themes and compares the design contributions of each theme. The review focuses on FPGA-based system design, low-power microcontroller platforms, nanowire growth, and the possible convergence of these technologies in future VLSI and embedded systems.

The FPGA section considers high-level synthesis, dynamic reconfiguration, neural-network acceleration, system-on-chip design, healthcare applications, measurement systems, and cybersecurity. The microcontroller section considers energy-efficient design, wireless communication, sleep-state management, dynamic voltage and frequency scaling, TinyML frameworks, and benchmarking. The nanowire section considers growth mechanisms, semiconductor materials, transistor applications, sensing applications, transport behaviour, and integration challenges.

The scope of the paper is intentionally interdisciplinary. VLSI and embedded systems are not limited to one layer of design. A practical product involves device technology, circuit design, architecture, firmware, software tools, communication, security, and application requirements. Therefore, this review evaluates the selected literature from a system-design perspective and identifies where stronger connections are needed between these layers.

4. LITERATURE REVIEW AND THEMATIC SYNTHESIS

4.1 FPGA-Based System Design in Contemporary VLSI Practice

The FPGA literature shows that reconfigurable hardware has moved beyond simple prototyping. FPGAs are now used in real applications where fast development, parallelism, and customized processing are needed. High-level synthesis is one of the main reasons for this progress. Cong et al. **[2]** explained how HLS supports the movement from prototyping to deployment. Molina et al. **[3]** reviewed HLS models, methodologies, and frameworks for FPGA accelerators. Lahti and Hämäläinen **[4]** also showed that HLS improves design productivity, although hardware knowledge remains important for achieving efficient results.

Another important topic is dynamic and partial reconfiguration. Vipin and Fahmy **[5]** reviewed methods and applications that allow selected parts of an FPGA to be changed during operation. This is useful in embedded systems where the same hardware may need to perform different tasks at different times, such as sensing, encryption, signal processing, and inference. Instead of building separate hardware for every function, the system can reuse logic resources more efficiently.

FPGA-based machine-learning acceleration is a very active research area. Guo et al. **[9]**, Wu et al. **[10]**, and Yan et al. **[11]** reviewed FPGA accelerators for neural-network inference and machine-learning workloads. These studies show that FPGAs can be effective for quantized, sparse, and latency-sensitive models because designers can customize data paths, memory use, and numeric precision. However, the same studies also show that FPGA programming can be complex and that portability between devices and vendors remains a challenge.

Application-specific FPGA studies also show the practical value of reconfigurable hardware. Saidi et al. **[7]** discussed soft-core embedded FPGA system-on-chip design. Suresh et al. **[8]** examined FPGA use in low-power vision systems. Aridhi et al. **[12]** reviewed FPGA technology in healthcare electronics. Galaviz-Aguilar et al. **[13]** reviewed FPGA-based lock-in amplifier systems for advanced measurement applications. These examples show that FPGAs are strong when a system needs custom timing, specialized interfaces, or fast parallel processing.

Despite these strengths, FPGA systems also have limitations. They often require specialized knowledge, vendor-specific tools, careful timing closure, and power-aware design. Security must also be considered because bitstreams, hardware intellectual property, and update processes can be attacked. Proulx et al. **[6]** reviewed FPGA cybersecurity strategies and showed that secure FPGA deployment requires protection at both hardware and design-flow levels.

4.2 Low-Power Microcontrollers and Always-On Embedded Intelligence

Low-power microcontrollers are the practical foundation of many embedded and IoT systems. They are not designed to provide the same throughput as FPGAs, but they are very effective for control, sensing, communication, and low-duty-cycle computation. Al-Kofahi et al. **[19]** discussed energy-efficient microcontrollers and IoT systems. Wisniewski et al. **[20]** reviewed hardware solutions for low-power smart edge computing, while Barge and Gerardine **[22]** examined low-power techniques for IoT implementation.

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Wireless communication is a major source of energy consumption in embedded systems. Baker et al. **[21]** reviewed short-range wireless communication for ultra-low-power embedded platforms and showed that protocol choice, transmission distance, duty cycle, latency, and wake-up behaviour strongly affect energy use. This means that a low-power microcontroller must be supported by an energy-aware communication strategy.

Dynamic voltage and frequency scaling is another important method for saving energy. Zidar et al. **[23]** showed that DVFS can reduce energy consumption in ultra-low-power embedded systems when workloads vary. However, DVFS is not always automatically beneficial. The system must consider whether the energy saved is greater than the overhead caused by changing voltage and frequency states.

TinyML has made microcontrollers more important in intelligent edge systems. Rajapakse et al. **[24]** reviewed reformable TinyML, and Saha et al. **[25]** reviewed machine learning for microcontroller-class hardware. Ramos-Sanchez et al. **[26]** and Kallimani et al. **[27]** discussed TinyML tools, applications, challenges, and future research directions. These works show that microcontrollers can now support local inference for sensor data, health monitoring, audio detection, vibration analysis, and simple vision tasks.

Several tools have helped TinyML become practical. TensorFlow Lite Micro supports machine learning on tiny embedded systems **[28]**. CMSIS-NN provides optimized neural-network kernels for Arm Cortex-M processors **[29]**. MCUNet and MCUNetV2 show how neural networks can be co-designed with small hardware platforms **[30]**, **[31]**. MLPerf Tiny provides a benchmark for comparing tiny machine-learning systems **[32]**. More recent work on TinyTrain and micro-NPU benchmarking suggests that the field is moving toward better evaluation and more capable low-power intelligence **[33]**, **[34]**.

The main limitation of microcontrollers is that they are constrained by memory, clock speed, and processing throughput. They are excellent for always-on sensing and lightweight intelligence, but they cannot efficiently handle every workload. This is why future systems may combine microcontrollers with FPGA accelerators or specialized devices.

4.3 Nanowire Growth and Nanoelectronics Device Opportunities

Nanowire research looks at VLSI progress from the device and material side. Schmidt et al. **[41]** reviewed growth, thermodynamics, and electrical properties of silicon nanowires. Dasgupta et al. **[42]** reviewed semiconductor nanowire synthesis, characterization, and applications. Dick **[43]** discussed nanowire growth promoted by alloys and non-alloying elements, especially in III-V nanowire systems. Ramanujam et al. **[44]** reviewed silicon nanowire growth and properties.

A key concern in nanowire research is practical integration. McIntyre and Fontcuberta i Morral **[45]** discussed the important question of when semiconductor nanowires should be grown and when other device solutions may be more practical. This question matters because VLSI manufacturing requires reproducibility, compatibility, stable interfaces, and contamination control. A nanowire device may perform well in a laboratory, but it must also be manufacturable and reliable before it can become part of a mainstream embedded system.

Nanowires are promising for sensing, energy, and transistor applications. Hsu et al. **[46]** reviewed nanowire properties and applications. Consonni et al. **[47]** discussed zinc oxide nanowires for energy-related applications. Leshchenko and Sibirev **[48]** reviewed III-V nanowire heterostructures. Yang et al. **[49]** studied patterned metal chalcogenide nanowires, and Olšteins et al. **[50]** demonstrated cryogenic multiplexing using selective-area-grown semiconducting nanowires.

Catalyst-free growth is an important direction because it may reduce contamination concerns. Gao et al. **[51]** reported catalyst-free synthesis of sub-5 nm silicon nanowire arrays. Bertness et al. **[55]** studied catalyst-free GaN nanowire growth. Wu et al. **[52]** reported silicon nanowire channels for high-performance field-effect transistors, showing that nanowire geometry can influence transistor behaviour. Badawy and Bakkers **[53]** reviewed transport and quantum phenomena in nanowires, while Akbari-Saatlu et al. **[54]** reviewed silicon nanowires for gas sensing.

The main challenge is that nanowire research is still not fully connected to embedded-system design. Device researchers often focus on growth, structure, and transport properties. Embedded designers focus on interfaces, firmware, power states, security, and deployment. A stronger bridge between these viewpoints is needed if nanowires are to become part of practical VLSI and embedded platforms.

4.4 Cross-Domain Convergence

When the three areas are considered together, a clear future direction becomes visible. FPGAs are suitable for acceleration and hardware flexibility. Microcontrollers are suitable for low-power control and always-on operation. Nanowires are suitable for advanced sensing and device innovation. A future embedded system may combine a nanowire sensor, a low-power microcontroller, and an FPGA accelerator in one complete architecture.

However, this type of full-stack design is still not mature in the literature. FPGA studies often assume conventional digital input sources. Microcontroller studies often focus on conventional sensors and standard silicon platforms. Nanowire studies often stop at device-level demonstration. Future research needs to connect these levels so that new device technologies can be evaluated not only as materials achievements but also as practical system components.

5. COMPARISON AND ANALYSIS OF PREVIOUS WORKS

The reviewed literature can be divided into four major categories. Each category contributes something important to VLSI and embedded-system design, but each also has limitations.

Category	**Representative Literature**	**Main Strengths**	**Main Limitations**
FPGA-based system design	Cong et al. **[2]**; Molina et al. **[3]**; Vipin and Fahmy **[5]**; Guo et al. **[9]**	Reconfigurable hardware, parallel acceleration, rapid prototyping, hardware/software co-design, deterministic timing	Higher design complexity, vendor dependence, power overhead, portability issues, and security concerns
Low-power microcontrollers	Al-Kofahi et al. **[19]**; Baker et al. **[21]**; Zidar et al. **[23]**; Saha et al. **[25]**	Very low energy use, mature embedded ecosystems, strong fit for IoT, TinyML, sensing, and supervisory control	Limited memory, limited throughput, restricted support for large AI models, and communication-energy challenges
Nanowire growth and devices	Schmidt et al. **[41]**; McIntyre and Fontcuberta i Morral **[45]**; Wu et al. **[52]**; Badawy and Bakkers **[53]**	New device geometries, high sensitivity, improved electrostatic control, and potential for future transistors and sensors	Fabrication variability, integration difficulty, contamination concerns, packaging challenges, and weak link to embedded toolchains
Cross-domain heterogeneous systems	Emerging research direction	Potential to combine ultra-low-power control, reconfigurable acceleration, and advanced sensing	Lack of unified benchmarks, limited CAD support, fragmented evaluation, and insufficient real deployment evidence

Table 1. This tables shows the comparison and Analysis of Previous Works

The comparison shows that the strongest future direction is not to choose one technology over the others. Instead, future systems should combine the right technology for the right task. FPGAs can handle demanding acceleration tasks, microcontrollers can manage energy-efficient control, and nanowire devices can improve sensing or device-level performance. This combination is more realistic than expecting one platform to solve every design challenge.

6. RESEARCH GAP AND PROBLEM IDENTIFICATION

6.1 Methodological Fragmentation

The first major gap is fragmentation between research communities. FPGA studies focus on acceleration and reconfiguration. Microcontroller studies focus on energy efficiency and embedded intelligence. Nanowire studies focus on material growth and device behaviour. Very few studies connect these areas into a single design method that begins at the device level and ends with a deployable embedded system.

6.2 Lack of Unified Power-Performance Models

A second gap is the lack of unified power-performance models. Designers need better ways to decide whether a task should run on a microcontroller, an FPGA, or a specialized nanowire-enabled front end. Most existing comparisons are

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made within one technology group. Future systems require cross-platform evaluation that includes energy per task, latency, memory use, throughput, reliability, security, and implementation cost.

6.3 Weak Toolchain Integration

The third gap is weak toolchain integration. FPGA design tools, TinyML runtimes, embedded firmware tools, and nanowire fabrication workflows are usually developed separately. As a result, system-level co-design becomes difficult and often depends on manual effort. A stronger design flow should connect device parameters, circuit behaviour, workload partitioning, firmware design, acceleration, and security.

6.4 Limited Implementation Realism

Many nanowire studies demonstrate useful device characteristics but do not fully address packaging, manufacturability, CMOS compatibility, testing, or long-term stability. On the other hand, many embedded-system studies assume conventional devices and do not consider how emerging nanoscale sensors or transistors could change the design. More real implementation studies are needed to connect these two sides.

6.5 Security and Lifecycle Maintainability

Security and maintainability are also important gaps. FPGA systems need secure bitstreams and trusted update mechanisms. Microcontroller systems need secure boot, protected firmware, and reliable communication. Nanowire-enabled devices need stable interfaces and fault monitoring. Heterogeneous systems that combine these technologies must include lifecycle telemetry, authenticated updates, fault diagnosis, and hardware-aware security from the beginning **[6]**.

7. PROPOSED FRAMEWORK AND FUTURE SCOPE

7.1 Heterogeneous Co-Design Framework

A useful future direction is a heterogeneous co-design framework. In this framework, FPGAs, microcontrollers, and nanowire technologies are treated as complementary layers. The microcontroller works as the always-on supervisory unit. It manages wake-up control, energy accounting, sensor scheduling, communication, secure control, and lightweight inference. The FPGA works as an on-demand accelerator for workloads such as signal processing, cryptography, image processing, or machine-learning inference. Nanowire-enabled components work as advanced sensors, specialized transistor channels, or future nanoelectronics front ends.

7.2 Application-Level Requirement Definition

The design process should begin by defining application requirements. These requirements should include latency, energy per task, memory budget, accuracy target, reliability target, security policy, update method, communication cost, and manufacturing constraints. Once these requirements are clear, designers can decide which part of the system should run on the microcontroller, which part should be accelerated on the FPGA, and where nanowire devices may provide real benefit.

7.3 Power-Aware Workload Partitioning

Future systems should evaluate the full energy path. This includes sensing, signal conditioning, data movement, preprocessing, inference, encryption, storage, wireless transmission, sleep-state transitions, and firmware updates. Looking at only one part of the system can give a misleading view of energy efficiency. In many embedded systems, communication and wake-up overhead may consume more energy than computation **[21]**, **[23]**.

7.4 Benchmarking and Standardization

Benchmarking is necessary for fair evaluation. TinyML has already made progress through tools such as TensorFlow Lite Micro and MLPerf Tiny **[28]**, **[32]**. FPGA research would benefit from benchmarks that report energy, latency, throughput, portability, security, design effort, and update cost. Nanowire research would benefit from benchmarks that connect growth quality and device properties to circuit-level and system-level effects.

7.5 Manufacturability and Trust

Manufacturability and trust should be considered early. For FPGA and microcontroller systems, this includes secure boot, authenticated firmware updates, hardware monitoring, and safe lifecycle management. For nanowire-enabled systems, this includes reproducible growth, contamination control, stable interfaces, packaging compatibility, and possible CMOS integration **[45]**, **[52]**, **[53]**.

7.6 Future Research Directions

Future research should focus on five areas. First, cross-layer CAD tools should be developed to connect device models, circuit behaviour, hardware acceleration, firmware, and system-level energy analysis. Second, heterogeneous edge platforms should combine microcontroller control with FPGA acceleration. Third, nanowire sensors should be tested with practical embedded interfaces under real operating conditions. Fourth, standardized power-performance benchmarks should compare microcontrollers, FPGAs, and emerging devices fairly. Fifth, security and lifecycle maintainability should be included in all future VLSI and embedded-system designs.

8. CONCLUSION

The review of VLSI and embedded systems took place through three interrelated areas, namely FPGA-based system design, low-power microcontrollers, and nanowire growth. It appears from literature that every one of the above-listed domains plays its own role, and these roles are described in more detail below. Specifically, FPGAs bring flexibility, parallel computation, fast prototyping, and hardware acceleration, whereas low-power microcontrollers offer efficient control, sensing, communications, and TinyML support.

Thus, the key lesson from the analysis is that none of these areas seems to be integrated deeply enough yet. FPGA and microcontroller studies tend to get close to deployable embedded systems, but nanowire-related work may stay in the domain of materials science and device engineering. Nonetheless, it is expected that in the future, the combination of all those technologies will be critical for VLSI and embedded platforms.

Hence, what needs to be done to make the discussed combination possible is the improvement of integration across different layers. Such aspects as the connection between the device technology, architecture, firmware, tools, benchmarks, and security need to be enhanced. In case these challenges are met, the combination of reconfigurable logic, ultra-low-power microcontrollers, and nanowires will enable the next-gen embedded systems.

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