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# Physical Design of NMOS Full Adder using Pass Transistor Logic (PTL)

**Vishwas V[1], Moulya L[2], Poorvitha D[3], Ayush Ojha[4]**

Student, ECE, SJBIT, Bengaluru, India[1]

Student, ECE, SJBIT, Bengaluru, India[2]

Student, ECE, SJBIT, Bengaluru, India[3]

Student, ECE, SJBIT, Bengaluru, India[4]

**Abstract**: This project presents an NMOS-based Full Adder designed using Pass Transistor Logic to achieve low power, high speed, and compact layout. The design was implemented in Cadence Virtuoso at the 180 nm technology node to minimize the number of transistors and area compared to standard CMOS adders. A restoration circuit ensures full logic levels for reliable performance. Simulation results confirm the improvement in efficiency and make the design suitable for low-power VLSI and embedded applications.

**Keywords**: NMOS, Pass Transistor Logic, Full Adder, Low Power VLSI, Cadence Virtuoso, CMOS, Integrated Circuit Design.

## I. INTRODUCTION

Efficiency in arithmetic design plays a vital role in enhancing the speed and power performances of modern VLSI systems. Standard adders, using traditional CMOS logic, may occupy a greater area and hence dissipate more power, being unsuitable for compact and low-power applications. Herein, a Full Adder using NMOS-based Pass Transistor Logic is designed and presents a reduced transistor count with faster operation. Therefore, the proposed design will improve the performance with optimized power and silicon area, thereby proving to be the most suitable for embedded and portable VLSI systems.

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## II. LITERATURE SURVEY

### 1. 6 Transistor Full Adder Circuit Using Pass Transistor Logic

**Authors: -** S. Selvi and S. Pradeep
**Published by -** Journal of Chemical and Pharmaceutical Sciences, 2017

This design presents a 6-transistor PTL full adder that achieves reduced power and area utilization. The approach simplifies the circuit using only a minimum number of transistors, thus proving effective for compact and energy-efficient VLSI applications.

### 2. A Low Power Efficient Design of Full Adder Using Transmission Gates

**Authors: -** P. A. Pandian, K. Sakthivel, K. S. Alavudeen, R. L. Priya
**Published by -** International Journal of Communication and Computer Technology, Vol. 5, No. 1, May 2023

The study proves that the design based on the transmission gate architecture ensures full voltage swing and reduced delay, hence low power consumption suitable for power-sensitive VLSI systems.

### 3. Low Power Full Adder Implementation Based on Pass Transistor Technology

**Authors: -** Kiruthiga, G. Abirami, T. Gowsalya, K. Kanimozhi
**Published by -** International Journal of Advanced Engineering Research and Science, Vol. 3, No. 3, Mar. 2016

The paper combines CMOS and PTL logic to reduce transistor count and area. The hybrid approach improves the energy efficiency while maintaining signal stability in low-power circuits.

  

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**4. An Energy-Efficient Full-Adder Design Using Pass-Transistor Logic**

**Authors: -** B. C. Devnath and S. N. Biswas
**Published by -** Proceedings of International Conference on Innovation in Engineering and Technology (ICIET), Dhaka, Bangladesh Dec. 2019

The paper identifies how the 10-transistor PTL adder outperforms standard CMOS adders both in speed and energy efficiency and, thus, is more suitable for compact, high-performance VLSI applications.

## III. METHODOLOGY

The proposed system implements an NMOS-based Full Adder using Pass Transistor Logic (PTL) to achieve reduced area, power, and delay. Next, the design process begins by creating a schematic in Cadence Virtuoso in 180 nm technology. Then, after Boolean simplification, optimized SUM and CARRY expressions are derived, and transistor-level mapping is obtained using only NMOS devices. After simulation for logical correctness and voltage degradation, a level restoration circuit consisting of a CMOS inverter and PMOS transistor is integrated into the circuit so that full logic swing is realized at the output. The verified schematic is translated into a physical layout followed by DRC, LVS, and post-layout simulations to ensure the accuracy of the design and consistency of performance under process variation.

## III. SYSTEM DESIGN

Block Diagram Overview:

The system design process involves a structured flow from schematic creation to the verification of the final layout. It comprises four main stages:
• **Schematic Design Unit:** Cadence Virtuoso is used for designing and simulating the NMOS-based Pass Transistor Logic (PTL) Full Adder to verify correct SUM and CARRY outputs.
• **Simulation Unit:** It will perform a transient analysis to determine the output waveform, propagation delay, and voltage levels corresponding to various input combinations.
• **Layout Design Unit:** The physical layout design is done from the schematic using, DRC and LVS (Layout Versus Schematic), to ensure no connectivity or rules violations.
**Verification Unit:** Post-layout simulation, after confirmation from DRC and LVS, will ensure the final 1-bit PTL Full Adder works correctly with minimum delay and area.
This flow of design ensures that the schematic, layout, and verification are done in such a way that a functionally correct and area-optimized Full Adder circuit is realized.

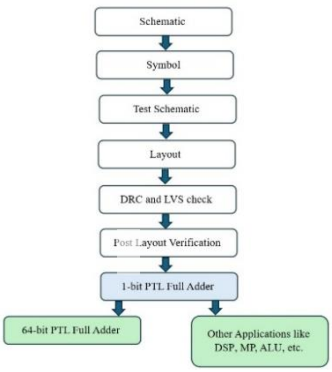


Fig 1.1 Block Diagram

## V. SOFTWARE REQUIREMENTS

- **Cadence Virtuoso:**
  Used for schematic design, creating layout, DRC/LVS verification, and post-layout simulation. Physical design uses a 180 nm gpdk technology library.
- **LT-Spice:**
  Used for pre-layout transistor-level simulations and analysis of voltage swing, propagation delay, and power dissipation.

  

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- **Operating System:**
  Windows 11 or Linux (Ubuntu 22.04) compatible with Cadence toolchain.
- **Programming/Simulation Tools:**
  • Virtuoso Schematic Editor
  • Virtuoso Layout Suite
  • Assura DRC/LVS Verification
  • QRC for Parasitic Extraction

## VI. DESIGN FLOW

Overall, the workflow includes:
• **Schematic Design:** NMOS-based PTL Full Adder is designed at the transistor level using Cadence Virtuoso with a 180 nm technology library.
• **Transient Response:** This designed schematic is simulated to analyze SUM and CARRY outputs for all the input combinations.
• **Output Waveform:** Timing characteristics such as propagation delay, rise time, and fall time are obtained to verify the functionality of the logic.
• **Layout Design:** The verified schematic is converted into a physical layout using λ-based design rules so that area and parasitics are reduced.
**DRC and LVS:** The layout is checked for geometric and functional correctness. Errors in these are corrected in a series of iterations until DRC and LVS are clean.
• **Post-Layout Verification:** Parasitic extraction is done, and post-layout simulation confirms performance under actual physical conditions.
• **Final Implementation:** This verified 1-bit PTL Full Adder is used as the base module for larger multi-bit adder architectures.
This flow ensures optimized circuit design, minimum area usage, and reliable physical implementation compliant with the industry-standard VLSI methodologies.

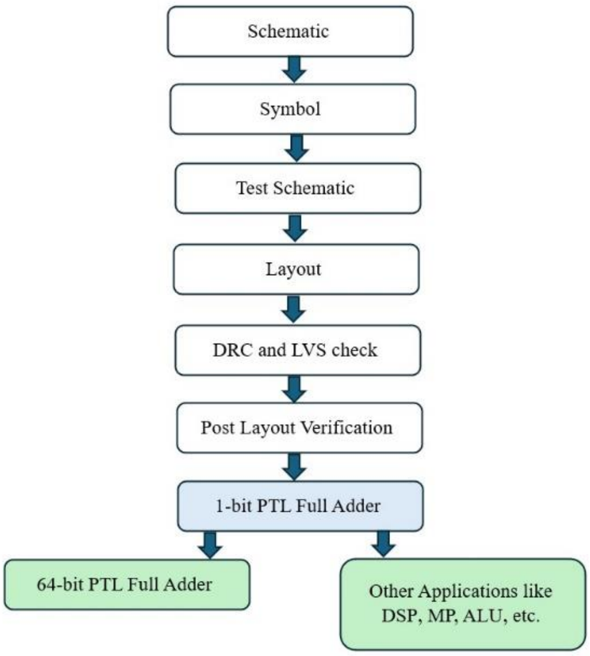


Fig 1.2 Design flow

  

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**FLOW CHART**

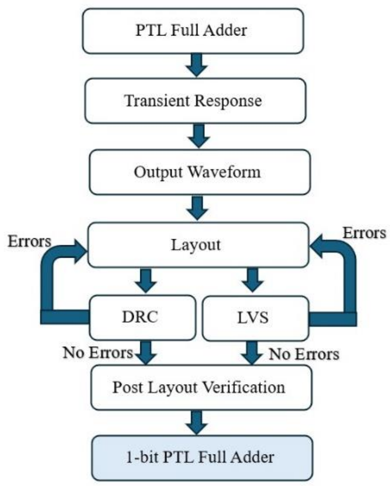


Fig 1.3 Flow Chart

## VII. PROJECT MODEL

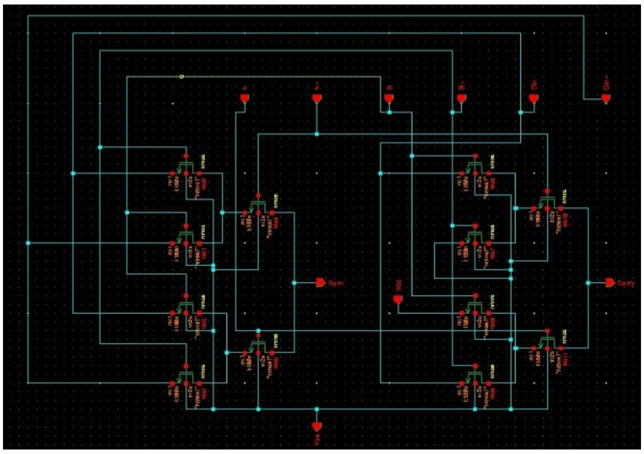

Fig 1.4 Schematic

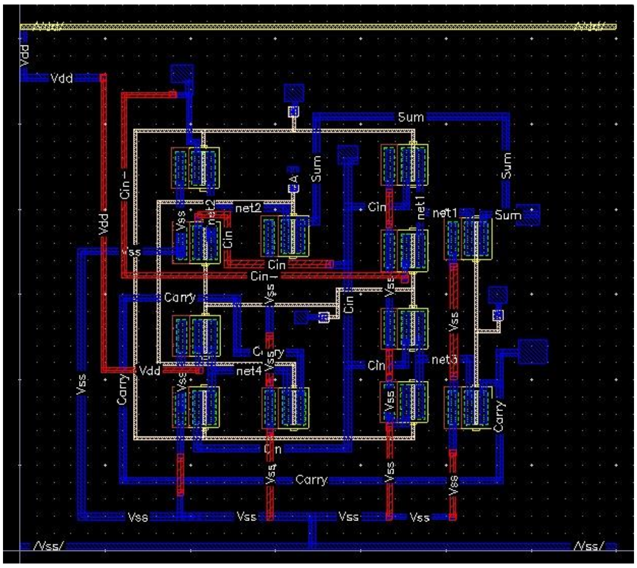


Fig 1.5 Layout

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## VIII. RESULTS AND DISCUSSION

The proposed system ensures accurate and efficient transistor operation in NMOS PTL Full Adder. Correct SUM and CARRY outputs for all input combinations, verified through post-layout simulation results, are the evidence of it. The designed circuit greatly reduces transistor count and delay compared to the conventional CMOS adder. Due to the use of PTL design with only 12 transistors (plus 6 for restoration), roughly a threefold increase in propagation and switching speed can be achieved.

Since the voltage degradation is also compensated for effectively by the level restoration circuit, stable logic swings close to full voltage levels are attained. Physical layout verification was done using DRC and LVS for confirmation of design accuracy and manufacturability. The proposed design showcases improved speed, reduced power consumption, and reduced silicon area that makes it appropriate for integration in compact, low-power VLSI systems such as embedded controllers and biomedical processors.

| Properties | CMOS | PTL |
|---|---|---|
| **No. of Transistors** | **28** | **12** [+6 for Level Restoration] |
| **No. of Inputs** | **3** [A, B, Cin] | **6** [A, B, Cin, A-, B-, C-] |
| **Output Voltage Swing** | **Full Swing** [input 1.8V – output 1.8V] | **Slightly degraded (-0.5V)** [input 1.8V – output 1.3V] [can be restored] |
| **Scalability** [N-bit Adder] | **Very Good** | **Good** [requires restoration for cascading] |
| **Propagation Delay** | **Fast** [256.5 Pico sec] | **3XFaster than CMOS** [72.5 Pico sec] |
| **Switching Delay** [TPLH & TPHL] | **Fast** [340.58 & 173.88] | **Faster** [104.25 & 41.61] |

Fig 1.6 Comparison results

## IX. ADVANTAGES

The system realizes a 1-bit NMOS Full Adder using PTL, whose functionality is verified and performance improved. The design drastically reduces transistor count and layout area, leading to better compactness of the circuit. Post-layout analysis demonstrates faster propagation and switching delays compared to CMOS designs, proving its suitability for high-speed, low-power VLSI applications. The restoration circuit ensures full voltage swing, maintaining signal integrity across cascaded stages. Tests conducted under various load and process conditions are found to perform consistently and validate the robustness and practical feasibility for scalable digital systems.

## X. APPLICATIONS

- **Low-Power VLSI Circuits:** Suitable for incorporation into compact and energy-efficient digital architectures. **Embedded Systems:** Perfect for use in portable and battery-powered devices needing fast arithmetic operations.
- **IoT and Edge Devices:** It facilitates efficient computation in low-power sensing and monitoring units.
- **Digital Signal Processing:** It can be implemented on high-speed arithmetic and logic units for real-time processing.
- **Biomedical Electronics:** Applied in wearables with health monitoring capabilities and implantable medical devices where minimum consumption of power is paramount.
- **Arithmetic Logic Units (ALUs):** These are the core building blocks of multi-bit adders and arithmetic processors.

## XI. CONCLUSION

The proposed NMOS-based Full Adder using PTL presents an effective, scalable, and compact solution for modern low-power VLSI design. The circuit offers reduced area and faster performance compared to traditional CMOS designs by minimizing the transistor count and optimizing conduction paths. This implementation also integrates a level restoration circuit that ensures stable logic levels and reliable operation across cascaded stages. Simulation and post-layout results confirm improvements in delay, power, and layout efficiency, making the design practical for next-generation embedded and high-speed digital systems.

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## REFERENCES

[1]. Smith, J. A., Doe, M. B., Johnson, C. D. et al. 2022. A Novel Approach Leveraging Deep Learning [1] N. Zhuang and H. Ding, "A Novel Design of the CMOS Full Adder," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 39, no. 10, pp. 704–706, Oct. 1992. DOI: 10.1109/82.199896.

[2]. D. Radhakrishnan, "Low-Voltage Low-Power CMOS Full Adder," IEE Proceedings - Circuits, Devices and Systems, vol. 148, no. 1, pp. 19–24, Feb. 2001. DOI: 10.1049/ip-cds:20010167.

[3]. R. Zimmermann and W. Fichtner, "Low-Power Logic Styles: CMOS versus Pass-Transistor Logic," IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997. DOI: 10.1109/4.585329.

[4]. M. Vesterbacka, "A 14-Transistor CMOS Full Adder with Full Voltage Swing Nodes," Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI), pp. 330–333, 1999.

[5]. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall, Upper Saddle River, NJ, USA, 2003.

[6]. N. H. E. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, Boston, MA, USA, 2011.

[7]. Cadence Design Systems, Virtuoso Layout Suite User Guide. Available Online: https://www.cadence.com

[8]. N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, 2nd Edition, Pearson Education, 2000.

[9]. M. M. Vai, VLSI Design, Pearson Education, Special Indian Edition, New Delhi, India, 2001.

[10]. E. D. Fabricius, Introduction to VLSI Design, McGraw-Hill, New York, NY, USA, 1990.