

A Full-Bridge Converter of the ZVZCS Type Suitable for MVDC Collection Systems Utilizing Renewable Energy

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Abstract: This research presents a full-bridge DC-DC converter that utilizes zero-voltage zero-current switching (ZVZCS), structured around a dual-transformer configuration with two output filter capacitors. The converter is engineered for seamless integration with DC collection systems in medium-voltage renewable energy applications, where stability, adaptability, and efficiency are of utmost importance. The primary switches function under a pulse width modulation (PWM) strategy with a fixed duty cycle to control voltage and power output. Under full load conditions, the main full-bridge circuit provides the majority of the power and achieves zero-voltage switching (ZVS) due to the meticulous design of the main transformer's turn ratio, which significantly reduces switching losses. To support this, an auxiliary circuit implements ZVZCS and manages a minor portion of the power. Efficiency can be further enhanced by fine-tuning the auxiliary transformer's turns ratio, which balances power contribution while minimizing conduction losses. In addition to traditional control techniques, a fuzzy logic controller is integrated to improve real-time adaptability. The fuzzy controller dynamically modifies control signals in response to fluctuating input voltage, load conditions, and switching timing, enabling the converter to sustain soft-switching conditions even amidst transient disturbances or parameter variations. It supersedes inflexible threshold-based decision-making. Utilizing linguistic principles, this approach facilitates a more intelligent management of system nonlinearity and uncertainty. The design features, the definition of the fuzzy rule base, and the optimization strategies for the suggested converter are thoroughly detailed. In order to confirm the efficacy of the proposed method and to validate the simulation outcomes, a prototype rated at 200 V / 2 kv / 3 kw has been constructed and evaluated. The findings indicate enhanced switching performance, improved thermal management, and increased overall efficiency as a result of the integrated application of ZVZCS and fuzzy logic control.

I. OVERVIEW

Researchers from across the globe have been focusing on renewable energy sources due to the increasingly concerning effects of gas emissions and pollution on the environment. Large solar photovoltaic (PV) systems and offshore wind farms serve as examples of renewable energy sources that are primarily linked to grid stations at medium voltage levels before being elevated to high voltages for the extensive transmission and distribution of electrical power [1], [2]. It is clear that medium voltage direct current (MVDC) presents significant advantages over medium voltage alternating current (MVAC) when assessing the medium voltage AC (MVAC) and medium voltage DC (MVDC) voltages for the large-scale integration of renewable energy sources. Some of these advantages include higher efficiency, enhanced stability, reduced system weight, lower costs, and the absence of reactive power [3], [4]. Consequently, MVDC technology is recommended for the broad integration of renewable energy sources. Furthermore, the DC power output from renewable energy The integration of various sources with the MVDC collection system is facilitated by sources. This technology does not encounter issues related to reactive power correction and frequency stability. Consequently, this DC collection system symbolizes the future of power systems. Numerous types of electronic DC-DC converters with high gain power have been proposed in the literature. For MVDC systems, non-isolated power electronic DC-DC converters have been documented in references [5] and [6], offering advantages such as a reduced power rating. A switched-capacitor DC-DC converter characterized by a low power rating and output capacitance was published in reference [7]. Reference [8] has showcased a resonant switched-capacitor power electronic converter utilizing a soft-switching topology, achieving high efficiency and minimal switching loss. The main drawback of using these non-isolated power electronic DC-DC converters is the reliance on passive components, which can lead to power losses and high voltage strains in high voltage applications. Depending on the voltage levels, such as medium-to-high, a frequency transformer can be employed to isolate the power electronic DC-DC converters. This galvanic isolation removes the

necessity for high-voltage switches and diminishes the protection requirements in renewable energy sources. For high power applications, isolated power electronic DC-DC converters have been frequently chosen, including phase shift full-bridge converters [9], [10], [11], LCC series-parallel resonant converters [12], [13], single active type bridge converters [14], [15], and three phase dual active bridge DC-DC converters [16]. The full-bridge configuration is utilized for constructing the aforementioned converters in high-power applications. Two methods are utilized to achieve soft-switching for these full-bridge converter topologies. They reduce power and switching losses to attain a high gain. The first method is ZVS [11], [17], and [18]. The second method is ZVZCS [19], [20]. ZVS is particularly suitable for mosfets due to their. Applications are favoured due to their ability to handle higher current and voltage ratings compared to mosfets. Nevertheless, the tail current effect influences the igbts [21], [22]. The zero-current switching (ZCS) technique mitigates the tail current effect by reducing the turn-off switching loss [23], [24]. However, for ZCS to be achieved, the current must decrease to zero prior to the commutation. This can be accomplished through either the resonance mode [25] or the current reset mode [26]. Modifications to the converter's structure have enabled the auxiliary circuits in [27] and [28] to achieve the resonance mode. ZCS can be realized using resonance techniques, such as the LCC resonance type, with the switch's frequency adjustable to regulate the output voltage [29]. A significant drawback of these auxiliary circuits is their electromagnetic compatibility and the design of the inductive filter, which becomes more complex when a variable switching frequency is employed [29], [30]. The single active bridge converter in [15] utilizes interleaving currents to reduce the ripple in the output current. However, a major disadvantage of this method is that the high switch turn-off currents diminish conversion efficiency. A soft-switching study covering a broad operational range was presented by the three-phase dual active bridge converter proposed in [16]. However, it is less suitable for high voltage applications due to the requirement for the switches to withstand high voltage stresses. To achieve ZCS, the researchers in [31] introduced a topology for the primary IGBT switches that incorporates full-bridge cells and a dual transformer. However, conduction loss and the transformer increased due to the significant amplitude of the triangle current. As a result, the design of the inductive filter becomes complex and costly to manufacture. All these limitations significantly affect the efficiency and practicality of the converter. This research proposes a full-bridge ZVZCS DC-DC converter based on a dual transformer with two output filter capacitors, which is particularly suitable for medium voltage applications. Which provides the advantage of straightforward control. Through optimization, the turns ratio of the primary transformer and primary full-bridge converter can effectively transfer a substantial amount of power while also achieving Zero Current Switching (ZCS) across the entire load range. Consequently, the switching losses are significantly reduced. To further minimize converter losses and enhance conversion efficiency, the turns ratio of the secondary transformer can also be modified. Moreover, the converter circumvents the necessity for large inductance and high voltages by employing output capacitive filtering for medium and high output voltages. The organization of this document is outlined as follows. The circuit architecture and operational principle of the proposed converter are detailed in Section II. Section III discusses the parameter design. The simulation analysis conducted to validate the proposed converter's design is presented in Section IV, confirming the effectiveness of the proposed topology and the simulation outcomes.

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II. DESIGN AND OPERATION PRINCIPLE OF CIRCUITS

For applications requiring high power, igbts are integrated within the full-bridge converter configuration. Zero Voltage Zero Current Switching (ZVZCS) can be utilized for the switches to operate with a fixed duty cycle of 50%, thereby achieving significant efficiency at elevated power levels without necessitating additional control circuitry. This approach is employed in the discontinuous conduction mode (DCM), which is commonly observed in traction systems and resonant transformers. However, its main drawback is that this state cannot be maintained in high power applications. To address this limitation, an auxiliary circuit is introduced in Fig. 1, allowing the igbts to operate through their control.

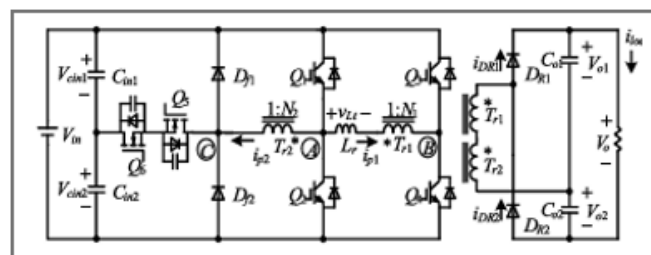


Figure 1. Proposed converter.

In DCM, both the voltages and currents will reach zero. By adjusting the transformer turns ratios, it is feasible to decrease the control current and switching losses, allowing a smaller current to flow through the auxiliary switches while a larger current flows through the main switches. Based on the preceding analysis, a ZVZCS full-bridge converter is proposed. This converter is responsible for the ZVZCS function, as depicted in Figure 1. The full-bridge circuit consists of four primary IGBT switches (Q1–Q4), an inductor (L_r), and a transformer (Tr1) with a turns ratio of N_1 . The auxiliary circuit is composed of two MOSFET switches (Q5 and Q6), capacitors C_{in1} and C_{in2} , diodes for freewheeling operations Df1 and Df2, and a transformer Tr2 with a turns ratio of N_2 . The connection between the two secondary terminals of the transformers is illustrated in Fig. 1. This configuration is implemented to achieve a voltage-doubler rectifier circuit input where the current remains constant. The power distribution is arranged such that the full-bridge converter supplies approximately 90% of the power, while the auxiliary circuit accounts for the remaining 10%.

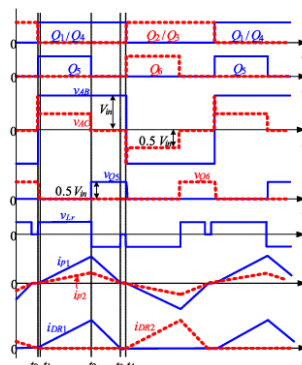


Figure 2. Key waveforms of the proposed converter.

The primary waveforms of the proposed converter are illustrated in Fig. 2. The gating pulse replaces the Q1, Q4, Q2, and Q3 switches, ensuring adequate dead time and a specified duty cycle of 50%. The transitions of Q1/Q4 and Q2/Q3 are not synchronized. A PWM-based control method, which functions on the leading edges of Q1 and Q4, is employed for the switches Q5 and Q6.

The duty cycles of Q5 and Q6 control the output voltages of the proposed converter. The analysis is based on the following assumptions:

- 1) Each semiconductor device utilized is considered to be ideal.
- 2) Given that the input capacitor values C_{in1} and C_{in2} are kept constant, it follows that $V_{cin1} = V_{cin2} = V_{in}/2$.
- 3) To ensure that the output voltage stabilizes at a constant level where $V_{o1} = V_{o2} = V_o/2$, the filter capacitors C_{o1} and C_{o2} are maintained at a high, equal value.
- 4) The leakage inductance of the auxiliary transformer Tr2 is deemed negligible due to its low value.

For simplicity, we will focus solely on the half-cycle of the proposed circuit. Figure 3 illustrates the four operational modes of the converter. At time t_0 , a new switching cycle commences. The switches Q1, Q4, and Q5 are activated, while Q2 and Q3 are turned OFF at the moment of t_0 . Prior to the initiation at time t_0 , no current flows through any of the switches. Zero Current Switching (ZCS) is employed to turn ON switches Q1, Q4, and to turn OFF Q2 and Q3. Furthermore, the voltage across Q6 is $V_{in}/2$, while the voltage across Q5 is zero, indicating that it is activated with Zero Voltage Zero Current Switching (ZVZCS). The complete analysis is presented as follows:

Mode 1: This mode operates between t_0 and t_1 . The voltage $v_{ab} = V_{in}$ results from the primary current i_{p1} from Tr1 flowing through Q1, Q4, L_r , Tr1, and C_{in1} . Similarly, the primary current i_{p2} from Tr2 flows through the windings of Q1, Q4, Q5, Tr2, the parasitic capacitance of Q6, and C_{in1} . The voltage $v_{ac} = 0.5V_{in}$ is the result of the voltages across Q6 discharging from $0.5V_{in}$ to zero at the instant t_0 . Current i_{p1} traverses through Q1, L_r , Tr1, and Q4, while i_{p2} flows through Tr2, Q5, and Q1, as depicted in Figure 3(a). Consequently, the current passing through switches Q1 and Q4 is the sum of i_{p1} and i_{p2} .

Mode 2: This mode operates between t_1 and t_2 . The current i_{p2} also flows through the body diode of switch Q6 since the voltage across it was reduced to zero in the previous mode at instant t_1 . As a consequence, i_{p1} takes a comparable path. Thus, the current through L_r rises in a linear fashion. Currently, the point voltages remain unchanged from Mode-1, indicating that $v_{ab} = V_{in}$ and $v_{ac} = 0.5V_{in}$. The primary current of Tr2, denoted as i_{p2} , traverses through Q1, Q4, Q5, and C_{in1} . The secondary terminal voltage of Tr1 is expressed as $0.5(V_o - N_2V_{in})$, whereas the secondary terminal voltage of Tr2 is represented as $0.5V_{in}/N_2$. For the circuit to operate effectively in this mode, it is essential that v_{lr} exceeds zero. As illustrated in Fig. 4, this results in a nonlinear decrease of v_{p2} , while i_{p1} , i_{p2} , i_{dr1} , and v_{p1} all experience a

linear increase. The current i_{p2} now flows through the anti-parallel diode of Q6. The current flowing through switches Q1 and Q4 is shown in Fig. 3(b) as the aggregate of i_{p1} and i_{p2} .

$$V_{Lr} = V_{in} + 0.5N_2V_{in}/N_1 - V_o/2N_1$$

(1)

$$i_{p1}(t) = \frac{V_{in} + 0.5N_2V_{in}/N_1 - V_o/(2N_1)}{L_r}(t - t_0) \quad (2)$$

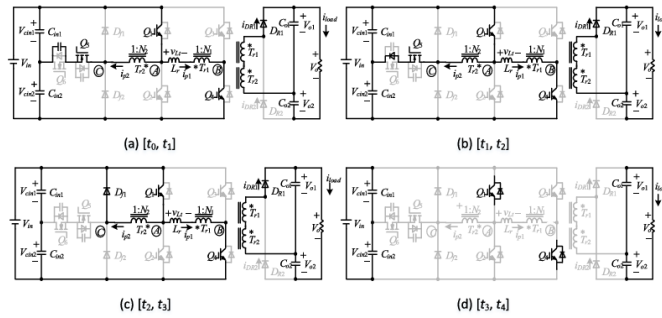


Figure3. Circuit paths of the four modes of operation of the proposed converter.

$$i_{p2}(t) = i_{p1}N_2/N_1 \quad (3)$$

$$i_{DR1}(t) = i_{p1}(t)/N_1 \quad (4)$$

Mode 3: This mode operates between t_2 and t_3 . In the case of ZCS, the switch Q5 is turned off. The current that previously flowed through the body diode of Q6 now starts to charge the parasitic capacitance of Q5.

$$i_{Lr} = V_{in} - V_o/(2N_1) \quad (5)$$

This mode necessitates that v_{lr} be less than zero for proper functionality, leading to a linear decay in the currents i_{p1} , i_{p2} , and i_{dr1} , as detailed below:

$$i_{p1}(t) = \frac{V_{in} + \frac{N_2V_{in} - V_o}{2N_1}}{L_r} \frac{D}{T_s} + \frac{V_{in} - \frac{V_o}{2N_1}}{L_r}(t - t_1) \quad (6)$$

$$i_{DR1}(t) = i_{p1}(t)/N_1 \quad (7)$$

$$i_{p2}(t) = i_{p1}(t)N_2/N_1 \quad (8)$$

In this scenario, D represents the duty ratio for switches Q5 and Q6. T_s indicates the duration of the switching time period. The current flowing through switch Q4 is illustrated in Fig. 3(c) as the total of both i_{p1} and i_{p2} . Mode 4: This mode operates between t_3 and t_4 . At the moment t_3 , the currents i_{p1} , i_{p2} , and i_{dr1} drop to zero due to effective design on L_r , N_1 , and N_2 . Zero Current Switching (ZCS) is employed to deactivate the diodes D_{f1} and D_{R1} . The condition $N_1V_{in} - N_2 < 0.2V_o$ holds true because the magnitude of the reflected voltage is lower than the rectified voltage. During this mode, switches Q1 and Q4 are activated, yet no current flows through them. The supply is derived from i_{p1} , i_{p2} , i_{dr1} , C_{o1} , and C_{o2} . The current pathway for Mode-4 is depicted in Fig. 3(d). The initial half of the switching cycle concludes at the moment t_4 , and simultaneously, the second half of the cycle commences. As L_t is responsible for controlling the current increase, switches Q2, Q3, and Q6 are now activated with ZCS, while Q1 and Q4 are deactivated with ZCS. It activates with Zero Voltage Zero Current Switching (ZVZCS) since the voltage across switch Q6 remains at zero when transitioning from Mode-3 to Mode-4. A fixed gating sequence mechanism has been employed for the Q1Q4 switches. However, these switches can also operate with PWM, allowing for the possibility of turning off switches Q1 and Q4 at the specific moment t_3 . Given that no current flows through these switches, the PWM-based control will not influence the operation of the proposed converter. A significant drawback of implementing PWM control for switches Q1 and Q4 is the necessity of a current sensor to verify ZCS switching, which is essential for accurately recording the precise moment of t_3 . Consequently, PWM-based control is not selected for the first four switches. In

summary, for switches Q1 and Q4 to be activated and deactivated using ZCS, they must withstand V_{in} . In contrast, switches Q5 and Q6 need to endure $0.5V_{in}$ to be turned ON with ZVZCS and OFF with ZVS. The switching characteristics of the switches and diodes considered in the previous analysis are detailed in Table 1.

TABLE1. Voltage Stress and Switching Characteristics

	Q_1, Q_4	Q_5, Q_6	D_{f1}, D_{f2}	D_{R1}, D_{R2}
Turn-ON	ZCS	ZVZCS	—	—
Turn-OFF	ZCS	ZVS	ZCS	ZCS
Voltage Stress	V_{in}	$0.5V_{in}$	V_{in}	V_o

III. PARAMETER DESIGN

Table 2 contains the characteristics of the suggested converter for this experimental study.

TABLE 2. Specifications.

Input Voltage V_{in}	1.5 kV
Output Voltage V_o	15 kV
Rated Power P_N	1 MW
Switching Frequency f_s	1 kHz

A. TURNS RATIO

A critical design factor for all industrial applications is the turns ratio. It is imperative that the transformer's turns ratio is appropriately sized to ensure that the auxiliary circuit provides the remaining power while the full-bridge section delivers the majority. To maintain simplicity, We will discuss the first half-cycle to illustrate how the turns ratio influences the distribution of power between the two components of the circuit. If the proposed converter achieves a transmission efficiency of 100%, the total power P_{tot} for the interval $[t_0, t_4]$ can be expressed as follows:

$$P_{tot} = \frac{2}{T_s} \frac{V_o}{2} \int_{t_0}^{t_3} i_{DR1} dt = \frac{V_o}{T_s} \int_{t_0}^{t_2} i_{DR1} dt \quad (9)$$

The power that the Tr1 transfers during $[t_0, t_4]$ is stated as follows:

$$P_m = \frac{2}{T_s} V_{in} \int_{t_0}^{t_3} i_{p1} dt = \frac{2V_{in}}{T_s} \int_{t_0}^{t_2} i_{p1} dt \quad (10)$$

From (3) and (7), P_m also can be expressed as:

$$P_m = \frac{2V_{in}}{T_s} \int_{t_0}^{t_3} N_1 i_{DR1} dt = \frac{2N_1 V_{in}}{T_s} \int_{t_0}^{t_2} i_{DR1} dt \quad (11)$$

Combining (9) and (11), one can obtain

$$\frac{P_m}{P_{tot}} = \frac{2N_1 V_{in}}{V_o} \quad (12)$$

The subsequent expression represents the power transmitted by the auxiliary circuit, in accordance with the law of conservation of energy:

$$P_a = P_{tot} - P_m \quad (13)$$

The subsequent power distribution is obtained from equations (12) and (13):

$$\frac{P_m}{P_a} = \frac{P_m}{P_{tot} - P_m} = \frac{2N_1 V_{in}}{V_o - 2N_1 V_{in}} \quad (14)$$

Once N_1 and the voltages have been calculated, the P_m/P_a ratio is assessed. The power ratios along with their parameters are illustrated in Fig. 4. It is observable that the ratios of P_{in}/P_{tot} and P_a/P_{tot} fluctuate in unison with an increase in N_1 .

Therefore, it is clear that the power distribution between the full-bridge and the auxiliary circuit is influenced by the value of N_1 . Furthermore, the full-bridge circuit requires a significant value of N_1 to handle more power than the auxiliary circuit. As indicated in Fig. 4, the ratios of $P_{in}/P_{tot} = 90\%$, $P_a/P_{tot} = 10\%$, and $P_m/P_a = 9:1$ are achieved when N_1 is set to 4.5. The time ratio r_t , representing the rise time to fall time, can be less than, greater than, or equal to 1, as determined, since the rise time of this half-cycle is longer than the fall time, as shown in Fig. 2.

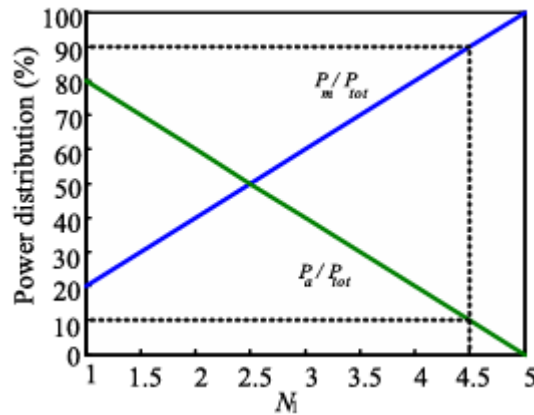


Figure 4. Power distribution versus N_1 .

From N_2 . The value of r_t can be determined by utilizing equation (15) along with the volt-second balance principle of the inductor.

$$r_1 = \frac{t_1 - t_0}{t_2 - t_1} = \frac{V_o/2 - N_1 V_{in}}{N_1 V_{in} + 0.5 N_2 V_{in} - V_o/2} \quad (15)$$

The subsequent results can be derived by rearranging this equation:

Given that N_1 is presumed to be 4.5, Fig. 5 illustrates the r_t versus N_2 curve obtained from (16).

As r_t diminishes, it becomes clear that the value of N_2 increases. Therefore, this demonstrates the impact of N_2 on the power loss of the converter.

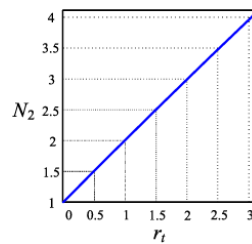


Figure 5. Curve of r_t versus N_2 when $N_1 = 4.5$.

B. INDUCTOR "LR"

It is essential to decrease both the low-voltage inductance and the use of high-voltage inductors. $T_s/2$ is equivalent to the total of the rise and fall times. These times are specified as follows:

$$T_r = t_1 - t_0 = T_s r_1 / (2 + r_1) \quad (17)$$

$$T_f = t_2 - t_1 = T_s / (2 + 2r_1) \quad (18)$$

From (2) and (17), the inductance can be written as follows:

$$L_r = T_s \frac{(N_1 V_{in} + \frac{1}{2} N_2 V_{in} - 2 N_1 V_{in})}{2 N_1 N_2 V_{in} I_{peak}} \quad (19)$$

The maximum current of IP1 at the specified power level is referred to as I_{peak} .

It is essential that the inductor's value remains below the threshold established in (19) for the converter to operate effectively.

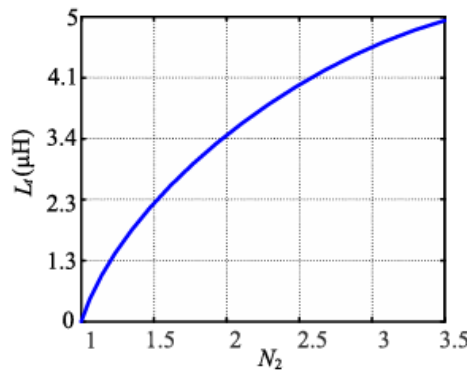


Figure 6. Relationship of L_r and N_2 when $N_1 = 4.5$.

Figure 6 illustrates the connection curve between L_r and N_2 as presented in (19). It is clear that an increase in N_2 corresponds with a rise in inductance.

C. "CO1 & CO2" OUTPUT FILTER CAPACITORS

The output filter capacitors serve to reduce the high voltage ripples caused by high current fluctuations, and the voltage-doubler rectifier configuration is employed to decrease the turns ratio of the main transformer. "U" represents the charging phase of Co_1 , where $ico_1 = idr_1 - I_{load} > 0$, while "D" denotes the discharging state, where $ico_1 < 0$. Consequently, under steady-state conditions, the areas "U" and "D" are equivalent. One method to articulate the load current is as follows:

$$I_{load} = \frac{P_N}{V_o} = \frac{1}{T_s} \int_{t_0}^{t_3} i_{DR1} dt = \frac{1}{4} \frac{I_{peak}}{N_1} \quad (20)$$

The ratio I_{peak}/N_1 indicates the peak value of idr_1 . The anticipated time interval for "U" is $3T_s/8$ for any r_t value, as derived from equations (17) and (20). Consequently, the peak-to-peak voltage ripple value is determined as follows:

$$\Delta V_{pp} = \frac{1}{C_{o1}} \left(\frac{I_{peak}/N_1 - I_{load}}{2} \right) \frac{3T_s}{8} \quad (21)$$

When (20) and (21) are combined, the resulting output filter capacitor values are as follows:

$$C_{o1} = C_{o2} = \frac{9}{64} \frac{I_{peak}}{N_1 \Delta V_{pp} f_s} \quad (22)$$

D. DESIGN ILLUSTRATION

A comprehensive design example is provided in this chapter, referred to as Case A in the subsequent Simulation Analysis section. Initially, it is established that the output voltage V_o is 15 kv, while the input voltage V_{in} is 1.5 kv. The converter is rated for a power of 1 MW and operates at a switching frequency (f_s) of 10 khz. The design of the temporal ratio r_t is derived from equation (15), with a value of 0.5 selected. N_1 is determined to be 4.5 based on the preceding subsection and Fig. 4, and N_2 is calculated using equation (16), resulting in a value of 1.5. From the output voltage and rated power, the load current I_{load} is computed to be 67 A, as per equation (20). The peak current I_{peak} , which is found to be 1.2 ka based on the measurement of the load current, can also be derived using equation (20). According to equation (19), the inductor L_r is calculated to be 2.315 μH . The peak-to-peak voltage ripple V_{pp} , which is approximately 1% of the output voltage, amounts to 150 V and is utilized to estimate the output filter capacitors. Finally, it is determined that the output capacitors Co_1 and Co_2 have a value of 25 μf , as indicated in equation (22).

E. EVALUATION OF ALTERNATIVE CONVERTERS

The existing literature indicates various converter topologies that utilize twin transformers. To demonstrate the enhanced performance and effectiveness of the proposed converter, Table 3 provides a comparison between the proposed converter and the existing literature.

IV. ANALYSIS OF SIMULATIONS

A simulation is conducted utilizing PLECS software to validate the operational principle of the proposed converter and to assess the influence of the turns ratio N_2 on the losses and current. Magnitude. In the simulation analysis, three cases—

A, B, and C—were established with different parameters. Table 4 enumerates these significant parameters utilized in the simulation. To assess its effect on the inductor L_r and capacitors C_{o1} and C_{o2} , along with other parameters to validate ZVZCS, the turns ratio N_2 is kept constant for each scenario. The actual power P_o is slightly less than the theoretical power P_N . The primary element affecting the power transfer between the primary full-bridge and auxiliary full-bridge circuits is the turns ratio N_1 . However, the overall power losses of the converter are greatly influenced by the turns ratio N_2 . Three scenarios—A ($N_2 = 1.5$, $n = 0.5$), B ($N_2 = 1.25$, $n = 0.25$), and C ($N_2 = 1.1$, $n = 0.1$)—have been analyzed to determine the effect of the turns ratio N_2 , while ensuring a consistent turns ratio $N_1 = 4.5$ across all cases to maintain uniform power distribution for all N_2 values. These cases, $T_r < T_f$, $T_r = T_f$, and $T_r > T_f$, respectively, illustrate three unique current waveforms. The inductance L_r for each of the three scenarios can be calculated using (19) for various N_2 values. According to (20), the peak and average values of i_{p1} for the three cases are the same. Since the currents flowing through the secondary windings of both transformers are identical, the primary current (i_{p2}) and the currents through Q5, Q6, and N2 are directly proportional to one another. As the currents through Q3, Q4, and i_{p1} and i_{p2} equal the sum of both, they also vary in direct proportion to N_2 . The total power P_{tot} of the converter is set below its rated power of 1 MW to ensure operation in DCM. The simulated waveforms for v_{ab} , v_{ac} , v_{lr} , i_{p1} , and i_{p2} for the three scenarios are presented in Fig. 7. Figure 8 illustrates the waveforms of i_{p1} , i_{p2} , and the current through Q1 for the three scenarios.

TABLE 3. Comparison of proposed converter with similar topologies in literature.

	[24]	[19]	[32]	[33]	[28]	Proposed
Switching Frequency	5 kHz	10 kHz	15 kHz	20 kHz	10 kHz	10 kHz
No. of Switches	6	6	10	10	6	6
No. of Diodes	4	6	0	0	6	4
Rated Power	1.4 kW	1.4 kW	1.2 kW	0.3 kW	1.4 kW	3 kW
Soft-switching	ZVS & ZCS	ZVS & ZCS	ZVS	ZVS	ZVS & ZCS	ZVS & ZCS
Full-load Efficiency	97.3%	97.3%	96.5%	94%	97.2%	97%

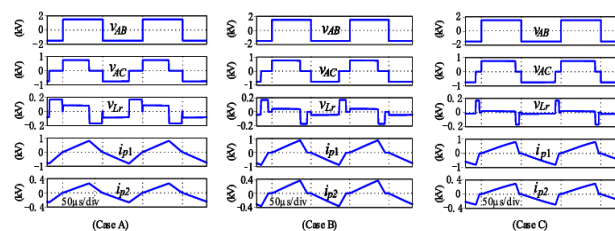


Figure 7. Simulation waveforms showing v_{ab} , v_{ac} , v_{lr} , i_{p1} and i_{p2} for the three cases.

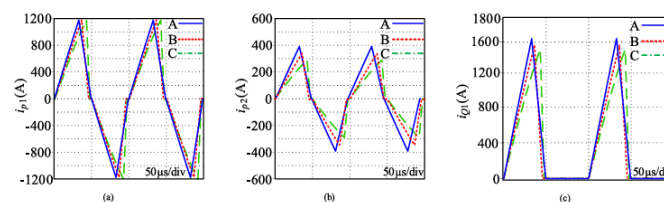


Figure 8. Simulation waveforms of the three cases. (a) i_{p1} , (b) i_{p2} , (c) Current flowing through switch Q1.

TABLE 4. Simulation parameters.

Parameters	A	B	C
Theoretical Power P_N	1 MW		
Input Voltage V_{in}	1.5 kV		
Output Voltage V_o	15 kV		
Switching Frequency f_s	1 kHz		
Time Ratio r_t	0.5	0.25	0.1
Turns Ratio N_1	4.5		
Turns Ratio N_2	1.5	1.25	1.1
Inductance L_r	$2.315\mu H$	$1.389\mu H$	$0.631\mu H$

Instances. The primary current i_{p1} exhibits identical average and peak values across various time ratios r_t , as illustrated in Fig. 8(a). Consequently, for different N_2 values, the losses in switches Q1 and Q2 remain consistent across all three scenarios. Fig. 8(b) presents the values of. In every instance, there are significant differences in both the average and

peak values of i_{p2} . Given the differing circumstances, the conduction loss can be categorized as $A > B > C$. The primary current i_{p1} demonstrates the same average and peak values for various time ratios r_t , as depicted in Fig. 8(a). It can be deduced that case C experiences the least conduction losses, as the 32440 turn-off currents of Q5, Q6, and i_{p2} are equivalent. It is clear from Fig. 8(c) that the current flowing through Q3(Q4) equals the sum of the currents flowing through Q2, Q6(Q1, Q5), with Q3(Q4) exhibiting the lowest current value. These three cases illustrate that the average and peak current values through switches Q3 and Q6 diminish as the current decreases.

N2 results in reduced switching and conduction losses. It is important to highlight that the simulation analysis conducted previously utilized ideal transformers without accounting for their shortcomings. In each of the three scenarios, the primary transformer handles the same power, turns ratio, average, and peak values. Consequently, the losses of the primary transformer are approximately equal across all three scenarios. The auxiliary transformer processes identical power and current values in each scenario; however, in example C, it exhibits a significantly lower primary current compared to cases A and B, suggesting that the auxiliary transformer in case C is the most efficient in terms of losses. In conclusion, the simulation findings indicate that a modest value of N2 is essential for achieving high conversion efficiency and minimal required inductance. The following presents the complete analysis: Improved Version with Fuzzy Logic: For high-power applications, igbts are incorporated into a full-bridge converter configuration, where a fuzzy logic controller (FLC) is utilized to improve operational efficiency. Unlike traditional control techniques, FLC offers dynamic adaptability by processing vague inputs and modifying the switching states in real-time. This method guarantees optimal performance under fluctuating load conditions while sustaining a 50% fixed duty cycle. The implementation of FLC enhances the system's resilience, especially in traction systems and resonant transformers, by accelerating response time and minimizing power losses. Furthermore, the auxiliary circuit depicted in Fig. 1 facilitates precise control of the igbts, allowing for efficient operation at elevated power levels. In scenarios where both voltages and currents drop to zero in DCM, it becomes feasible to decrease the control current and switching losses by adjusting the transformer turns ratios, enabling a smaller current to flow through the auxiliary switches while a larger current flows through the main switches. A ZVZCS full-bridge converter is proposed based on the aforementioned analysis. The proposed converter is in The full-bridge circuit consists of switches (Q1–Q4), an inductor (L_r), and a transformer (Tr1) with a turns ratio of N1. The auxiliary circuit is composed of two MOSFET switches (Q5 and Q6), capacitors C_{in1} and C_{in2} , diodes for freewheeling operations (Df1 and Df2), and a transformer (Tr2) with a turns ratio of N2. The connection between the two secondary terminals of the transformers is illustrated in Figure 1. This configuration is implemented to achieve a voltage-doubler rectifier circuit input, ensuring that the current remains constant. Power distribution is arranged such that the full-bridge converter supplies approximately 90% of the power, while the auxiliary circuit accounts for the remaining 10%. The paragraph model adeptly oversees the system's performance by modifying switching sequences and managing power distribution, thereby facilitating efficient energy conversion and minimizing losses. The primary waveforms of the proposed converter are presented in Fig. 2. The gating pulse replaces the switches Q1, Q4, Q2, and Q3, ensuring adequate dead time and a fixed duty cycle of 50%. The transitions of Q1/Q4 and Q2/Q3 are not synchronized. PWM-based control, which functions on the leading edges of Q1 and Q4, is employed for switches Q5 and Q6. The duty pulses of Q5 and Q6 are responsible for regulating the output voltages of the proposed converter. The analyses are based on the following assumptions: Each semiconductor device utilized is considered an ideal device.

Given that the values of the input capacitors C_{in1} and C_{in2} are kept constant, it follows that $V_{cin1} = V_{cin2} = V_{in}/2$. To ensure that the output voltage reaches a steady state where $V_{o1} = V_{o2} = V_o/2$, the filter capacitors C_{o1} and C_{o2} are maintained at a high, uniform value.

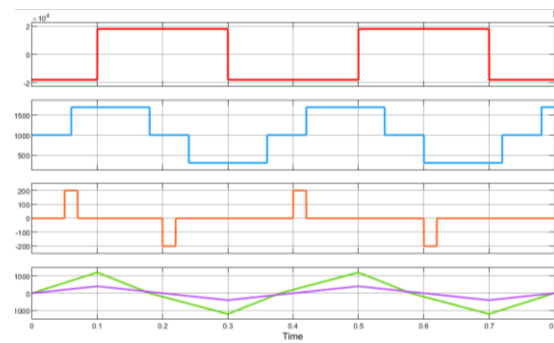
Due to its low value, the leakage inductance of the auxiliary transformer Tr2 is deemed negligible. For simplicity, we will focus solely on the half-cycle of the proposed circuit. Fig. 3 illustrates the four operating modes of the converter. At time t_0 , a new switching cycle commences. At this moment, switches Q1, Q4, and Q5 are activated, while Q2 and Q3 are deactivated. Before the initiation The paragraph model proficiently handles these switching sequences and enhances energy conversion through accurate power regulation.

Mode 1: This mode takes place between the time intervals t_0 and t_1 . Within this timeframe, the voltage $v_{ab} = V_{inv_AB} = V_{in}$ is generated by the primary current i_{p1_p1} of transformer Tr1, which flows through switches Q1, Q4, inductor l_{rlr} , Tr1, and capacitor C_{in1} . Concurrently, the primary current i_{p2_p2} from Tr2 traverses Q1, Q4, Q5, Tr2, the parasitic capacitance of Q6, and C_{in1} . The voltage at point AC, $v_{ac} = 0.5V_{inv_AC} = 0.5V_{in}$, results from Q6 discharging from $0.5V_{in}$ to 0 at time t_0 . The currents i_{p1_p1} and i_{p2_p2} share a common route through Q1 and Q4, and their combined flow is depicted in Fig. 9(a).

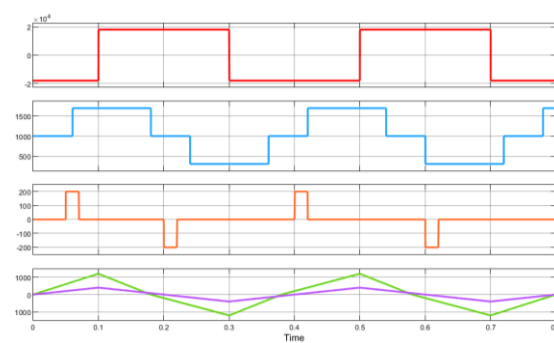
Mode 2: Covering the period from t_1 to t_2 , this mode witnesses i_{p2_p2} starting to flow through the body diode of Q6 as the voltage across it decreases to zero at the conclusion of Mode 1. Simultaneously, i_{p1_p1} continues along

a similar trajectory, leading to a linear increase in current through I_{rl_rlr} . The voltage conditions remain consistent with those in Mode 1, preserving $v_{ab}=V_{inv_AB}=V_{in}$, $v_{ab}=V_{in}$ and $v_{ac}=0.5V_{inv_AC}=0.5V_{in}$, $v_{ac}=0.5V_{in}$. The primary current i_{p2} of Tr2 flows through Q1, Q4, Q5, and Cin1. The secondary terminal voltage of Tr1 is $0.5(V_o - N_2V_{in})$, while Tr2's is $0.5V_{in} - N_2V_{in}$. To guarantee a reliable transition between modes, the voltage across I_{rl_rlr} , v_{lr} , must remain above zero. As illustrated in Fig. 10, this results in nonlinear behaviour in v_{p2} , while i_{p1} , i_{p2} , i_{dr1} , and v_{p1} increase linearly. In this context, a fuzzy logic controller can improve dynamic adaptability by identifying transition points (such as body diode conduction) and modifying gate signals in real-time to minimize switching losses and facilitate soft switching.

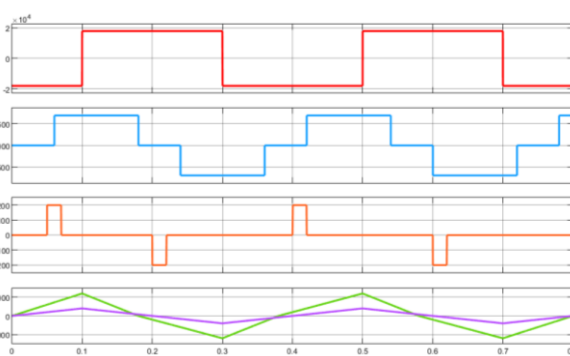
Mode 3: Functioning between t_3 and t_4 , this mode signifies the reduction of currents i_{p1} , i_{p2} , and i_{dr1} to zero, influenced by optimal selection.



Case1



Case2



Case 3

Figure 9: Simulation waveforms showing v_{ab} , v_{ac} , v_{lr} , i_{p1} and i_{p2} for the three cases.

V. CONCLUSION

This document presents a ZVZCS full-bridge DC-DC converter that functions in DCM and utilizes a dual transformer along with two output capacitive filters. The proposed converter consists of one main transformer, two auxiliary

transformers, and four primary switches. The auxiliary switches experience significantly lower power and current stress compared to the main switches. The distribution of power between the two transformers is governed by the turns ratio of the main transformer. A full-bridge DC-DC converter is proposed based on the ZCS technique, ensuring ZCS for each primary switch. Auxiliary switches can utilize mosfets due to their lower voltage stresses compared to the primary switches, enabling ZVZCS operation. Consequently, the switching losses of the converter can be substantially reduced while maintaining high efficiency. Alongside a comprehensive explanation of the operational principles of the proposed PWM-based full-bridge converter, the design parameters have been established. The performance of the proposed converter is further validated through experimental results, and the simulation outcomes align with the derived operational principles. High experimental efficiency has been achieved across a wide load range.

REFERENCES

- [1]. C. Rahmann, V. Vittal, J. Ascui, and J. Haas, "Mitigation control against partial shading effects in large-scale PV power plants," *IEEE Trans. Sustain. Energy*, vol. 7, no. 1, pp. 173–180, Jan. 2016.
- [2]. S. Cui, N. Soltan, and R. W. De Doncker, "A high step-up ratio soft switching DC–DC converter for interconnection of MVDC and HVDC grids," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2986–3001, Apr. 2018.
- [3]. C. Meyer, key components for future off shored cgrids. rwthaachen: Shaker, 2007.
- [4]. Y. Chen, Z. Li, S. Zhao, X. Wei, and y. Kang, "Design and implementation of a modular multilevel converter with hierarchical redundancy ability for electric ship MVDC system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 189–202, Mar. 2017.
- [5]. H. Athab, A. Yazdani, and B. Wu, "A transformerless DC–DC converter with large voltage ratio for MV DC grids," *IEEE Trans. Power Del.*, vol. 29, no. 4, pp. 1877–1885, Aug. 2014.
- [6]. W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and comparison of medium voltage high power DC/DC converters for offshore wind energy systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 2014–2023, Apr. 2013.
- [7]. W.Qian,D.Cao,J.G.Cintron-Rivera, M.Gebben,D.Wey,andf.Z.Peng, "A switched-capacitor DC–DC converter with high voltage gain and reduced component rating and count," *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1397–1406, Jul. 2012.
- [8]. W. Chen, X. Ruan, and R. Zhang, "A novel zero-voltage-switching PWM full bridge converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 793–801, Mar. 2008.
- [9]. J. You, D. M. Vilathgamuwa, N. Ghasemi, and B. Fu, "Virtual resistor based integrated DC bus voltage conditioner for stability improvement of cascaded power converters," *IEEE Access*, vol. 7, pp. 95959–95969, 2019.
- [10]. D.-D.Tran,H.-N.Vu,andw.Choi,"Anovelquasi-resonantzvzcsphase shift full bridge converter with an active clamp in the secondary," in *Proc. IEEE8thInt. Powerelectron. Motion Control Conf. (IPEMC-ecceasia)*, May 2016, pp. 492–495.