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Design of R-2R Digital to Analog Converter (DAC) using CMOS Technology

Mahantesh H.[1], Aditya U. M.[2], Akash R. M.[3], Anushree A. U.[4], Hanamanth Laddi[5]

Assistant Professor, Department of E & CE, B.I.E.T., Davanagere, Karnataka, India[1]

Student, U.G., Departmentof E & CE, B.I.E.T., Davanagere, Karnataka, India[2,3,4,5]

Abstract: This work presents the design and simulation of a two-stage CMOS operational amplifier integrated into an R-2R ladder-based Digital-to-Analog Converter (DAC). Implemented in 180nm CMOS technology, the amplifier comprises a differential input stage and a common-source gain stage, optimized for high gain, stability, and low power. The design supports 4-bit and 8-bit R-2R DAC architectures to achieve accurate digital-to-analog conversion. Simulations using Cadence Virtuoso and Spectre validated DC, AC, and transient performance, confirming linear outputs, low glitch energy, and power efficiency. The study demonstrates an efficient approach to compact analog interface design for modern mixed-signal systems.

Keywords: Amplifier, DAC, CMOS, Power.

I. INTRODUCTION

Modern electronic systems rely heavily on digital signal processing, but many real-world applications such as audio, instrumentation, and communication require analog outputs. Digital-to-Analog Converters (DACs) bridge this gap, with the R-2R ladder DAC being one of the most widely used architectures due to its simplicity, scalability, and minimal component requirements. Its ability to generate accurate analog signals from binary inputs makes it suitable for integration in mixed-signal circuits.

To achieve reliable performance, DACs are often combined with operational amplifiers for buffering and gain. CMOS technology is the preferred choice for implementing such analog building blocks because of its low power consumption, high integration density, and compatibility with VLSI systems. This work presents the design and simulation of a two-stage CMOS Op-Amp integrated with 4-bit and 8-bit R-2R DACs using 180nm technology. Simulations performed in Cadence Virtuoso validated DC, AC, and transient performance, confirming linear output, low glitch energy, and power efficiency, thereby making the design suitable for modern embedded and signal processing applications.

II. METHODOLOGY

The two-stage CMOS operational amplifier was chosen over other architectures because it offers an optimal balance between gain, output swing, simplicity, and stability.Implemented in 180nm CMOS technology, the amplifier achieves high gain, wide swing, and reliable performance, making it well-suited for mixed-signal applications. Similarly, the R-2R ladder DAC was selected due to its simplicity, scalability, and efficient implementation using only two resistor values (R and 2R), ensuring compact layout and linear digital-to-analog conversion.

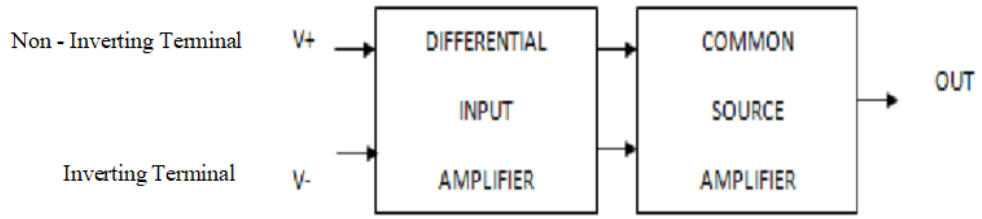

Fig. 1: Block Diagram shows two stage Op-Amp

Using this designed Op-Amp, both 4-bit and 8-bit R-2R ladder DACs were implemented. The Op-Amp serves as the output buffer, ensuring low output impedance, high linearity, and reliable stepwise digital-to-analog conversion. The integration highlights the practical application of the amplifier design in mixed-signal systems.

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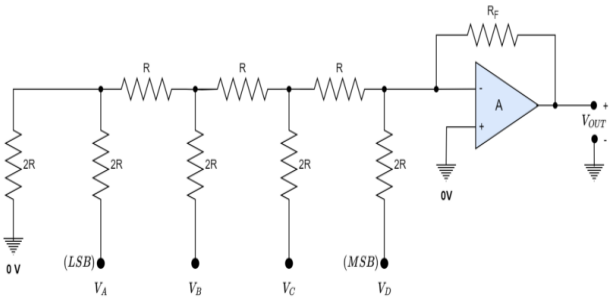

Fig. 2: 4-bit R-2R DAC Design using 2 Stage Designed Op-Amp.

III. DESIGN METHODOLOGY

A. Design of Differential Amplifier (Stage I)

The differential amplifier stage is the first building block of the two-stage operational amplifier. Its purpose is to amplify the difference between two input signals while rejecting any signal common to both inputs (common-mode signals). This enhances the amplifier's accuracy and stability and is critical for driving the next stage of amplification.

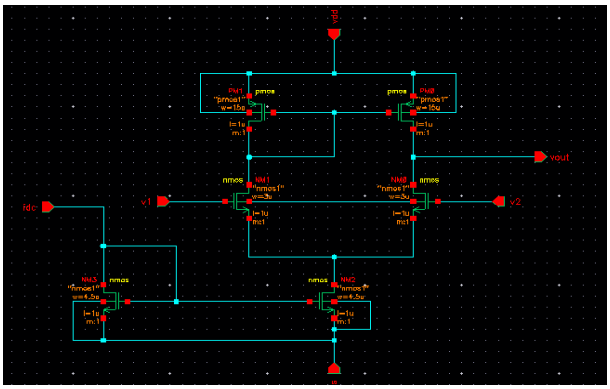

Fig. 3: Design of Differential Amplifier

B. Design of Common Source Amplifier (Stage II)

The second stage of the operational amplifier, known as the common source amplifier, is designed to provide additional voltage gain, wider output swing, and the ability to drive the output load effectively. This stage complements the differential amplifier by ensuring that the signal is sufficiently amplified and prepared for interfacing with subsequent circuit stages or external loads

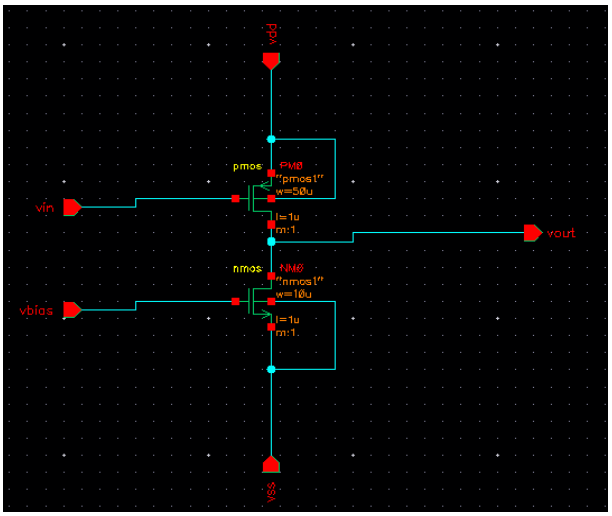

Fig. 4: Design of Common Source Amplifier

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C. Two-Stage Operational Amplifier

The integration of the differential amplifier (Stage I) and the common source amplifier (Stage II) is essential for achieving both high gain and wide output swing in the two-stage CMOS Op-Amp.

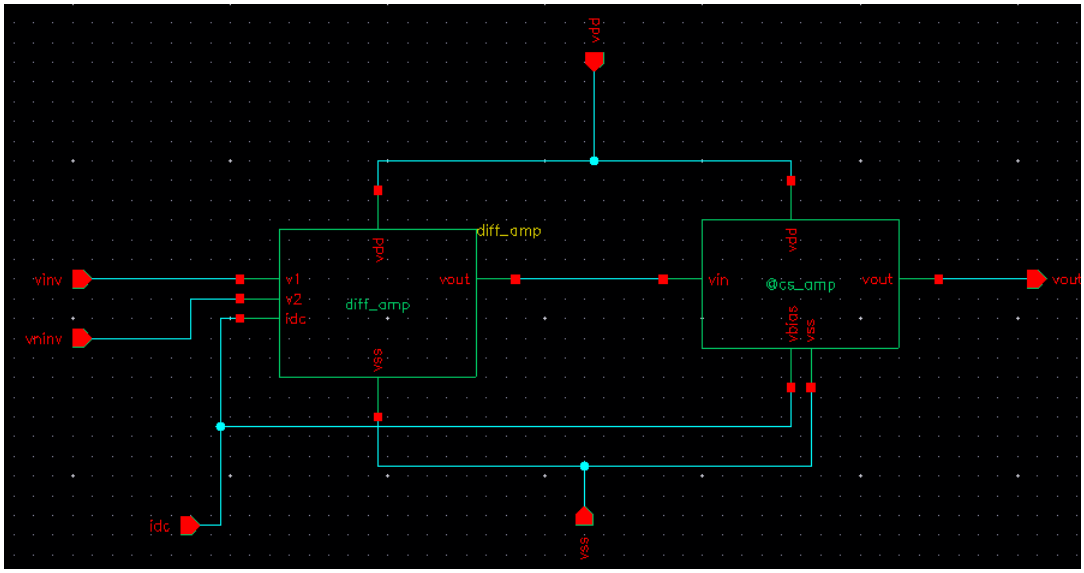

Fig. 5: Two Stage Operational Amplifier – Symbolic Schematic View

D. R-2R Ladder DAC Design

The 4-bit R-2R DAC is implemented using a resistor ladder network consisting of alternating R and 2R resistors. Each digital input controls a switch that connects either to the reference voltage (2V) or ground. The binary-weighted configuration ensures that each bit contributes proportionally to the output voltage, starting from the Most Significant Bit (MSB) to the Least Significant Bit (LSB). The analog output is buffered using the designed two-stage CMOS operational amplifier, which provides high gain, wide output swing, and low output impedance.

The DAC produces 16 discrete output levels, ranging from 0 V (0000) to approximately 1.875 V (1111). The output voltage for a given digital input is expressed as:

$$V_{out} = V_{ref} \cdot \left[\frac{D}{2^4}\right]$$

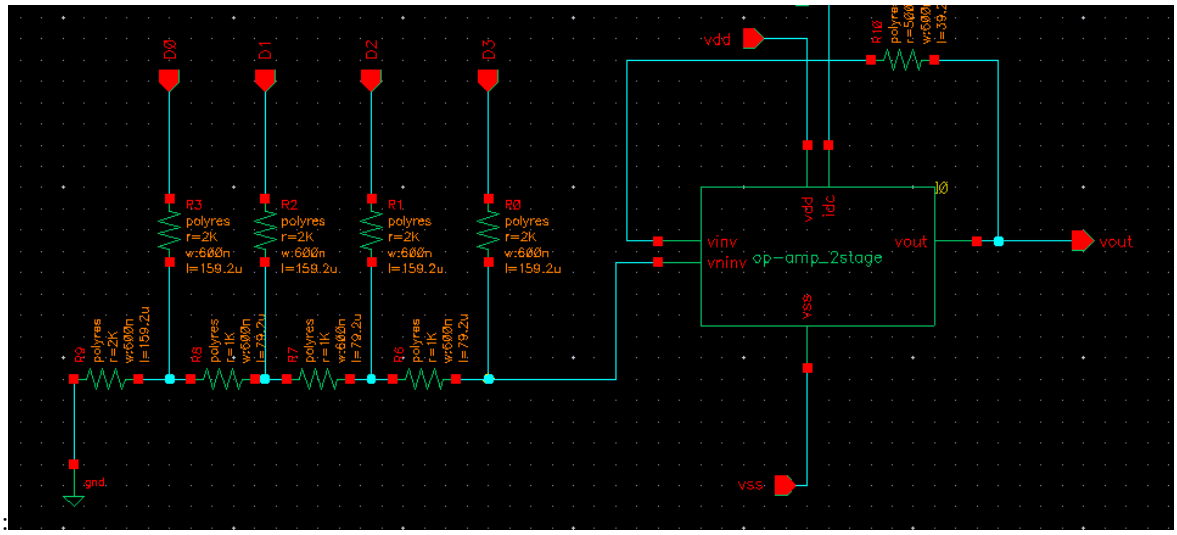

Fig. 6: 4-bit R-2R DAC Design

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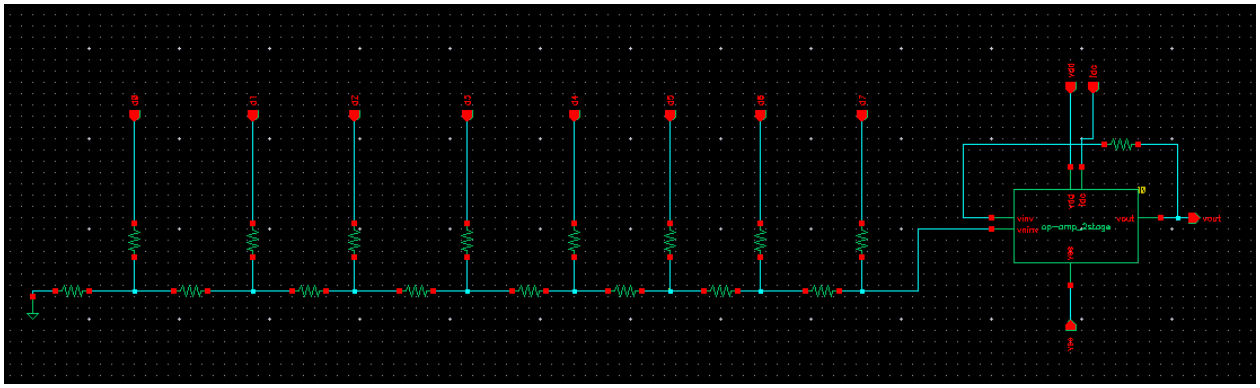

Fig. 7: 4-bit R-2R DAC Design

Also, integrated the 8 bit R-2R ladder with designed Op-Amp. for power consumption analysis w.r.t resolution

IV. RESULTS AND DISCUSSION

A. Simulation of 4 bit R-2R DAC

Discrete voltage levels for each digital input. Confirms correct and glitch-free digital-to-analog conversion.

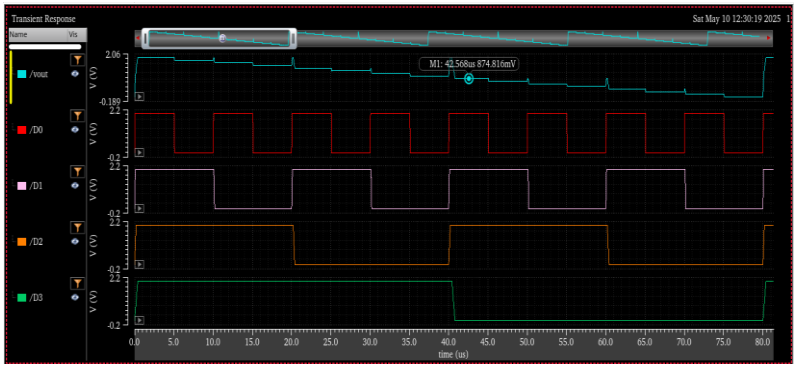

Fig. 7: Transient Analysis of 4 bit R-2R DAC

B. Power Consumption

Power consumption shown in table 8.5.1 in analog blocks like DACs and Op-Amps includes **static** (bias current × supply voltage) and **dynamic** components (due to switching).

Table 1: Power Consumption

Component	Supply Voltage (V)	Typical Power Consumption	Analysis Type
Two Stage Op. Amp.	2.5V	500.7 µW	Transient
4 bit DAC	Vref = 2V	2.102 mW	Transient
8 bit DAC	Vref = 2V	3.411 mW	Transient

i. **4-bit DAC**: Lower power due to fewer resistors and switches.
ii. **8-bit DAC**: Higher power from increased switching and resistor count.
iii. **Op-Amp**: Power depends on biasing, gain-bandwidth, and load.
In general, power increases with resolution, load, and speed.

Power Consumption vs. Resolution

A comparison of the 4-bit and 8-bit DACs demonstrates the trade-off between resolution and power consumption. The 4-bit DAC consumes approximately 2.102 mW, while the 8-bit DAC requires 3.411 mW under identical simulation conditions. This increase is attributed to the higher number of switches and resistors in the ladder network, leading to increased switching activity and current flow. Despite this, the improved resolution of the 8-bit DAC makes it suitable

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for precision applications such as waveform synthesis and audio signal processing, whereas the 4-bit DAC is more suited to low-power, coarse-resolution systems.

V. CONCLUSION

This work demonstrated the design and simulation of a two-stage CMOS operational amplifier integrated with R-2R ladder DACs in 180nm technology. The amplifier, consisting of a differential input stage and a common-source gain stage, achieved high gain, stability, and wide output swing. The integration with 4-bit and 8-bit DAC architectures provided accurate stepwise digital-to-analog conversion.

Simulation results using Cadence Virtuoso and Spectre confirmed linear output behavior, low glitch energy, and power efficiency. The study highlights the effectiveness of CMOS technology for compact, low-power mixed-signal interfaces and provides a solid foundation for extending the design to higher resolutions, optimized layouts, and real-world SoC implementations.

REFERENCES

[1]. A. Bandyopadhyay, S. Kumar, R. Roy, and M. Sen, “Design and Simulation of 4-bit R-2R Ladder DAC using CMOS,” *International Journal for Research in Applied Science and Engineering Technology*, vol. 8, no. 5, pp. 1234–1238, May 2020.

[2]. N. Ayyanar and T. Shree Harsha, “A Low-Power High-Speed CMOS Op-Amp for Mixed-Signal Applications,” *International Journal of VLSI Design and Communication Systems*, vol. 12, no. 2, pp. 45–50, Apr. 2021.

[3]. R. P. Singh and S. J. Patel, “Analysis and Design of R-2R Ladder DAC using CMOS Technology,” in *Proc. IEEE Int. Conf. on Emerging Trends in Engineering and Technology*, 2022.

[4]. P. N. Verma and A. P. Yadav, “Design of a High-Speed Operational Amplifier in 180nm CMOS Technology,” *International Journal of Electronics and Communications*, vol. 136, pp. 123–129, Mar. 2021.

[5]. J. Diosanto, A. B. Bacus, R. A. Napone, and M. C. Clemente, “4-bit Digital to Analog Converter using R-2R Ladder and Binary Weighted Resistors,” *IOP Conf. Series: Earth and Environmental Science*, vol. 69, no. 1, p. 012194, 2017.

[6]. T. Yuan and Q. Fan, “Design of Two-Stage CMOS Operational Amplifier in 180nm Technology,” *arXiv Preprint*, arXiv:2012.15737, Dec. 2020.