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POWER CONSUMPTION COMPARISON OF COVENTIONAL AND SINGLE-ENDED 6T SRAM CELL USING CMOS

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Abstract: This project focusses on analysing memory systems' power usage utilising both single-ended and typical 6T SRAM cells. SRAM, or static random-access memory, is crucial for contemporary computer systems where power efficiency is a top priority. The traditional 6T SRAM cell uses a differential read method, which increases power consumption while offering great stability. The single-ended 6T SRAM cell, on the other hand, has a simpler read operation, which drastically lowers layout complexity and power consumption. The power dissipation of the two systems is assessed and compared in this study using simulation-based techniques. The results emphasise the limitations in power efficiency, showing that traditional 6T SRAM may be more appropriate for situations where power consumption is less crucial, while single-ended 6T SRAM cells are more suited for power-sensitive applications like low-power Internet of Things devices.

Keyword: SRAM Power Analysis, 6T SRAM Cell, Single-Ended SRAM, Low-Power Memory Design.

I. INTRODUCTION

Memory is crucial for computers, enabling them to store data and instructions, functioning similarly to a human brain. Memory devices are digital systems that store data, either temporarily or long-term, and require large, cost-effective capacities. Memories are structured into cells, each residing in a storage location with a unique address. A register represents a storage location, and the total bits a memory can hold defines its capacity. A cell stores a single bit of data, and data is managed through writing (storing) and reading (retrieving) processes.

A word is a group of bits where a memory unit stores binary information. A word with a group of 8 bits is called a byte. A memory unit consists of data lines, address selection lines, and control lines that specify the direction of transfer. The block diagram of a memory unit is shown below in figure 2

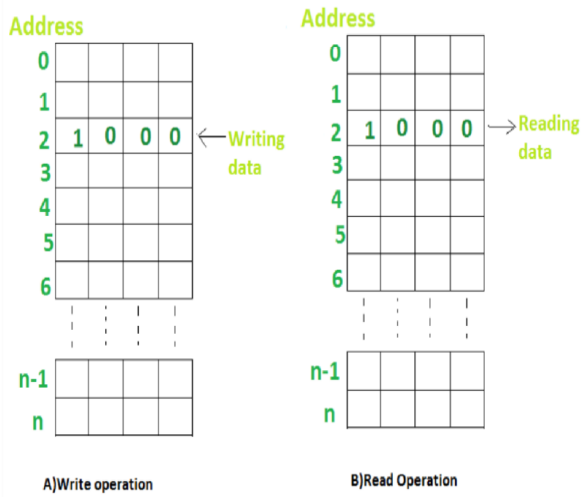

Figure 1 Write and Read operation

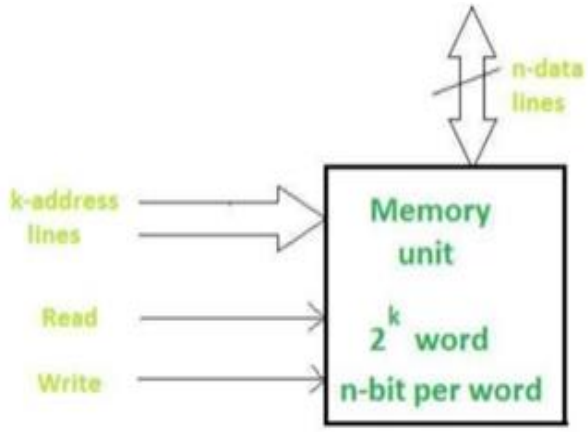

Figure 2 Memory

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II. OBJECTIVES

The objectives of the project are:

- To design and simulate a conventional 6T SRAM cell and a single-ended 6T SRAM cell.
- To evaluate and compare the power consumption of both SRAM cell designs.

III. METHODOLOGY

A. Conventional 6T SRAM Cell

A common memory component in digital systems, particularly for processor cache memories, is a typical 6T SRAM cell. "6T" refers to the six transistors that make up the memory cell. Due to its balanced power efficiency, this design is widely used in contemporary microelectronics. Structure of a 6T SRAM Cell: The 6T SRAM cell is composed of:

1. Two Cross-Coupled Inverters (4 Transistors): A feedback loop connecting two CMOS inverters makes up the SRAM cell's core. To create these inverters, two PMOS and two NMOS transistors are used. By establishing a bistable circuit, the cross-coupling enables the cell to hold a logical "1" or "0."

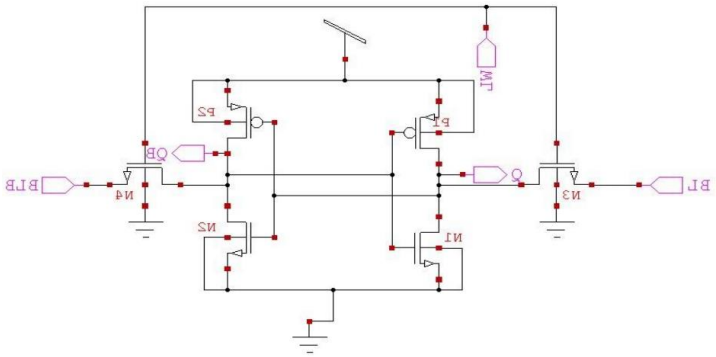

Figure 3 Schematic of Conventional 6T SRAM Cell circuit

2. Two Access Transistors: For read and write operations, the cell is connected to the bit-lines by the two NMOS transistors that remain. The word-line (WL) signal that controls these transistors establishes whether the cell is active.

Operation of Conventional 6T SRAM Cell

1. Write Operation: The word-line (WL), which activates the access transistors, is used to store data in the SRAM cell. The bit-line (BL) and its complement ($B\overline{L}$) are driven with the necessary data. The data is latched by the cross-coupled inverters according to the voltage levels of BL and $B\overline{L}$.

If BL = 1 and $B\overline{L}$= 0, the node Q is set to 1, and $\overline{Q}$ is set to 0.If BL = 0 and $B\overline{L}$= 1, the node Q is set to 0, and $\overline{Q}$ is set to1.

2. Read Operation: To retrieve the stored data: The word-line (WL) is activated, enabling the access transistors.

The stored value at Q is transferred to the bit-line (BL), while its complement ($\overline{Q}$) affects $B\overline{L}$. A sense amplifier connected to the bit-lines detects the voltage difference between BL and $B\overline{L}$ to determine the stored bit.

3. Hold Operation: When no read or write operation is occurring-

The word-line (WL) is deactivated, turning off the access transistors. The feedback loop in the cross-coupled inverters keeps the data latched, ensuring that the cell retains its state.

B. Single Ended 6T SRAM Cell

A variant of the traditional 6T SRAM cell, the single-ended 6T SRAM cell is made especially to use less power. This is achieved by use a single bit line (BL) rather than two complementary bit lines (BL and $B\overline{L}$). Although this simplification lowers complexity, it also adds special performance and stability design issues.

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Structure of a Single-Ended 6T SRAM Cell: The core structure of a single-ended 6T SRAM cell is similar to the conventional 6T SRAM cell, with the following key components:

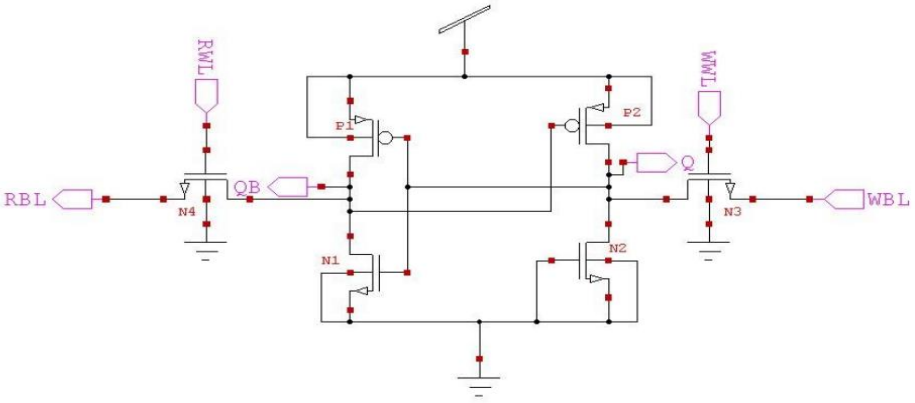

Figure 4 Schematic of Single-ended 6T SRAM

1. Cross-Coupled Inverters (4 Transistors): Two CMOS inverters, consisting of two PMOS and two NMOS transistors, are cross-coupled to form a bistable circuit. This configuration ensures that the cell retains its data as long as power is supplied.

2. Access Transistors (2 Transistors): Two NMOS transistors act as access transistors, controlled by the word-line (WL) signal. These transistors connect the storage nodes of the cell to the bit line (BL) for read and write operations.

3. Single Bit line (BL): Unlike the conventional design, which uses both BL and $B\overline{L}$, the single-ended cell uses only one bit line, reducing the overall wiring complexity and area.

Operation of Single ended 6T SRAM Cell

1. Write Operation: Writing data into a single-ended 6T SRAM cell involves activating the word-line to enable access transistors, driving the bitline to the desired logic level (high for '1', low for '0'), and allowing the cross-coupled inverters to latch the data, thus setting one storage node to the input logic level and the complementary node to its inverse.

2. Read Operation: In a single-ended 6T SRAM cell, the read operation employs a single bitline (BL) as there is no complementary bitline ($B\overline{L}$). Activation of the word-line (WL) enables access transistors, which transfer the voltage from node Q to the BL. A sense amplifier then determines the stored value by comparing the BL voltage to a reference voltage, with accuracy relying on the sense amplifier's sensitivity to small voltage changes.

3. Hold Operation: When no read or write operations are being performed, the word-line (WL) remains deactivated. The cross-coupled inverters maintain the state of the cell, ensuring data retention.

C. Flow Chart

The methodology details the design and power optimization of SRAM cells using CMOS technology. It covers the design of a standard six-transistor (6T) SRAM cell, including its logic schematic for data storage and read/write operations. Additionally, a single-ended 6T SRAM cell was developed to simplify design and improve power efficiency during read cycles. Power analysis was performed on both designs to compare their energy consumption in read, write, and hold states, identifying the more power-efficient option.

Power analysis is a crucial step in evaluating the performance of digital and analog circuits, particularly in memory design such as SRAM. In this project, power analysis was performed to measure and compare the power consumption of both conventional 6T and single-ended 6T SRAM cells designed using CMOS technology.

The analysis was carried out using the Cadence Virtuoso Design Environment with the Spectre simulator. A testbench was developed to simulate read, write, and hold operations of the SRAM cells. Transient analysis was used to capture dynamic behavior and calculate power consumption during these operations. This power analysis helped determine the more power-efficient SRAM design and provided insights for optimization in low-power applications.

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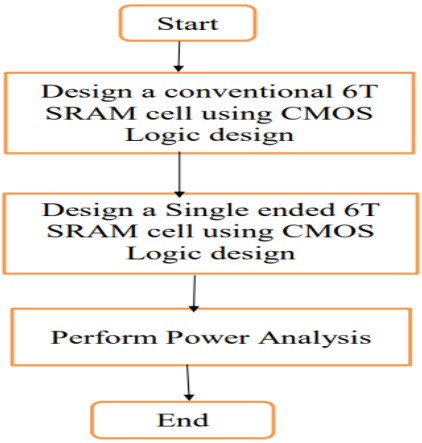

Figure 5 Flow Chart

Table 1: Comparison with Conventional 6T SRAM Cells and Single-Ended 6T SRAM Cell

Feature	Conventional 6T SRAM	Single-Ended 6T SRAM
Bitline Configuration	Differential (BL, $\overline{BL}$)	Single (BL)
Area Efficiency	Lower	Higher
Power Consumption	Higher	Lower
Read Speed	Faster	Slower

IV. TOOLS AND TECHNOLOGIES

4.1 Cadence Virtuoso Tool Steps

Step 1: Right click on created folder → open in terminal.

Step 2: Edit → [viii sem@cad24 px06] $ csh → source/home/install/cshrc → Virtuoso

Step 3: The Virtuoso environment is opened → file → new → library → Write Library Name: sram click on attach to → an existing technology → click on apply → attach library to Technology Library → select GPDK 45 →click on apply → ok.

Step 4: file → new → cellview → browse library →create cellview → click ok

Step 5: schematic editor window will opened → click on 'I' add instance→ browse a library → select gpdk 45→ select nmos and cmos transistor→ add specifications→ drag the nmos and pmos transistor.

Step 6: Wire all the transistor nodes as per the circuit diagram.

Step 7: click on 'p' in keyboard → give a pin names like vdd, vpulse, q q' b b' gnd → give a direction of pins like input or outputs → connect it.

Step 8: check and save all

Step 9: launch → ADEL → Analog design environment window will open → choosing analysis → dc → select save DC operating point→ select component parameter option → choose a component parameter in circuit diagram → dc vdc "dc voltage" → ok

Step 10: Analog design environment window → go to output, select to be plotted →select on schematic → click on input side wire and output side wire → click on run button → get a waveform.

4.2 Software tool

Software tool used is Cadence Tools for Functional Simulation: Incisive Simulator

The Incisive simulator from Cadence is employed for functional verification of digital designs described in Verilog HDL. The process involved setup and configuration, including design entry and testbench development with stimulus generation, response checking, and coverage collection. Execution entailed running simulations to verify functional correctness under specified conditions. Results analysis focused on examining waveforms and logs for debugging and generating functional coverage reports to confirm thorough testing.

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V. RESULTS AND DISCUSSION

5.1 Conventional 6T SRAM Cell Schematic Diagram:

The write driver waveform illustrates the process by which data is impressed onto bitlines (BL and BLB) during an SRAM write operation. Upon activation by a write enable signal, the write driver circuit drives one bitline to VDD and the complementary bitline to ground, corresponding to the input data logic (0 or 1), thereby overwriting the SRAM cell's existing content. This waveform is crucial for understanding how the write driver, a key SRAM peripheral composed of transistors, manages bitline voltage levels to ensure accurate data writing, using complementary bitlines in conventional 6T SRAM and a single bitline in single-ended 6T SRAM.

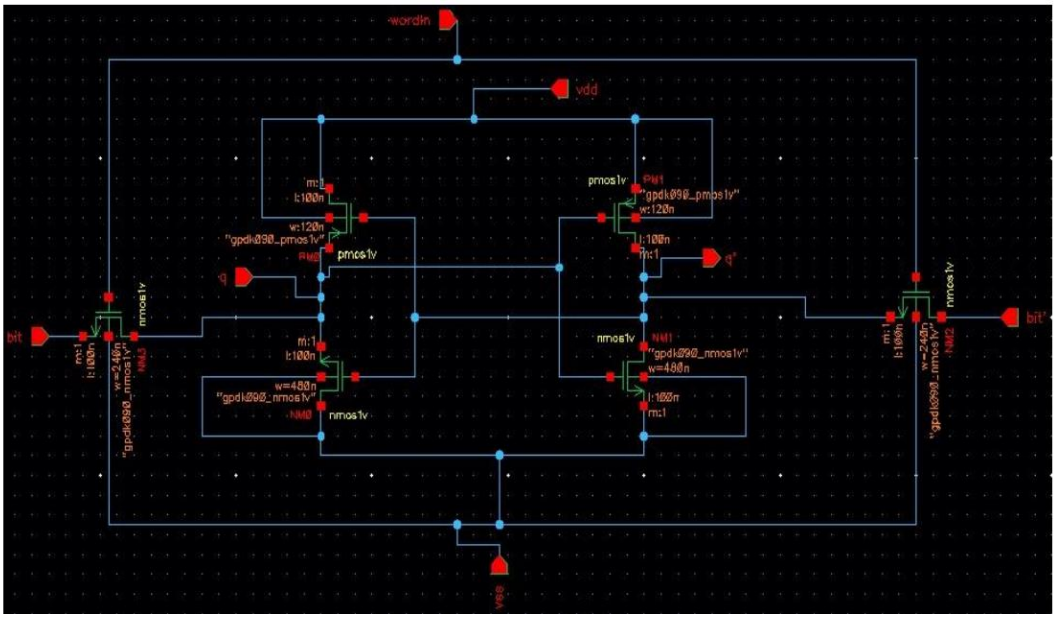

Figure 6 Conventional 6T SRAM Cell schematic circuit

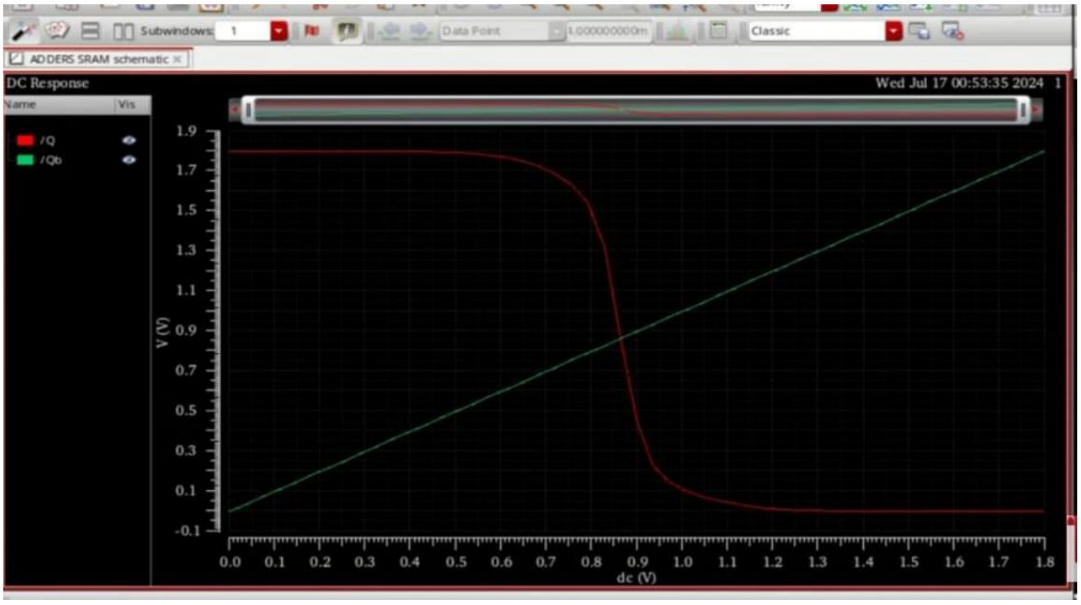

Figure 7 Wave form of conventional 6T sram cell

Optimizing SRAM write driver circuits is essential for improving system performance, balancing speed and power efficiency by adjusting transistor drive strength or using current-limiting techniques. In conventional SRAM, driver optimization can reduce cross-talk and write assist needs, while single-ended SRAM requires sufficient voltage swing without sacrificing stability. Techniques such as delayed write drivers or write assist circuits enhance reliability by

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preventing data corruption during write operations. Write driver optimization also affects SRAM cell power, speed, area, and scalability.

5.2 Single Ended 6T SRAM Cell schematic Diagram

This document describes the design and simulation of a 6-transistor (6T) Static Random-Access Memory (SRAM) cell using Cadence Virtuoso. The cell consists of two cross-coupled inverters made of PMOS and NMOS transistors that store a single bit at internal nodes (/Q and /QB). Two NMOS access transistors, activated by word lines (WWL and RWL), connect these internal nodes to bit lines (WBL and RBL) for read/write operations. The cell is designed for 1.8V operation, employing CMOS principles for low power and high noise margins for stable performance.

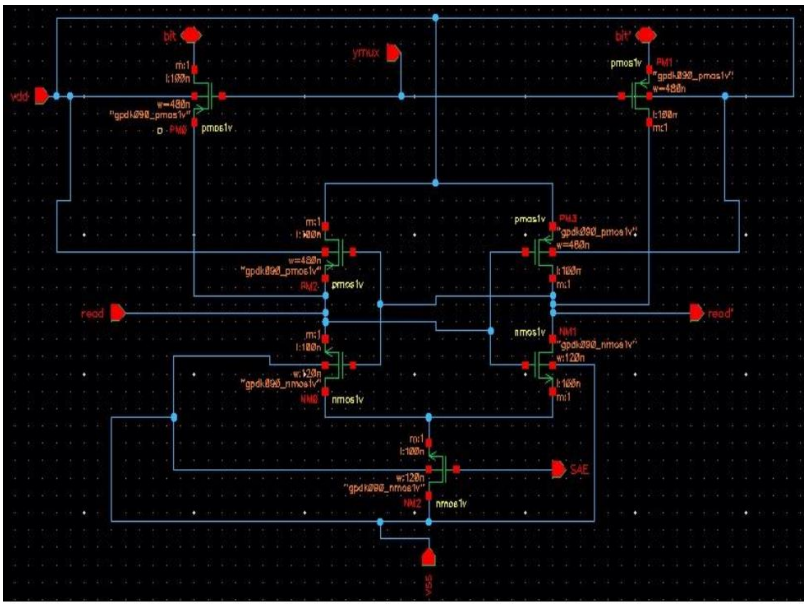

Figure 8 Single ended 6T SRAM Cell schematic circuit

Figure 9 Waveform of single-ended 6T SRAM cell

A DC analysis simulation using Virtuoso Visualization & Analysis XL was performed to examine SRAM cell node voltages (/Q and /QB) and power consumption during a control voltage sweep. The results demonstrate the bistable latch's stable high/low states and slight variations in static power consumption with input voltage changes. This simulation

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verifies the SRAM cell's correct static behavior, logic levels, stability, and power characteristics, essential for reliable operation in larger memory arrays and pre-physical implementation design assessment.

Table 2 Power consumption table of SRAM Cell

SL.NO	SRAM cell	Total power(microW)
1	Conventional 6T SRAM cell	101
2	Single ended 6T SRAM cell	82.43

VI. APPLICATION

Application of Conventional 6T SRAM Cell

1. CPU Cache Memory: Most common use-case. 6T SRAM offers the high speed and low latency required for fast instruction and data access.
2. Buffer and Register Files in Processors: Used for register files in CPUs, GPUs, and DSPs. Efficient read/write access is essential for high-performance computation.
3. Mobile Devices: Cache in application processors where high speed and low leakage are essential.
4. Embedded Systems: For storing frequently accessed data or instructions. Reduces latency compared to using off-chip memory.

Application of Single Ended 6T SRAM Cell

1. Low-Power Embedded Systems: Used in microcontrollers and IoT devices where minimizing power and area is more critical than speed. Some of the examples are : wearable electronics, smart sensors.
2. Biomedical Devices: Suitable for on-chip memory in implantable and wearable medical devices where ultra-low power is required.
3. Read-Mostly Applications: Ideal where write frequency is low compared to reads (since write performance is typically weaker than in differential SRAM).

VII. ADVANTAGES

Advantages of Conventional 6T SRAM Cell:

1. High Speed: Read and write operations are very fast, making it ideal for CPU cache memory.
2. Low Power Consumption (during standby): It consumes very little power when idle because it retains data statically (no refresh needed like DRAM).
3. No Refresh Required: Unlike DRAM, SRAM does not need periodic refresh cycles, simplifying control circuitry.
4. Scalability: With proper design, 6T SRAM cells can be scaled to smaller technology nodes while maintaining performance.
5. Simple Operation: Uses well-understood circuitry (two cross-coupled inverters and two access transistors), making it easy to analyze and optimize

Advantages of Single Ended SRAM Cell:

1. Lower Power Consumption: Fewer switching nodes (single bit line), reducing dynamic power during read/write. Sense amplifier design is simpler and more energy-efficient.

VIII. LIMITATIONS

Limitations of Conventional 6T SRAM Cell are

1. Reduced Stability at Lower Supply Voltages: Read/Write Stability suffers at low VDD due to smaller noise margins. Can lead to data corruption, especially in advanced nodes ($\leq$ 7nm).
2. Poor Scalability: Difficult to scale below certain technology nodes due to leakage, variability, andshort-channel effects. Increased sensitivity to process variations affects reliability and yield.
3. Read Disturb Problem: During a read operation, the stored data can be unintentionally flipped due to voltage drop at the internal node (read disturb).

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Limitations of Single-Ended 6T SRAM Cell are

1. Reduced Read Stability: During a read, the internal node storing '0' is directly connected to the bit-line, which can disturb the stored value (known as read disturb).
2. Slower Read and Write Speed: Sense amplifier must detect smaller voltage swings on a single bit-line, making read slower. Write operation is also less effective due to reduced driving strength.
3. Read and Write Conflict: Since the same path is used for reading and writing, there's a higher chance of contention or conflict, especially without proper isolation techniques.

IX. FUTURE SCOPE

1. Integration with Advanced Technology Nodes: Investigate the performance of conventional and single-ended 6T SRAM cells in sub-10 nm or FinFET technologies to address challenges like increased leakage currents and variability. This will help ensure their applicability in future-generation process nodes.
2. Adaptive Power Management: Implement dynamic power management techniques, such as adaptive voltage scaling, to further reduce energy consumption based on workload requirements, particularly for single-ended SRAM cells.
3. Error Correction and Reliability: Add error correction mechanisms like ECC (Error Correction Code) to enhance reliability, especially in single-ended designs, which might be more susceptible to noise and soft errors.
4. Mixed-Cell Architectures: Develop hybrid memory arrays that combine conventional 6T and singleended 6T SRAM cells. Such architectures can allocate high-speed cells for critical data and low-power cells for less frequently accessed information.

X. CONCLUSION

The Cadence Virtuoso tool is used in this project to simulate. The 45nm technology node's 6T SRAM cell is simulated. Analysis of the simulation and results is done in terms of power dissipation. The power consumption of a typical 6T SRAM cell is 101 microwatts. The power consumption of a single ended 6T SRAM cell is 82 microwatts. Single ended SRAM cells can be utilised to create memory systems since they use less power and are simpler of 16-, 32-, 64-, and so forth.

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