

DESIGN OF BANDGAP VOLTAGE REFERENCE CIRCUIT

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Abstract: The project focuses on designing and simulating a Bandgap Voltage Reference (BGR) circuit using 180nm CMOS technology to achieve a temperature-independent and precise voltage reference. This is crucial for reliable operation of analog and digital components. The design uses Complementary-To-Absolute-Temperature (CTAT) and Proportional-To-Absolute-Temperature (PTAT) characteristics to cancel out temperature effects and generate a constant reference voltage. The circuit is suitable for various applications, including Analog-to-Digital Converters, voltage regulators, temperature sensors, and battery-operated systems. The work not only demonstrates temperature compensation techniques but also enhances understanding of analog circuit behaviour under real-world conditions.

Keywords: Cadence, simulation, circuit, voltage.

I. INTRODUCTION

The bandgap voltage reference circuit is a widely used solution for maintaining a stable and accurate voltage reference in analog and mixed-signal integrated circuits. Traditional voltage reference circuits are sensitive to temperature variations, causing errors and reducing system reliability. The bandgap reference combines two voltage components with opposite temperature coefficients, PTAT and CTAT, to produce a reference voltage independent of temperature. This project focuses on implementing the bandgap reference using the current mirror technique, which improves accuracy and temperature stability of the reference voltage and simplifies its integration into modern CMOS technologies. The design methodology, implementation, and analysis of the bandgap voltage reference circuit using current mirrors are detailed, with a focus on temperature compensation and parameter optimization to achieve minimal voltage drift over a wide temperature range. DC analysis using Cadence Virtuoso is also included to validate the circuit's temperature independence and overall performance.

II. OBJECTIVES

The objectives of the project are:

- To design a bandgap voltage reference circuit using current mirror techniques that provides a stable and temperature-independent output voltage.
- To validate and optimize the circuit's temperature performance across 40°C to 125°C through DC analysis using Cadence Virtuoso.

III. METHODOLOGY

A. BLOCK DIAGRAM

The block diagram of the bandgap voltage reference circuit which illustrates the systematic flow from conceptual design, ensuring a robust and temperature-independent output voltage.

1. Design and Optimization: The CMOS-based schematic uses optimized device sizes and resistor values to balance PTAT and CTAT effects. Advanced techniques like genetic algorithms and deep learning help minimize the temperature coefficient (TC) of the reference voltage. Structural design methods also ensure low power and compact circuit implementation.

2. Simulation and Performance Analysis: After the initial design, the circuit is modelled and simulated in Cadence Virtuoso. DC analysis and temperature sweeps help evaluate performance across -40°C to 125°C. Component values are adjusted, and any issues are resolved through iterative refinements to ensure output voltage stability.

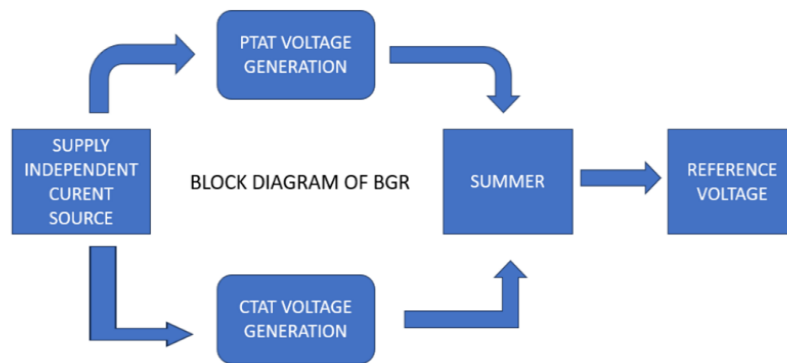


Figure 1 Block diagram

3. Layout and Parasitic Extraction: After schematic validation, the circuit is carefully laid out to minimize mismatches and parasitic. Techniques like common-centroid layout and precise routing are used to improve accuracy, and post-layout simulations ensure performance is maintained.

4. Final Validation: The final validation includes thorough testing of the integrated circuit to ensure minimal temperature coefficient and stable, accurate reference voltage. This confirms that the PTAT, CTAT, current mirror, and summing network function effectively together, producing a reliable bandgap reference ideal for precision analog and mixed-signal applications.

B. FLOW DIAGRAM

This flow chart ensures a systematic approach to the design, simulation, and validation of a temperature-independent bandgap voltage reference circuit, as supported by established methodologies in the literature.

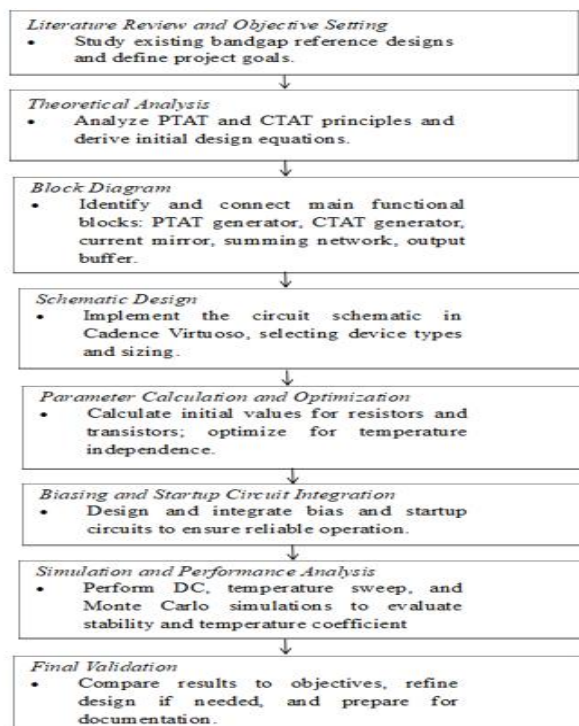


Figure 2 Flow Chart of Voltage Reference Circuit

IV. IMPLEMENTATION DETAILS

The section presents the practical realization of a temperature-independent bandgap voltage reference, detailing the system specifications, circuit architecture, and the step-by-step implementation and validation process in 180 nm CMOS technology.

4.1 Specification and System Architecture

The bandgap reference circuit, built using a 180 nm CMOS process, offers a good balance of performance, integration, and low power—suitable for precision analog and mixed-signal use. It operates over -40°C to 125°C with a 3.3 V supply, generating a ~ 1.2 V reference voltage aligned with the silicon bandgap. The design is optimized for high PSRR, low temperature coefficient, and compact area.

- 180 nm CMOS technology is the technological node.
- Operating Temperature Range: -40°C to 125°C.
- Nominal Supply Voltage (VDD) of 3.3 V.

Table 1 Specification and System Architecture Table

PARAMETER	VALUE
Reference Voltage	1.2 V
Technology	180 nm
Temperature Range	−40°C to 125°C
Power Supply (VDD)	3.3 V

4.2 Final System Architecture

The bandgap reference circuit architecture integrates several key functional blocks to achieve temperature-independent voltage output with high precision:

1. Proportional To Absolute Temperature (PTAT) Generator

This block generates a voltage (or current) that increases linearly with absolute temperature. It is typically implemented using the difference in base-emitter voltages (ΔV_{BE}) of bipolar junction transistors (BJTs) operating at different current densities. The PTAT behaviour is leveraged to cancel out the negative temperature dependence of the base-emitter voltage (V_{BE}), which is a Complementary To Absolute Temperature (CTAT) component.

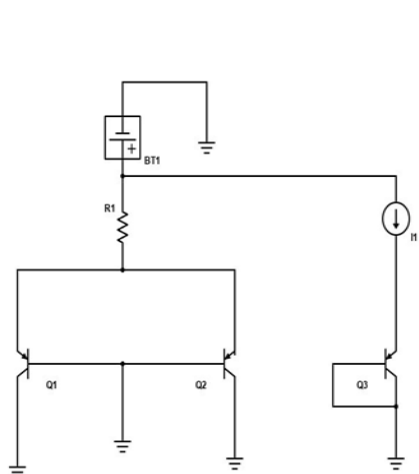


Figure 3 PTAT Generation Circuit

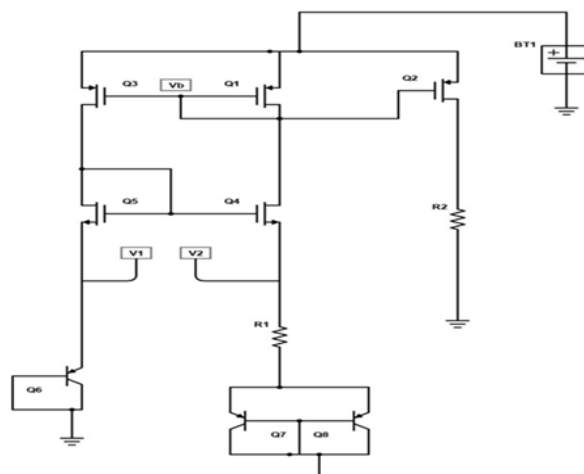


Figure 4 PTAT Generation using current mirror

Fig. 3 shows the PTAT circuit typically shows two BJTs operating at different current densities, generating a ΔV_{BE} that increases linearly with temperature.

The diode voltage equation is given by: $V_d = V_t \ln (I_o/I_s)$

Where V_D is the diode voltage, V_T is the thermal voltage, I_0 is the diode current, and I_S is the reverse saturation current. Here V_T is PTAT voltage \ln denotes the CTAT voltage.

To minimize the impact of the CTAT voltage in PTAT voltage generation, the reverse saturation current (I_S) must be reduced or removed. In the equation $V_D - V_{D1} = V_T \ln(n)$, the term $V_T \ln(n)$ reflects the thermal voltage scaled by the natural log of the diode count, representing the voltage difference between two diodes.

To equate the voltages V_D and V_{D1} , current mirror approach can be utilized.

Figure 4 shows the above approach involves using a cascade current mirror, which can provide an exact same current, ensuring V_D and V_{D1} are equal. Now the voltage across R_2 will be PTAT.

2. Complementary To Absolute Temperature (CTAT) Generator

Produces a voltage that decreases with temperature, primarily derived from the V_{BE} of a BJT. The CTAT component, which has a negative temperature coefficient, forms the baseline for generating a bandgap reference. The combination of PTAT and CTAT voltages yields a zero-temperature-coefficient output when scaled correctly.

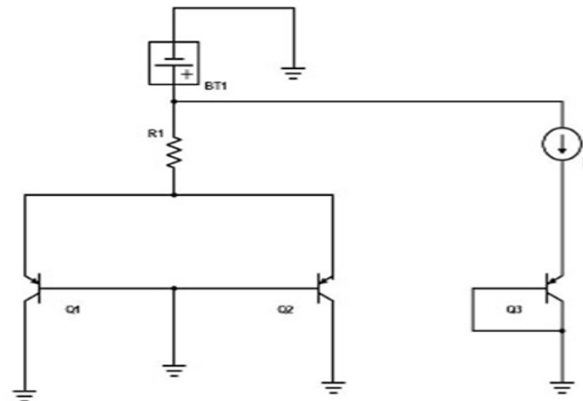


Figure 5 CTAT Generation Circuit

A forward-biased PN junction diode's voltage drop is what is known as the CTAT voltage, as was previously stated. The following is the diode current equation:

$$I_0 = I_{se} - V_d/V_t$$

The diode current (I_0) depends on device parameters, with the reverse saturation current as the scale factor. V_T is the thermal voltage, and V_D the forward voltage drop, acts as a CTAT voltage, decreasing by about $-1.6 \text{ mV}/^\circ\text{C}$ when a constant current is applied.

3. Current Mirror

Ensures precise replication of currents within the circuit, critical for maintaining accurate scaling between the PTAT and CTAT voltages. Typically implemented using MOSFET current mirrors that copy and bias the currents through the temperature-dependent elements. The performance of this block directly affects the linearity, stability, and matching characteristics of the reference.

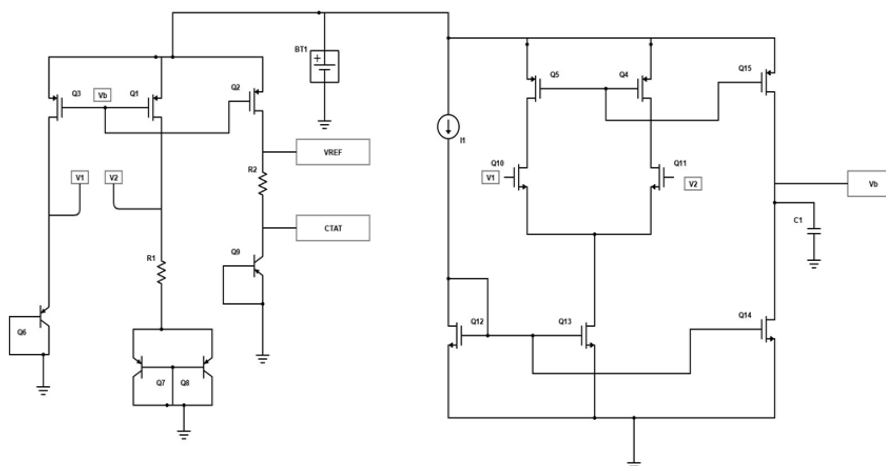


Figure 6 Bandgap Reference Circuit

In the current mirror setup, the CTAT voltage appears at node V_D , and a PTAT voltage across R_1 is mirrored to the next branch. A diode-connected PNP transistor combines PTAT and CTAT to generate V_{ref} . Resistors R_1 and R_2 help scale the

PTAT voltage to offset CTAT and temperature effects. Although only two PNP transistors are shown for simplicity, more can be added.

V. SOFTWARE DESCRIPTION

The temperature-independent bandgap reference circuit was designed, simulated, and validated using Cadence Virtuoso. Its accurate modelling of CMOS and BJT devices ensured stable reference voltages across temperature and process variations.

5.1 Overview of the tool: Cadence Virtuoso

Cadence Virtuoso was used to design and analyse the temperature-compensated bandgap reference circuit. Key features included: Temperature & Process Sweeps: Ensured reliable performance from -40°C to 125°C and across process variations. Parameter Optimization: Tuned resistor ratios and transistor sizes to minimize the temperature coefficient. Spectre Simulation: Enabled accurate SPICE-level modelling of transistor behaviour and circuit performance. Figure 7 shows Each component was configured with proper dimensions (transistors) and connected to form a complete analog subsystem. The schematic editor shown in figure 7 supports hierarchical design.

5.2 Virtuoso Analog Design Environment (ADE)

ADE in Cadence is used to set up and run simulations. It was used to verify DC operating points, perform temperature sweeps (-40°C to 125°C), run Monte Carlo simulations for mismatch analysis, and optimize resistor ratios through parameter sweeps.

5.3 Spectre Simulation Engine

Spectre provided high-accuracy simulations for Bandgap Core: Modelling BJT non-idealities (e.g., Early effect, leakage currents). Temperature Coefficient (TC): Calculated as V_{ref} as shown in figure 9.

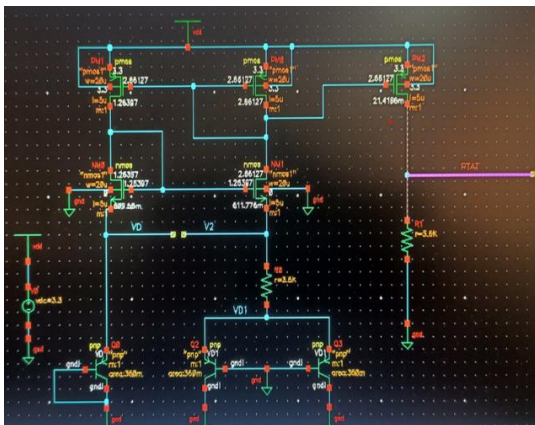


Figure 7 Virtuoso Schematic Editor Window

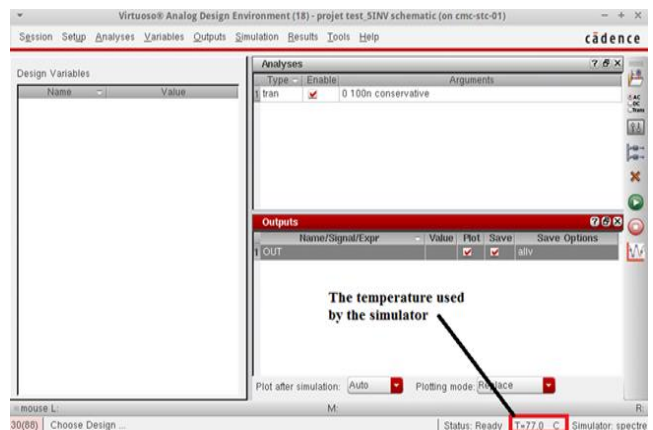


Figure 8 Virtuoso Analog Design Environment Window

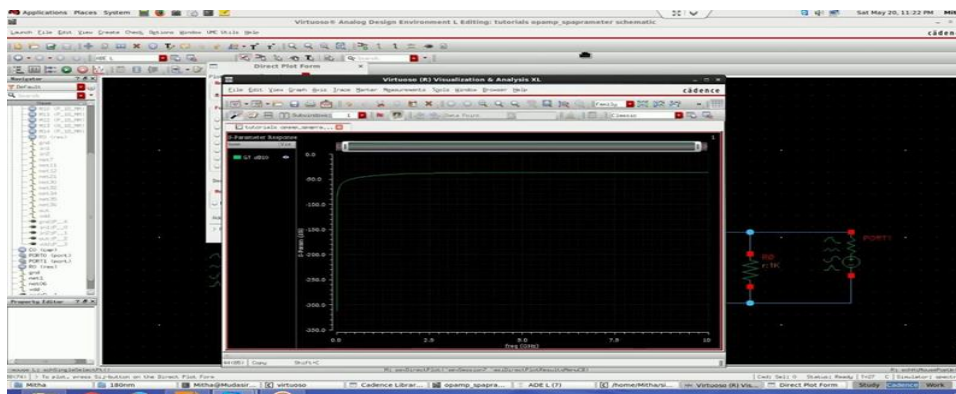


Figure 9 Spectre Simulation Engine

VI. RESULTS AND DISCUSSION

The BGR (Bandgap Voltage Reference) circuit consists of CTAT and PTAT blocks, which combine to produce a temperature-independent reference voltage. Their performance, along with the complete BGR, is analysed using simulation schematics and DC plots.

6.1 CTAT Circuit Results

The CTAT block uses a diode-connected PNP BJT biased by a constant current to operate in the active region. Its base-emitter voltage (V_{BE}) decreases with temperature, exhibiting CTAT behaviour.

Key Observations are: As temperature increases, the increase in intrinsic carrier concentration causes the saturation current to increase exponentially. This results in a logarithmic decrease in the base-emitter voltage V_{BE} , which is clearly depicted in the DC response. The CTAT output is hence useful for cancelling the positive temperature coefficient of the PTAT component.

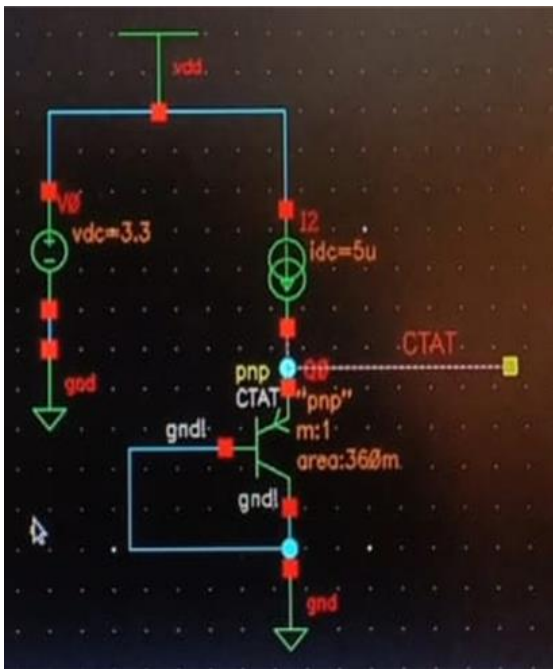


Figure 10(a)

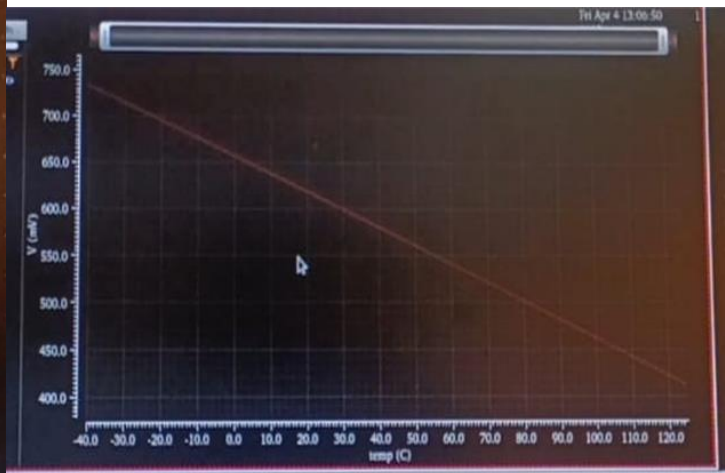


Figure 10(b)

Figure 10(a) shows the schematic of the CTAT circuit. Figure 10(b) illustrates the DC response of the CTAT circuit.

6.2 PTAT Circuit Results

The PTAT (Proportional to Absolute Temperature) circuit produces a current that increases linearly with temperature using the ΔV_{BE} between two BJTs. This voltage is applied across a resistor to generate a PTAT current, which is mirrored for biasing. The positive temperature coefficient helps offset CTAT behaviour, ensuring temperature stability.

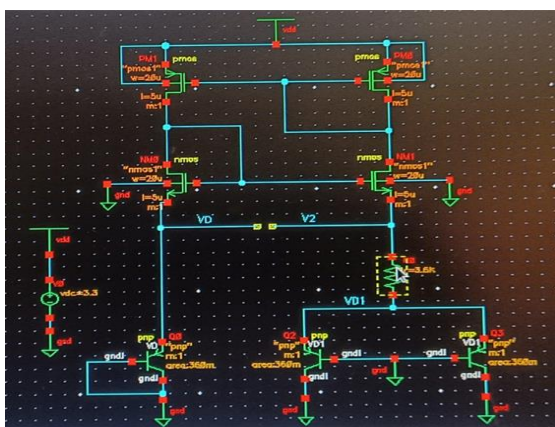


Figure 11 (a) Schematic of the PTAT circuit.

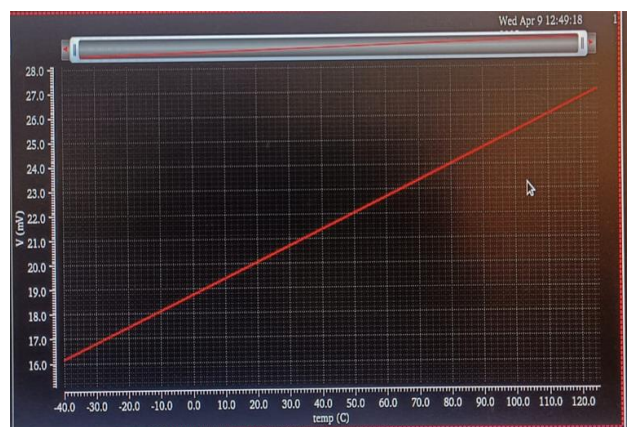


Figure 11 (b) PTAT generation circuit

Figure 11(b) shows the DC response of the PTAT circuit exhibits a rising voltage trend with increasing temperature. This confirms a positive temperature coefficient, which is the desired behaviour for PTAT generation.

6.3 Bandgap Voltage Reference Circuit Results

The final stage combines scaled PTAT and CTAT voltages to produce a stable, temperature-independent Bandgap Reference output (V_{REF}).

Design Strategy: PTAT and CTAT ratios are chosen to cancel temperature effects, yielding a stable V_{REF} near 1.2V.

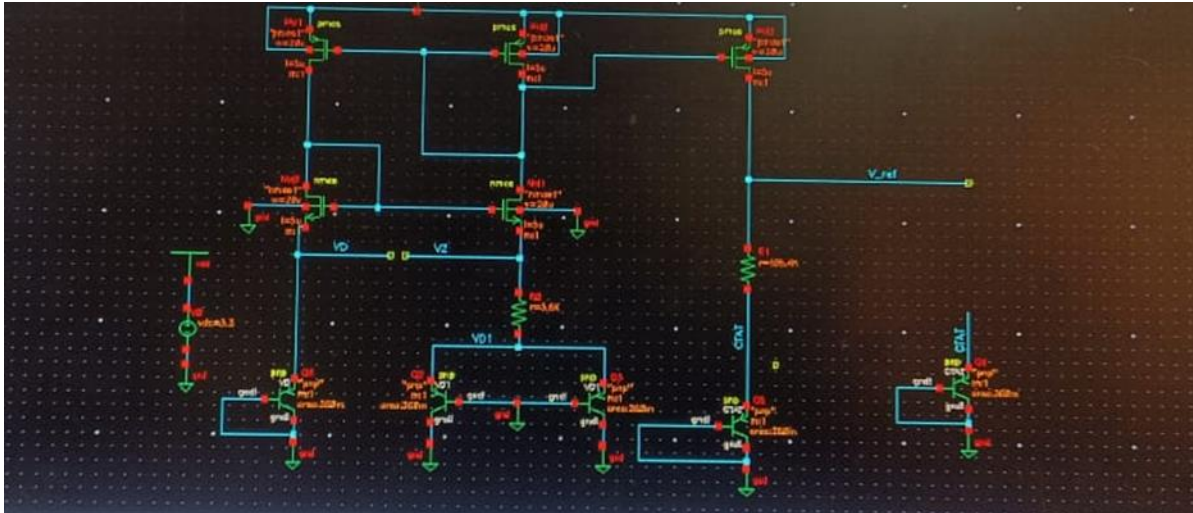


Figure 12(a) Schematic of the full BGR circuit

Figure 12(a) shows the complete Bandgap Reference circuit, which sums PTAT and CTAT voltages. Resistors and current mirrors are tuned to achieve temperature cancellation, producing a stable V_{REF} .

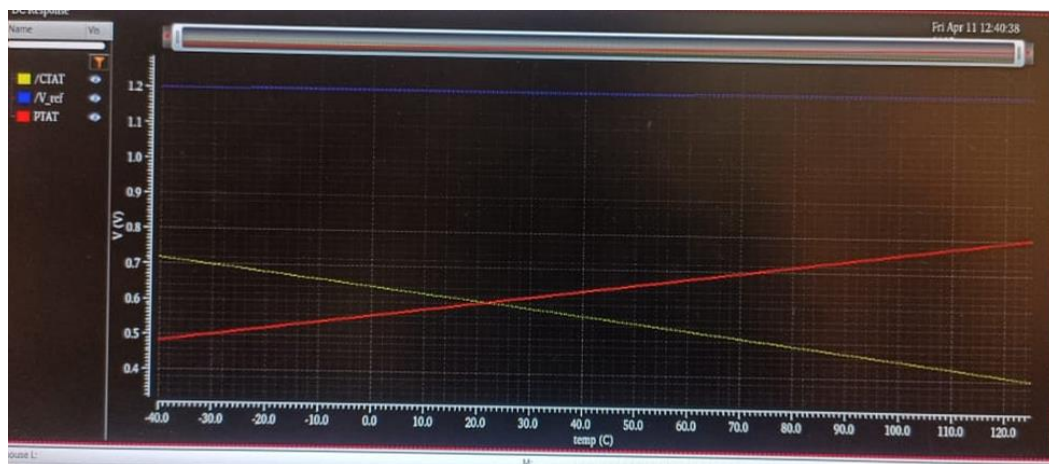


Figure 12 (b) DC response of full BGR circuit.

Figure 12 (b) shows the DC simulation of the BGR circuit, confirming a stable 1.2V output across temperatures, validating effective temperature compensation.

6.4 Discussion

The simulation results for each individual block and the integrated circuit were consistent with theoretical expectations. The following key findings were observed

1. Temperature Stability: The CTAT circuit showed a decreasing trend in voltage with temperature (negative coefficient). The PTAT circuit showed an increasing trend in current with temperature (positive coefficient). When combined, the opposing trends cancelled each other out, producing a stable voltage reference.
2. Accuracy and Output Voltage: The final V_{REF} achieved is near 1.2V, which is standard for BGR circuits. The reference voltage remained consistent over a temperature range typically from -40°C to $+125^{\circ}\text{C}$.
3. Performance Analysis: Low Power Consumption: Achieved by using 180nm CMOS technology. High Stability: Resulted from careful tuning of resistor ratios and transistor sizing. Design Efficiency: Simulation results matched closely with theoretical predictions, validating the design methodology.

VII. SUMMARY

The achieved results highlight the effective design and realization of a temperature-stable Bandgap Voltage Reference circuit. Cadence simulation tools played a key role in analysing the performance of the CTAT, PTAT, and overall BGR circuits. The final circuit is well-suited for applications like analog-to-digital converters, temperature sensing, voltage regulation, and other integrated systems that demand a reliable reference voltage.

VIII. CONCLUSION

The Bandgap Voltage Reference (BGR) circuit was designed and implemented successfully, addressing a key challenge in analog circuit design by integrating PTAT and CTAT voltage generation techniques. Cadence EDA tools were used for simulation and validation, ensuring accurate modelling of transistor behaviour. The final BGR circuit yielded a stable, nearly temperature-independent output voltage close to 1.2V. This project has practical implications for low-power, precision-driven electronic systems and reinforces the significance of bandgap references in integrated circuit design. It also provides a foundation for further enhancements, such as improving power supply rejection ratio, minimizing area, and extending output voltage range.

REFERENCES

- [1]. S. Patel and A. Naik, "Design of Start-up Enabled Bandgap Voltage Reference," Proc. 6th Int. Conf. on Devices, Circuits and Systems (ICDCS), Coimbatore, India, pp. 18–22, 2022, doi: 10.1109/ICDCS54290.2022.9780858.
- [2]. R. L. M. Bagundol, J. A. Hora, and E. L. Oling, "Design Methodology of a Voltage Bandgap Reference with High PSRR in Advanced Technology Nodes for LDO Application," Proc. IEEE 14th Int. Conf. on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment, and Management (HNICEM), Boracay Island, Philippines, pp. 1–6, 2022, doi: 10.1109/HNICEM57413.2022.10109433.
- [3]. A. Anand and P. R. Sreenidhi, "Design and Simulation of CMOS based Bandgap Reference Voltage with Start-up Circuit using 180 nm, 90 nm and 45 nm Process Technology," Proc. 8th Int. Conf. on Advanced Computing and Communication Systems (ICACCS), Coimbatore, India, pp. 1078–1083, 2022, doi: 10.1109/ICACCS54159.2022.9785154.
- [4]. S. S. Sangolli and S. H. Rohini, "Design of low voltage bandgap reference circuit using sub-threshold MOSFET," Proc. 5th Nirma Univ. Int. Conf. on Engineering (NUICONE), Ahmedabad, India, pp. 1–6, 2015, doi: 10.1109/NUICONE.2015.7449627.
- [5]. C.-L. Lee, R. M. Sidek, F. Z. Rokhani, and N. Sulaiman, "A low power bandgap voltage reference for Low-Dropout Regulator," Proc. IEEE Regional Symp. on Micro and Nanoelectronics (RSM), Kuala Terengganu, Malaysia, pp. 1–4, 2015, doi: 10.1109/RSM.2015.7354986.
- [6]. X. Min, Y. Wei-ming, Y. Wu-tao, Z. Jing, and Z. Yi-chuan, "An op amp-less band-gap voltage reference with high PSRR and low voltage," Proc. Asia Pacific Conf. on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Shanghai, China, pp. 166–169, 2010, doi: 10.1109/PRIMEASIA.2010.5604934.