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LOW POWER 3-BIT ENCODER DESIGN USING MEMRISTOR

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Abstract: Combinational circuits are the fundamental building blocks for almost all digital electronic systems. In this project, we are proposing one of the combinational circuit 3-bit encoder using Memristor. Here, we are designing 3-bit encoder in CMOS logic, Pseudo NMOS logic and Memristor (MRL) logic. A comparative analysis also have done among these configurations of design. From this analysis, we are able to choose best configuration of design that applicable for specified areas of applications.

Keywords: Memristor, 3-bit Encoder, Low Power Design, CMOS, Pseudo NMOS, MRL

I. INTRODUCTION

In the era of big data, data protection is vital and challenging because no one can predict where and when the next downtime will occur. Data backup technology is one of the best solutions in practice to minimize data loss and other negative impacts. Therefore, the efficiency in data backup and restoring will determine whether the system can maintain a continuous and stable operation. During the backup process, data stored in the volatile memory will be transferred to the nonvolatile memory and restored after downtime ends. The latency for the data transportation mainly depends on the type of memory and the structure of the system. How to minimize such latency becomes crucial for the efficiency of data backup.

II. OBJECTIVES

The objectives of the project are:

- This project aims to develop an optimized encoder by reducing transistor count, power dissipation.
- To achieve this, a comparative study is performed on encoders designed using CMOS, Pseudo-NMOS, and MRL techniques..

III. BLOCK DIAGRAM

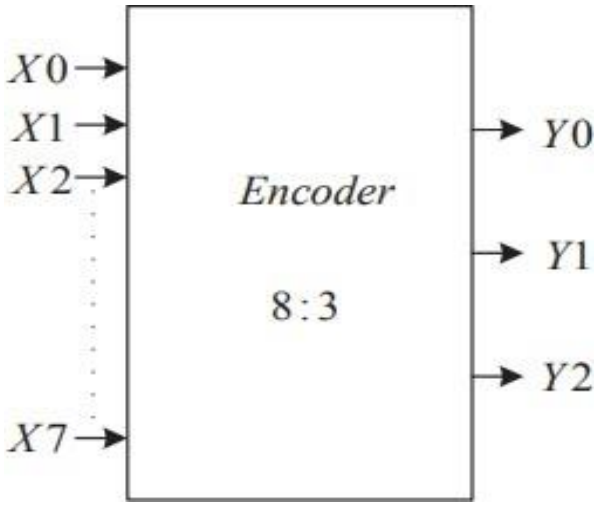

Figure 1. 3-bit encoder

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X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Figure 2. Truth table encoder

Information in digital logic circuits with specific meaning is encoded into corresponding binary bits. Encoder is a circuit which does this encoding function. The encoder‘s function is to encode when one of the input bits is of effective level, and the encoder‘s output changes in accordance with its input bits. The circuit has _N‘ outputs and _M‘ inputs and they are related by M = 2N.

From the Encoder truth table, the outputs and inputs are related by

Y0 = X1 + X3 + X5 + X7
Y1 = X2 + X3 + X6 + X7
Y2 = X4 + X5 + X6 + X7

From these relations, logic circuit can be implemented using CMOS, Pseudo NMOS and MRL. In the Encoder circuits, X1- X7 are input bits and Y2, Y1, Y0 are output bits. In Encoder circuit by using MRL, M1, M2, M3, M4 act as pull-down network and a Memristor acts as pull-up network. M1, M2, M3, M4 and Memristor constitute a 4-input NOR gate. X1, X3, X5, X7 are the input signals that pass through the NOR gate and the signal at the drain of M1 is inverted signal of (X1 + X3 + X5 + X7). M13 and Memristor constitute an inverter. The output of 4- input NOR gate is given as the input of inverter. The signal at the drain of M13 is Y0 = X1 + X3 + X5 + X7.

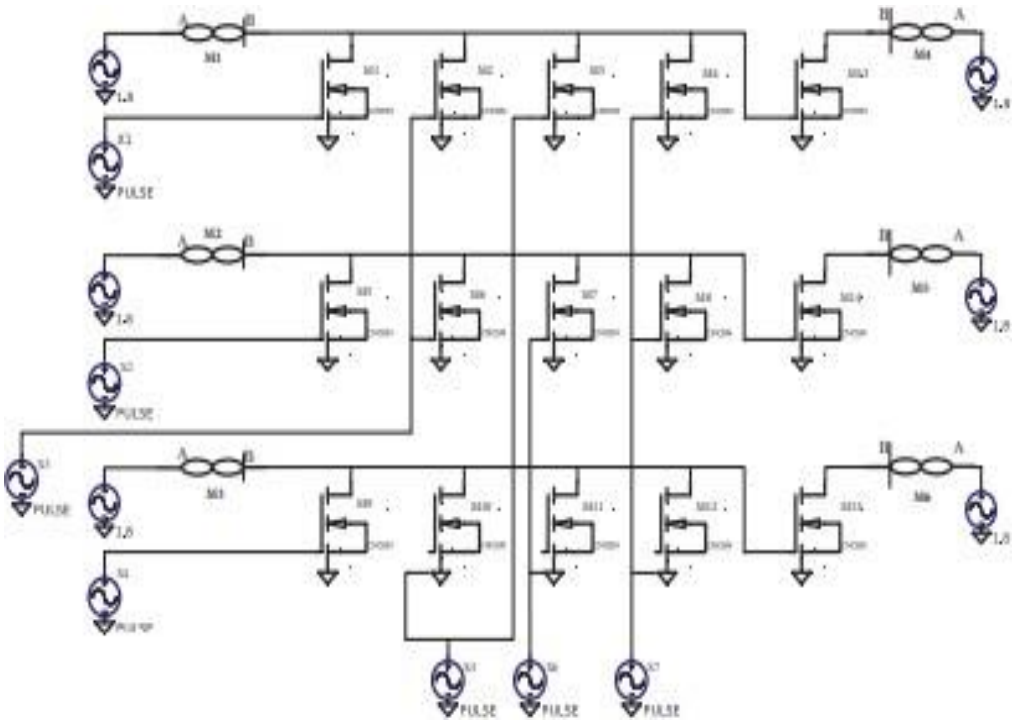

Figure 3. Schematic of encoder using memristor based logic

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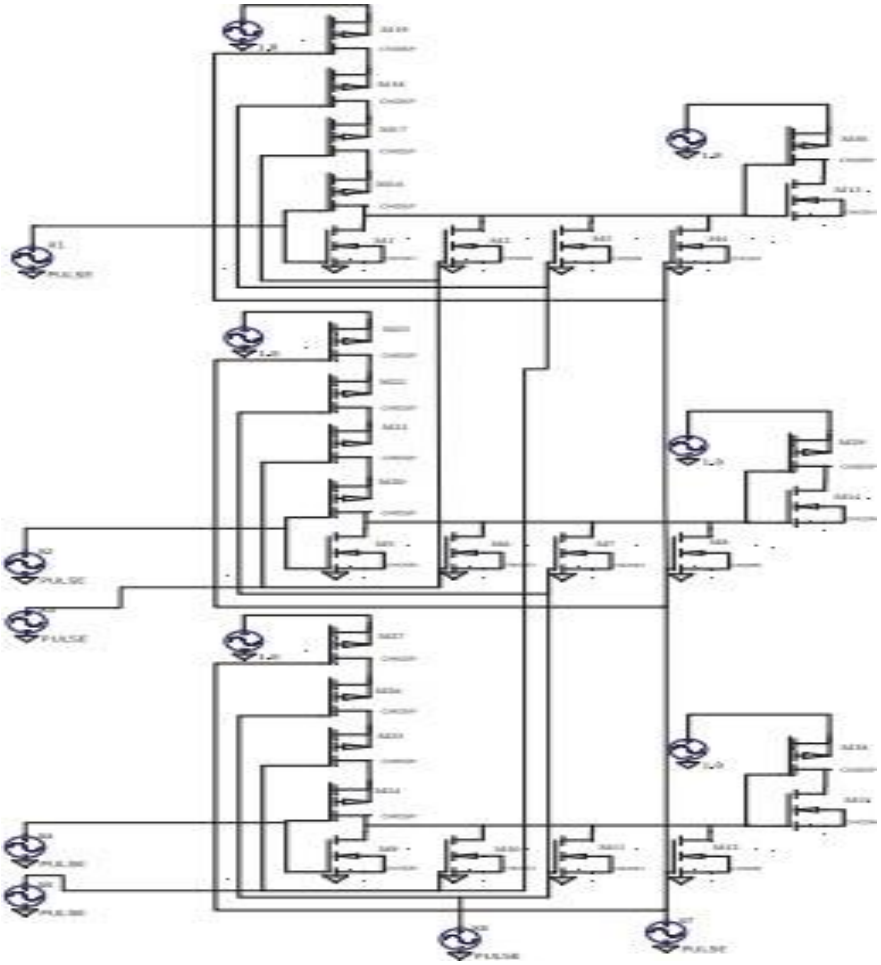

Figure 4. Schematic of encoder using CMOS Logic

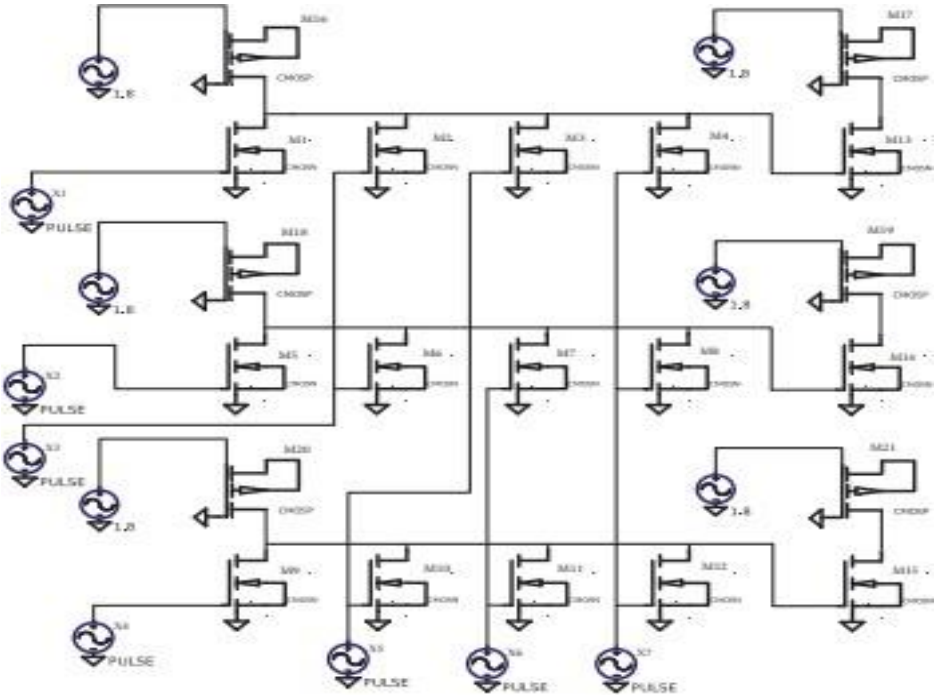

Figure 5. Schematic of encoder using Pseudo-NMOS Logic

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As, it is known that the area occupied by a Memristor based design is lesser than CMOS it can be depicted that this design is efficient with respect to the area consumed. It can be seen that the number of transistors that are required for this design is the least when compared to the conventional CMOS and Pseudo NMOS logic. By using CMOS technology, the encoder circuit has 30 transistors, of which 15 PMOS and 15 NMOS. By using Pseudo NMOS technology, the encoder circuit has 21 transistors, of which 5 PMOS and 15 NMOS. By using MRL technology, the encoder has 21 transistors, of which 6 Memristors and 15 NMOS.

IV. CIRCUIT IMPLEMENTATION

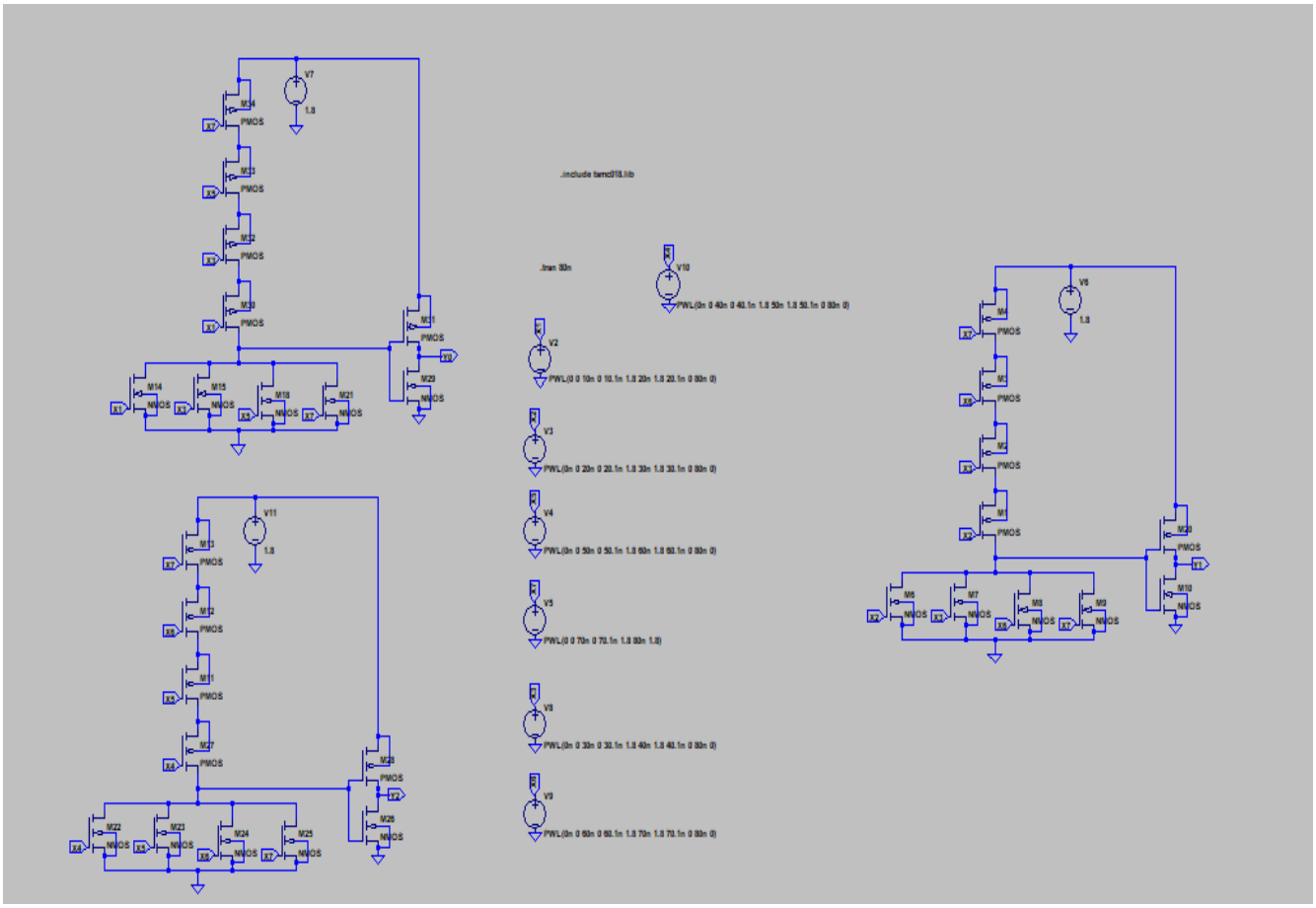

Figure 6. Block diagram of encoder for CMOS

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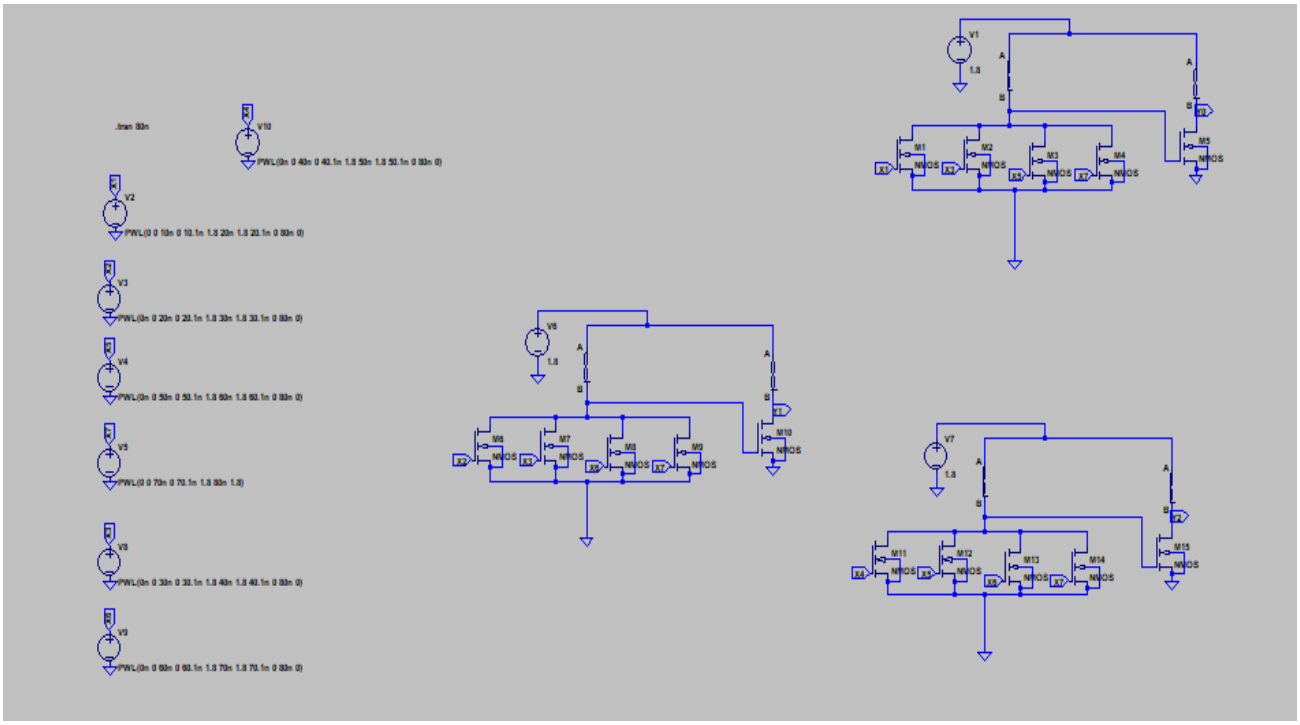

Figure 7. Schematic of memristor based encoder

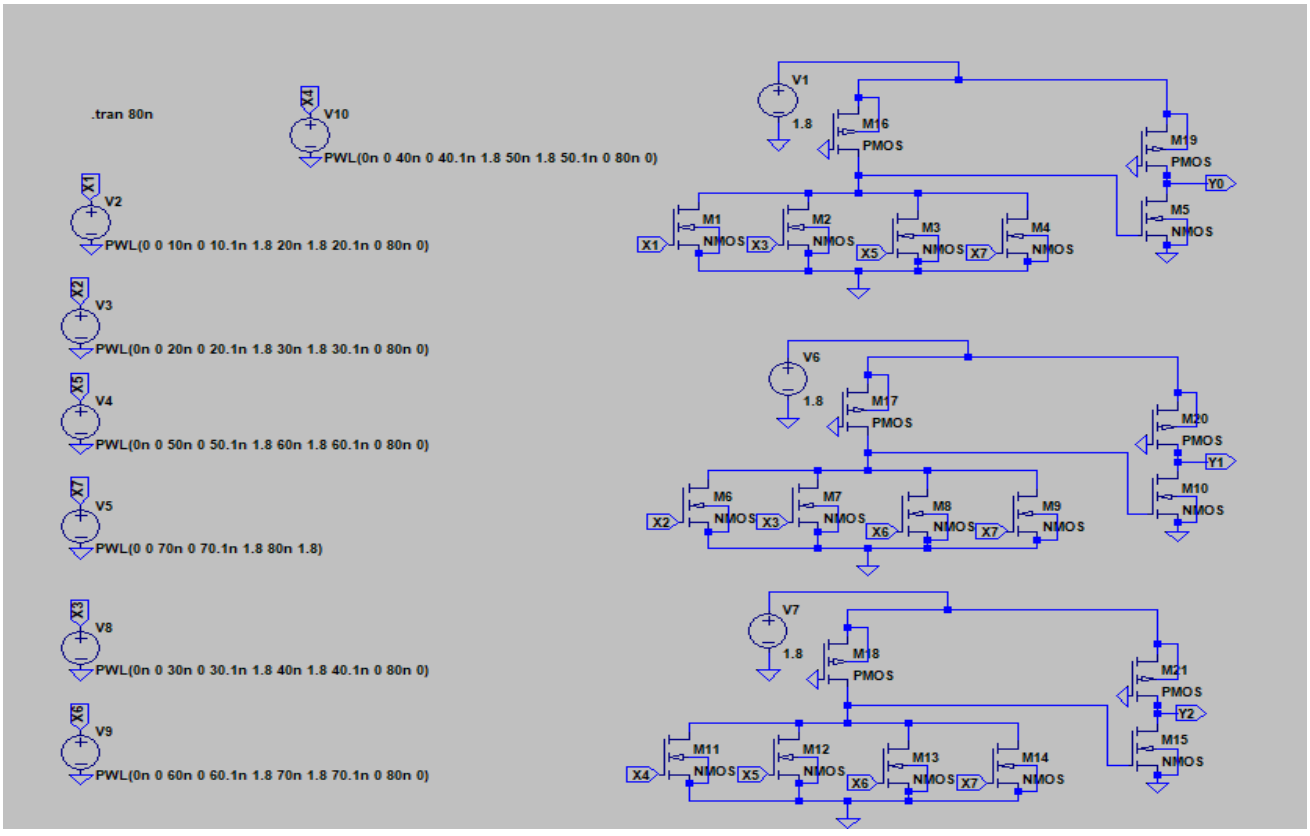

Figure 8. Schematic of Pseudo NMOS Encoder

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V. SIMULATION RESULT

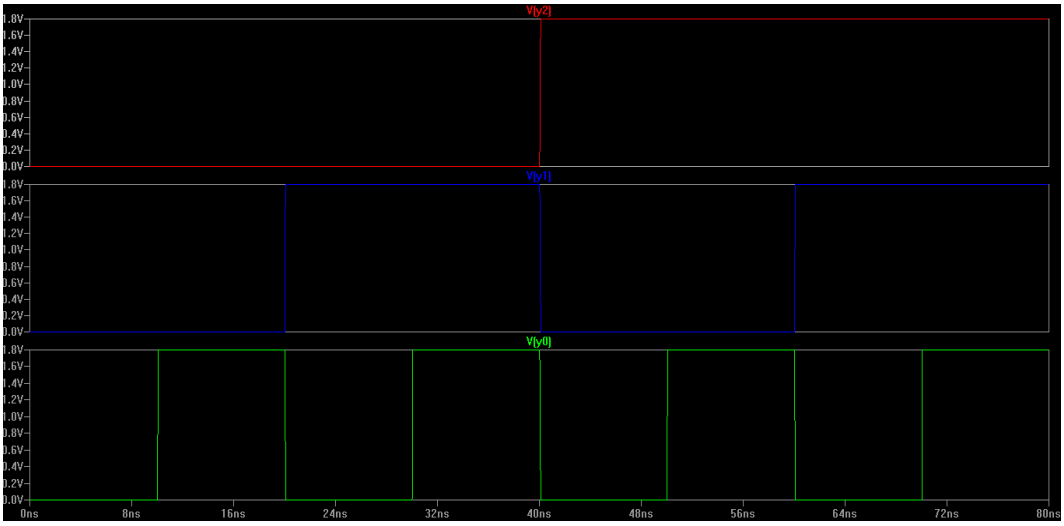

Figure 9. Output waveforms of encoder

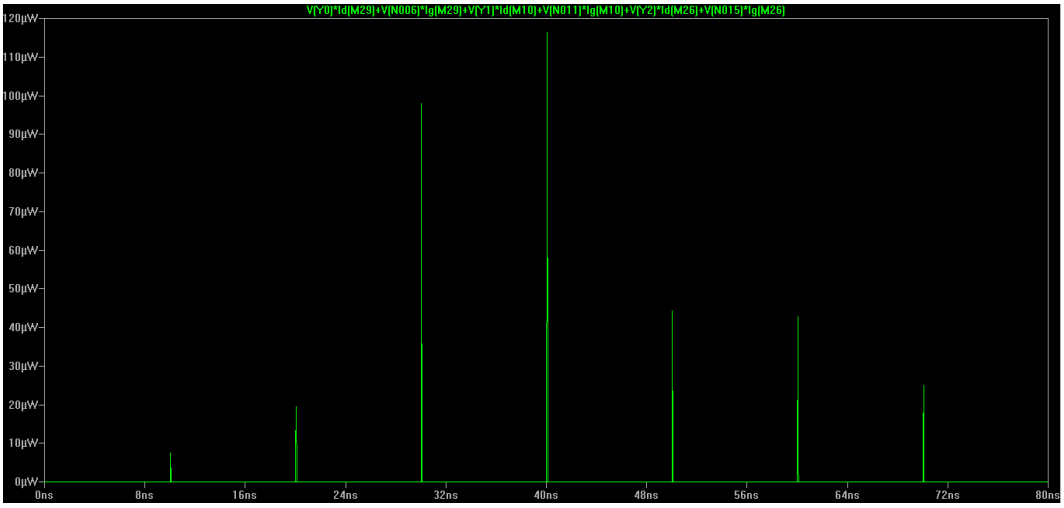

Figure 10. CMOS Power Waveform

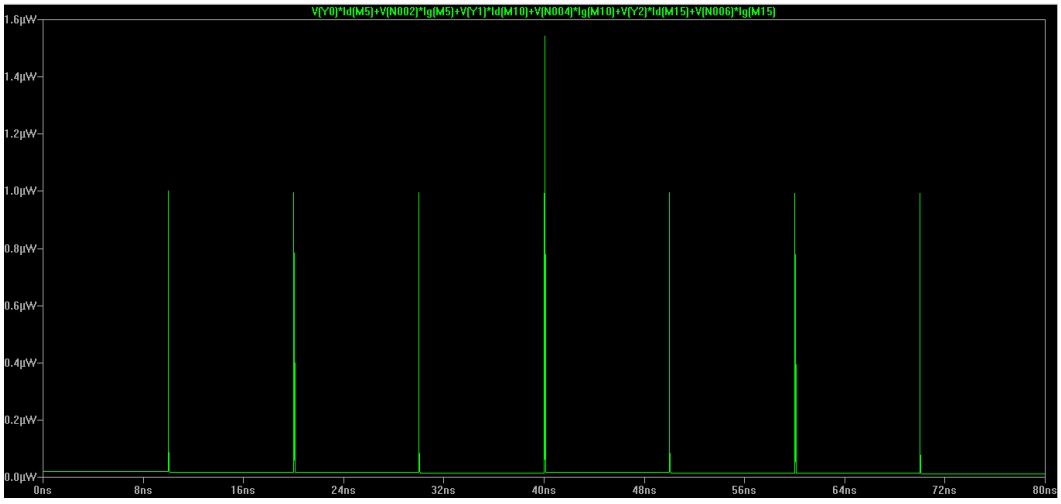

Figure 11. MRL Power Waveform

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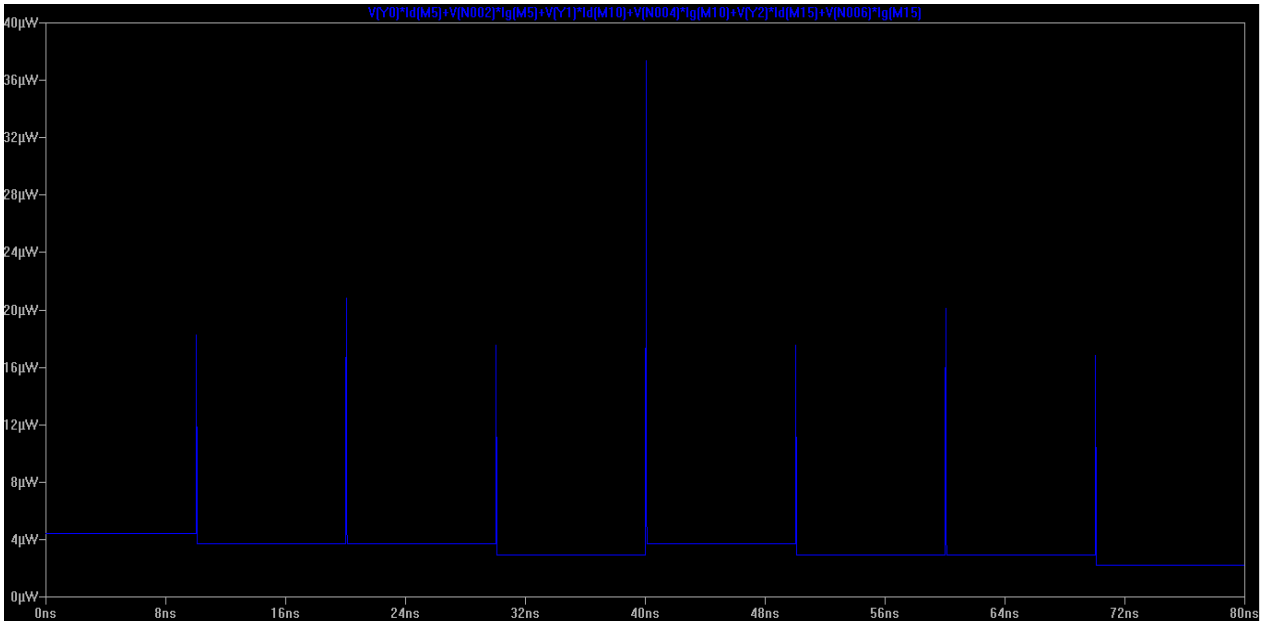

Figure 12. Pseudo NMOS Power Waveform

Comparison of performance parameters among CMOS, Pseudo NMOS and MRL based encoders.

	Average power
CMOS based encoder	169.63nW
Pseudo NMOS encoder	3.3598µW
MRL based encoder	18.413nW

Figure 13. Comparison of performance parameters

VI. ADVANTAGES, APPLICATIONS & LIMITATIONS

Advantages

- Encoder using memristor logic achieves lesser power consumption.
- And the transistor count is also reduced using the MRL design of encoder.

Applications

- Data backup technology.
- Non-volatile memory applications.
- Digital circuits.
- Logic circuits.
- Biological and neuromorphic systems.
- Computer technology.
- Digital as well as analog memory.

Limitations

- The document mentions a "trade-off between the power, area and speed of a circuit," which implies that optimizing one aspect may come at the cost of another. This presents a limitation in achieving simultaneous optimization of all three parameters.

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- The study is focused on a 3-bit encoder. Scaling the design to larger bit encoders may introduce new challenges and complexities that are not addressed in this paper.

- While the document demonstrates the advantages of Memristor-based design, it's important to acknowledge that Memristor technology is still an emerging field. Limitations related to the maturity of Memristor devices, such as reliability, variability, and manufacturing scalability, are inherent.

VII. CONCLUSION

Design of encoder with Memristor based logic design is much efficient in the aspects of power and area when compared with conventional CMOS logic and Pseudo NMOS logic. The trade- off between the power, area and speed of a circuit is persistent. It can be concluded that this design technique gives lesser number of transistor count required and makes it more efficient way of designing a digital circuit.

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