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Charge Based Modelling for the Semiconductor Substrate of the Ferroelectric Field Effect Transistor (FEFET)

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Abstract: This paper presents the modelling of FEFET by using the BSIM for the semiconductor layer while dealing with the Landau – Khalatnikov formulation for the Ferroelectric layer. Results are presented for the simulation for the charge-based evaluation of the semiconductor substrate, while the challenges to be addressed for the FE layer are enumerated.

Keywords: Ferro-Electric Field Effect Transistor, Landau – Khalatnikov Formulation, Berkeley Short Channel IGFET Model (BSIM), Interstitial Layer, Polarization of Domains.

I. INTRODUCTION

In accordance with Moore's Law the down-scaling in the size of transistors, specifically MOSFET [1], [2], has opened up newer avenues to investigate more power-efficient, high speed memory devices [3], [4]. With the CMOS reaching its limit of scalability, usually defined by the Boltzmann Tyranny [5], and the advent of ferroelectric materials [6], there is an increased awareness to further explore Ferroelectric Field Effect Transistors (FeFET), Fig. 1(a), for memory-based applications [7]. As shown in Fig. 1(b) the FeFET of Fig. 1(a) can be represented as a combination of 2 equivalent capacitive elements for the ferro-electric (FE) layer and the interstitial layer respectively (IL) in series with the gate terminal [8]. This paper deals with an overview and the future prospects with respect to the performance parameters viz. Swing, overdrive and Short Channel Effects (SCE) on the basis of Charge Based Modelling.

Fig.1 (a) Ferroelectric Field Effect Transistors (FeFET) (b) Equivalent Circuit representation.

II. NEGATIVE CAPACITANCE CONCEPTS

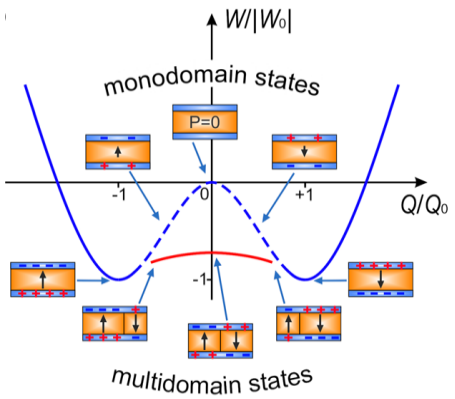

Fig.2 Domain formation and the corresponding energy distribution.

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The underlying concepts and mathematical nuances of the negative capacitance were articulated by T. K. Song [9], formulated on the basis of the equivalent circuit on the basis of Landau – Khalatnikov equation used to model the energy function in the FeFET.

$$W = a.R^2 + b.R^4 + c.R^6 \quad (1)$$

Where a, b, and c are empirical constants and R is the polarization.
Thereby the charge across the ferroelectric layer is given by

$$Q_{FE} = \varepsilon_0 E_{FE} + R \quad (2)$$

Where ε_0 is absolute permittivity, and E_{FE} is electric field across the FE layer. Apparently, the variance of the negative capacitance improves significantly by designing suitably the thickness of the coating used for the FE dielectric. This also implies that the domain formation, shown in Fig.2, is not uniform across the layer of the FE, and rather is a function of the energy W as given in (1). Shan Deng et al [3] have investigated the underlying mechanisms for the matching of charges between the FE layer and the IL. Consequently, the charge matching can be improved by suitably reducing the FE layer polarization and its dielectric material properties. Such a modulation of the inherent properties also led to an enhancement of the memory window (MW), as given by (3)

$$V_{fe(ret)} = \frac{P_{fe}}{C_{fe}+C_{is}} \quad (3)$$

where $V_{fe(ret)}$ is the voltage during the retention period, P_{fe} the polarization of the FE layer, $C_{fe} and\ C_{is}$ the capacitance of the FE and the IS layers. Chirag Garg et. al. [10] addressed the effects of traps on the performance of the FDSOI FET. Hot Electron Effects and Bias Temperature Instability (BTI) are fallouts of either interface traps or bulk traps. The concentration of the traps is affected by operational parameters like applied gate bias, while to some extent the process parameters like mechanical stress and chemical reactions during the fabrication process. In all, the capacitance of the FE layer can be represented using (4)

$$C_{fe} = \frac{1}{(2\alpha+12\beta P^2+30\gamma P^4)T_{fe}} \quad (4)$$

Where P is the polarization, α, β, γ are process parameters, and T_{fe} is the thickness of the FE layer. As evident from (4) the T_{fe} becomes a limiting factor in determining the maximum value of C_{fe}. Therefrom the range of voltages for the MW can be designed to suit the retentivity of memory for a particular application. These factors put together emphasize the necessity of charge-based modelling for the semiconductor bulk charges and the polarization across the FE to analyse the performance degrading parameters.

III. CHARGE BASED MODELING FOR FET

The Berkeley Short Channel IGFET Model (BSIM) [11] is used very much effectively to represent the transistor, while for the FE layer the Landau-Khalatnikov formulation is used. The BSIM takes into account several physical parameters for the semiconductor device along with the associated operational characteristics, and for the charge-based modelling, equation (5) is one of the most efficient methods used for the description of the threshold voltage V_{th}.

$$V_{th} = V_{FB} + \varphi_S + \gamma.\sqrt{\varphi_S - V_{BS}} - K_1.(\varphi_S - V_{BS}) - \eta.V_{DS} \quad (5)$$

As evident, the factors taken into account are Body Effect coefficient $\gamma = \sqrt{\frac{2.q.\varepsilon_{Si}.N_A}{C_{ox}}}$, the Source – Drain Depletion charge sharing coefficient K_1, the flat band voltage V_{FB}, surface potential φ_S, Source – Substrate bias V_{BS}, the Drain Induced Barrier Lowering parameter η, and the applied Drain – Source voltage V_{DS}.
While the current I_{DS} is 0 in the cut – off region, i.e. for the applied Gate – Source voltage $V_{GS} < V_{th}$, in the linear i.e. triode region for $V_{GS} > V_{th}, and\ 0 < V_{DS} < V_{DSsat}$ the I_{DS} is accurately represented by (6)

$$I_{DS} = \left(\frac{\mu_0}{1+U_0(V_{GS}-V_{th})}\right)\left\{\frac{C_{ox}.\frac{W}{L}}{1+\frac{U_1}{L}}\right\}\left\{(V_{GS}-V_{th})V_{DS} - \frac{a}{2}V_{DS}^2\right\} \quad (6)$$

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The body effect coefficient is scaled to account for the surface potential and the source substrate bias as given in (7) and is are quite different from the text-book models available in [12]

$$a = 1 + \frac{\left\{\left(1-\frac{1}{1.744+0.8364\left(\varphi_S - V_{BS}\right)}\right)\gamma\right\}}{2.\sqrt{\varphi_S - V_{BS}}} \tag{7}$$

In the saturation region i.e. for $V_{GS} > V_{th}, and\ V_{DS} > (V_{GS} > V_{th}) i.e. V_{DS} > V_{DSsat}$ the I_{DS} is given by (8)

$$I_{DS} = \frac{\left(\frac{\mu_0}{1+U_0(V_{GS}-V_{th})}\right)\left(C_{ox}.\frac{W}{L}(V_{GS}-V_{th})\right)}{2.a.K} \tag{8}$$

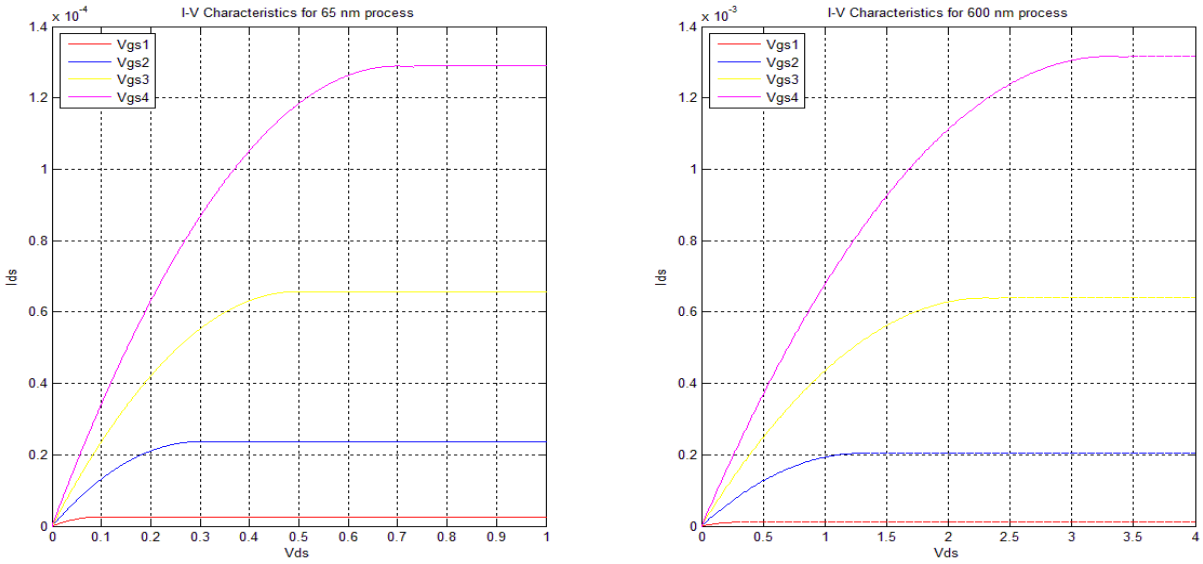

Fig. 3 I – V Characteristics for 600 nm and 65 nm process transistors

For the simulation results, obtained using MATLAB-R2024b, in the I – V characteristics as shown in Fig. 3 the discontinuities of the drain current are taken into account by the including the sub-threshold current into effect. This can be done by analysing the drain current as summation of the strong inversion component and the weak inversion component, equations (9), (10)

$$I_{DS} = I_{DS,strong} + I_{DS,weak} \tag{9}$$

$$I_{DS,weak} = \mu_0 C_{ox}.\frac{W}{L}\left(k.\frac{T}{q}\right)^2.e^{1.8}.e^{\frac{\frac{q}{k.T}(V_{GS}-V_{th})}{n}}\left[1-e^{-V_{DS}.\frac{q}{kT}}\right] \tag{10}$$

Here the empirically determined factor $e^{1.8}$ ensures that the discontinuity in the drain current is removed, and the overall subthreshold conduction does not have any adverse impact on the total drain current.

The BSIM model for the semiconductor has to be amalgamated with the equivalent circuit model for the FE layer of the FEFET. This ensures that there is suitable charge sharing [13] mechanism between the FE layer and the underlying semiconductor substrate for the equivalent circuit as shown in Fig. 1(b). In such a scenario the voltage across the FE layer is given by equation (11)

$$V_{FE} = \frac{P_{FE}}{C_{FE}+C_{IS}} \tag{11}$$

Where P_{FE} is the polarization of the FE layer required for a higher retentivity of the data, $C_{FE}\ and\ C_{IS}$ are the capacitance of the FE and the interstitial layers (IL), respectively. The C_{FE} is largely affected by the thickness of the FE layer in addition to being dependent upon the polarization P_{FE}. Therefore, from the perspective of design of the FE layer the thickness has to be optimized to get the higher reliability.

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IV. CONCLUSION

The polarization domains of the FE layer play an important role in determining the Memory Window (MW) of the FEFET, and hence the charge-based modeling for the semiconductor layer seems to be the most effective way to obtain a better performance.

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