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CMOS Design and Performance Analysis of Ring Oscillator for Different Stages

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Abstract: In the evolving landscape of Very Large Scale Integration (VLSI), ring oscillators play a critical role in evaluating process, voltage, and temperature (PVT) variations, and are widely used in applications such as clock generation, frequency synthesis, and on-chip testing. This project presents a comprehensive CMOS-based design and performance analysis of ring oscillators with varying stages using the Cadence design suite. The primary objective is to study how the number of stages impacts key performance parameters such as oscillation frequency, power consumption, propagation delay, and area.The design methodology involves the implementation of odd-stage CMOS inverter chains (3, 5, 7, and 9 stages) in the Cadence Virtuoso platform using a standard 180nm technology library. Post-layout simulations are performed using Spectre simulator to ensure accurate timing and power analysis. The frequency of oscillation is observed to decrease with an increasing number of stages, while power dissipation and area show a proportional rise. This study provides valuable insights into the trade-offs involved in the design of ring oscillators, aiding in the selection of optimal configurations for various low-power and high-speed VLSI applications.

Keywords: VLSI, Ring Oscillator, PVT, Power Consumption, Propagation Delay, Cadence Virtuoso, Spectre simulator.

I. INTRODUCTION

The ring oscillator is a fundamental circuit widely used in various applications such as clock generation, frequency synthesis, and delay measurement in integrated circuits. This project focuses on the CMOS (Complementary Metal-Oxide-Semiconductor) design and performance analysis of ring oscillators with varying stages. The ring oscillator operates based on the principle that an odd number of inverter stages connected in a loop can produce a periodic oscillation without requiring an external input signal. The frequency of oscillation is determined by the number of stages and the propagation delay of each inverter.

In this project, different configurations of ring oscillators—such as 3-stage, 5-stage, and 7-stage designs—are developed and analyzed using CMOS technology. Key performance parameters such as oscillation frequency, power consumption, and propagation delay are studied to understand how increasing the number of stages affects the overall behavior of the oscillator.

Simulations are carried out using standard CMOS technology nodes to assess the trade-offs between speed, power efficiency, and circuit stability. The goal is to identify optimal design choices for specific application requirements. This analysis is crucial for designing efficient timing circuits in modern digital systems, where performance and power are critical design constraints.

Ring Oscillator is a Circuit made of an odd number of inverter stages(gain stages) connected in a closed group.It Oscillates without requiring an external input. Basic element of Ring Oscillator is an Inverter cell. Cell consist of complementary pairs[pmos,nmos].

II. OBJECTIVES

The objectives of the project are:

1. Study the impact of the number of inverter stages on frequency, power consumption and delay.
2. Compare power consumption across different stages to determine efficiency improvements.
3. Design and analyze CMOS ring oscillators with different stages (5, 7, and 9) using Cadence Virtuoso.

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III. BLOCK DIAGRAM

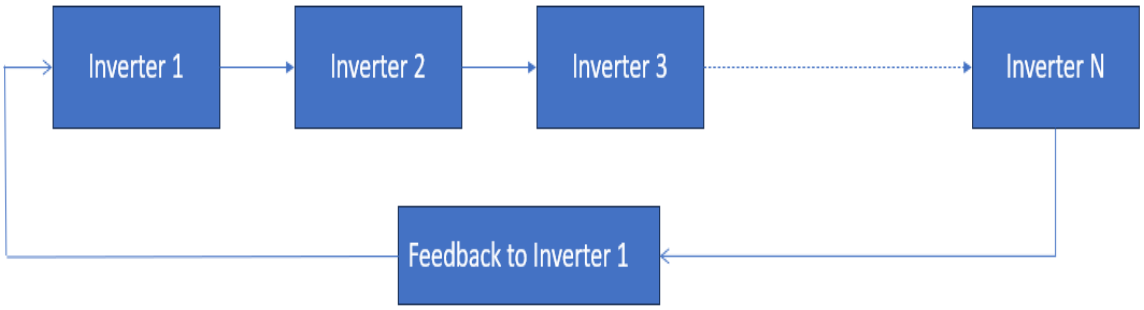

Figure 1. Block Diagram

This figure shows thats the basic structure of a ring oscillator, which is composed of an odd number of CMOS inverters connected in a loop. Each inverter's output is connected to the input of the next, creating a sequential chain. The last inverter (Inverter N) completes the loop by feeding its output back to the input of the first inverter (Inverter 1), forming a closed feedback path.

This closed-loop configuration is crucial for the operation of the ring oscillator. Because the number of inverters is odd, the signal inverts each time it passes through an inverter, resulting in a continuous oscillation between high and low voltage levels. If an even number of inverters were used, the signal would stabilize and stop oscillating.

When the circuit is powered on, any small disturbance or noise is enough to trigger a transition that propagates through the inverters, generating a periodic waveform. The frequency of oscillation depends on the number of stages and the delay of each inverter.

Ring oscillators are widely used in integrated circuit design for applications like clock generation, process monitoring, and performance testing. Their simplicity and ease of implementation make them valuable tools in digital electronics and VLSI design.

Sampling converts analog signals into digital data for processing. In this project, the Sampling Module captures signals from the Simulated cDAQ at 1000 samples per second, ensuring high-resolution data. LabVIEW's DAQmx Timing and Read functions enable accurate, continuous acquisition. Sampled data is then processed and stored under user-defined test names for analysis.

1. Inverter Stages:
- Each block (Inverter 1, Inverter 2, ..., Inverter N) represents an inverter circuit made from CMOS transistors (PMOS & NMOS).
- The odd number (N) of inverters ensures proper phase shift and oscillation.

2. Signal Propagation:
- The signal enters Inverter 1, gets inverted, and is passed to the next stage.
- This inversion continues until the last stage (Inverter N) is reached.

3. Feedback Path:
- The output of Inverter N is fed back to the input of Inverter 1.
- This feedback ensures continuous switching, leading to a self-sustaining oscillation.

IV. CIRCUIT IMPLEMENTATION

A. 3-Stage Ring Oscillator:

A 3-stage ring oscillator is a type of inverter-based oscillator commonly used in integrated circuits for clock generation, signal processing, and testing purposes. It consists of three CMOS inverters connected in a loop where the output of the last inverter is fed back to the input of the first inverter.

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The image shows a CMOS ring oscillator consisting of three CMOS inverter stages connected in series, with the output of the final inverter fed back to the input of the first. Each CMOS inverter is made up of a PMOS transistor at the top and an NMOS transistor at the bottom.

These pairs are arranged such that when one transistor conducts, the other does not, effectively inverting the input signal. In this configuration, the output of one inverter is connected to the input of the next, forming a chain of three stages. The output of the third inverter is connected back to the input of the first, creating a closed loop. Since each inverter introduces a delay and inverts the signal, having an odd number of inverters ensures that the signal cannot stabilize, resulting in continuous oscillation.

When power is applied, even a small noise signal or disturbance will propagate through the inverters, and due to the odd number of inversions and delay, a periodic waveform is generated. The frequency of oscillation is determined by the number of stages and the propagation delay of each inverter. This type of circuit is widely used for clock generation, testing, and measuring delay in integrated circuit designs.

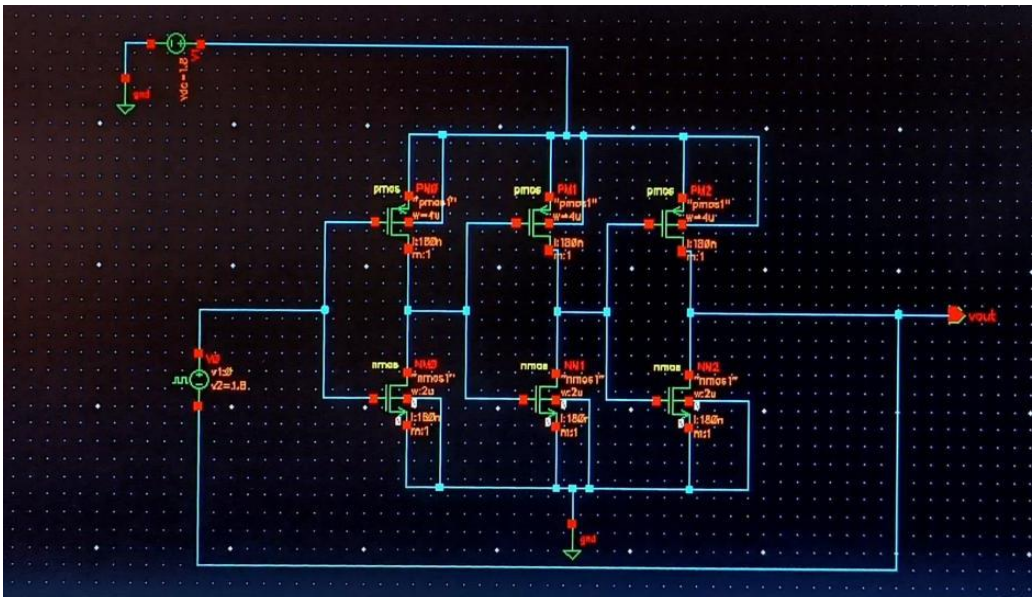

Figure 2. Schematic design of a 3-stage Ring Oscillator

B. 5-Stage Ring Oscillator:

A 5-stage ring oscillator works similarly to a 3-stage ring oscillator, but it has five CMOS inverters connected in a loop instead of three. The basic principles remain the same. If the first inverter starts with a high (1) input, it gets inverted to low (0). This signal propagates through the remaining inverters, alternating between high and low,creating a clock-like signal. By the time the signal reaches the fifth inverter, it is inverted and fed back to the first inverter, causing continuous oscillation.

In addition to the basic working of a 5-stage ring oscillator, several advanced factors influence its performance and practical use.Supply voltage and temperature play crucial roles in determining the oscillation frequency. Higher supply voltage reduces the propagation delay of each inverter, thus increasing the frequency. Conversely, increased temperature tends to slow down transistor switching, lowering the frequency.

Ring oscillators are also valuable tools for process variation monitoring in CMOS technology. Their frequency reflects changes in manufacturing conditions, making them useful for calibration and quality control in integrated circuits. However, they have limitations. Due to their simple structure, ring oscillators exhibit more jitter and lower frequency stability than precision oscillators like crystals, making them less suitable for high-accuracy timing.

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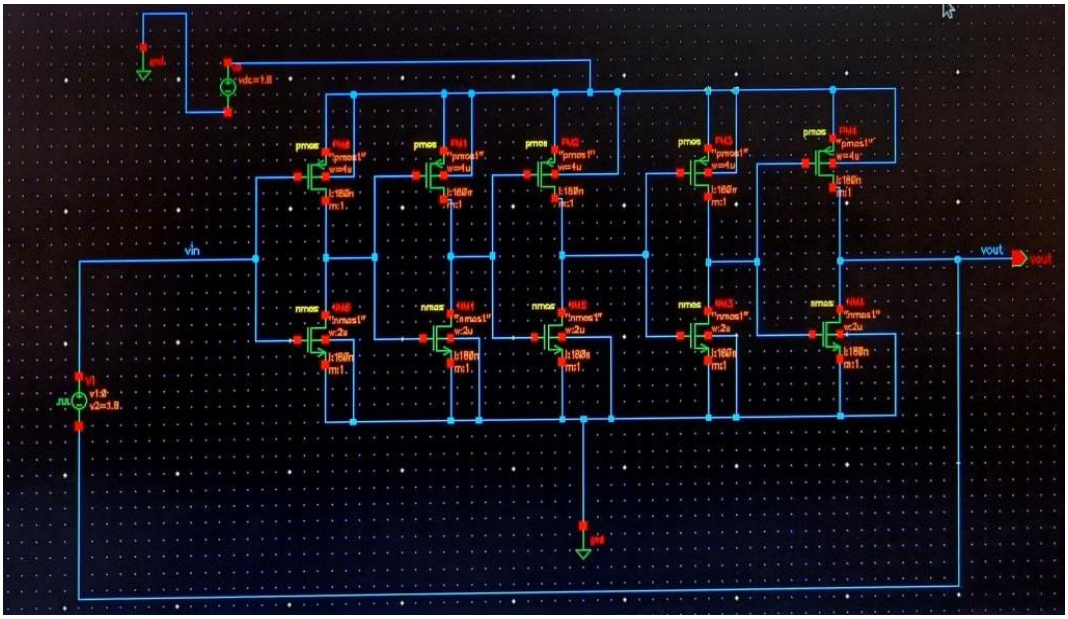

Figure 3. Schematic design of a 5-stage Ring Oscillator

C. 7-Stage Ring Oscillator:

A 7-stage ring oscillator is a type of CMOS oscillator consisting of seven inverters connected in a feedback loop. It is a self-sustaining oscillator. The output of the 7th inverter is fed back to the input of the 1st inverter to sustain oscillations. The circuit generates a periodic clock signal due to continuous toggling between logic high (1) and logic low (0).

A 7-stage ring oscillator consists of seven CMOS inverters connected in a loop, producing continuous oscillation due to the odd number of inversions. The oscillation frequency depends on the number of stages. Like other ring oscillators, its frequency is influenced by supply voltage and temperature—higher voltage increases frequency, while higher temperature reduces it. The oscillator is also useful for monitoring process variations in CMOS technology, as its frequency reflects changes in manufacturing conditions.

However, 7-stage ring oscillators exhibit higher jitter and lower stability compared to crystal oscillators, making them less suitable for high-precision timing applications. Additionally, layout factors such as parasitic capacitance and interconnect delays can affect performance in integrated circuit (IC) design. Despite these limitations, 7-stage ring oscillators are widely used in clock generation, testing, and variability analysis due to their simplicity and sensitivity to circuit conditions.

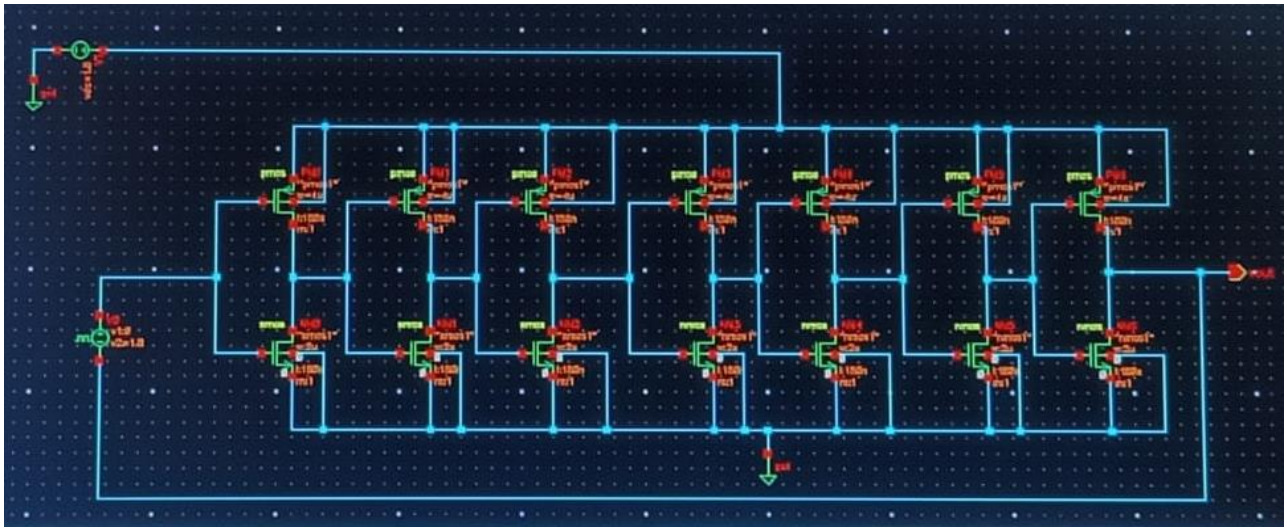

Figure 4. Schematic design of a 7-stage Ring Oscillator

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D. 9-Stage Ring Oscillator:

A 9-stage ring oscillator is a CMOS-based oscillator that consists of nine inverters connected in a loop. It generates a periodic oscillation due to the propagation delay of the inverters, making it useful for clock generation, frequency synthesis, and testing semiconductor variations.If the first inverter starts with a logic high (1) input, it gets inverted to logic low (0). This signal propagates through the remaining eight inverters, alternating between high and low states. The final inverter's output is fed back into the first inverter's input, ensuring continuous oscillation.

In addition to the basic operation of a 9-stage ring oscillator, several advanced factors affect its performance and practical applications. The oscillation frequency of a 9-stage ring oscillator depends on the number of stages and the propagation delay of each inverter. Higher supply voltage reduces delay, increasing the frequency, while higher temperatures increase delay, lowering the frequency.

9-stage ring oscillators are also useful in CMOS process monitoring, as their output frequency reflects changes in manufacturing conditions. This makes them valuable for on-chip calibration and quality control.

However, they are not ideal for high-precision timing. Due to their simple architecture, ring oscillators have more jitter and lower frequency stability compared to crystal oscillators. This limits their use in applications requiring high accuracy.

IC layout considerations are also important, as parasitic capacitance and interconnect delays from the physical placement of inverters can impact the oscillator's performance. These aspects are critical in practical applications like clock generation, random number generation, and semiconductor process evaluation.

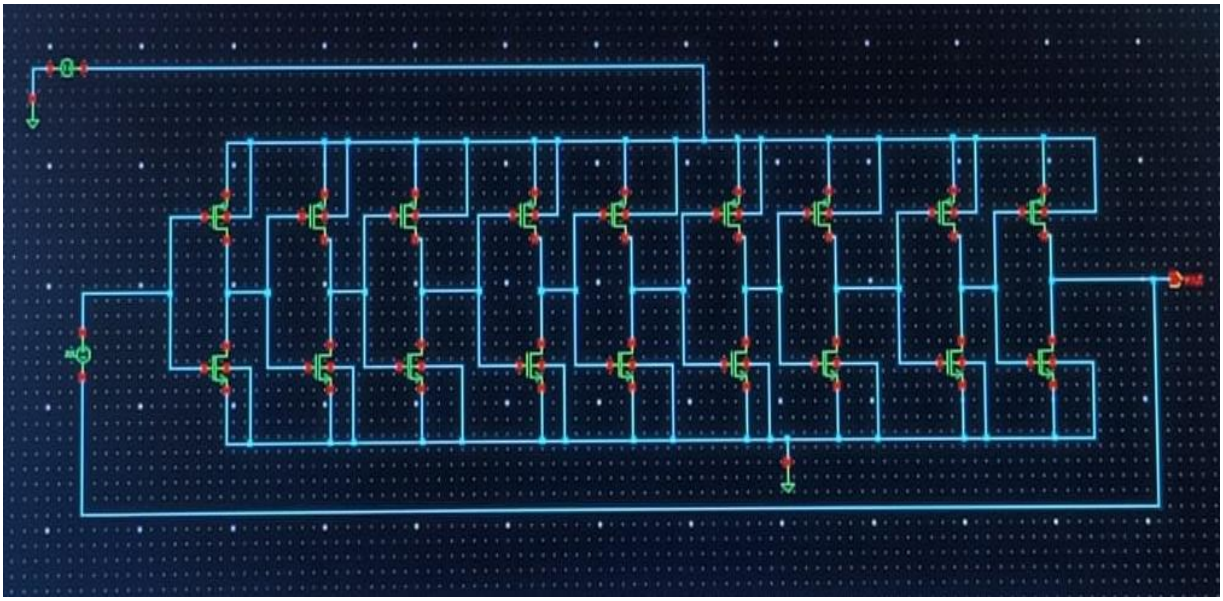

Figure 5. Schematic design of a 9-stage Ring Oscillator

V. SIMULATION RESULT

To verify the functionality and performance of the proposed Ring Oscillators of Different Stages, simulations were performed using Cadence Virtuoso. The presented work has been implemented in Cadence Virtuoso in 180nm technology. Then for evaluating the delay, frequency, power consumption, calculator option was used.

Different waveforms that resulted after simulation are shown in the following figures (Figure. 6 to Figure. 9). The output waveforms of all the different stages of Ring Oscillator shows the inverted output. The figures (Figure. 10 to Figure 12) gives the information about delay, frequency, power consumption calculated for different stages of Ring Oscillator (5,7,9).

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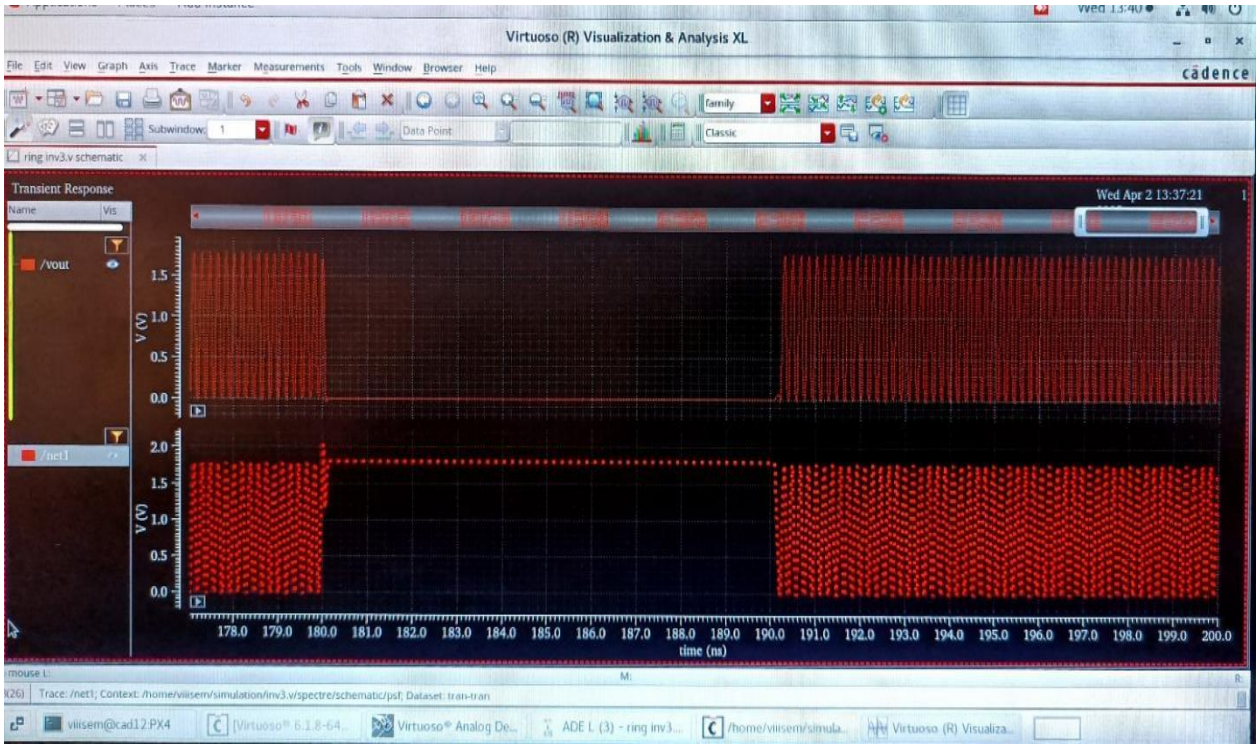

Figure 6. Output waveform of 3-stage ring oscillator

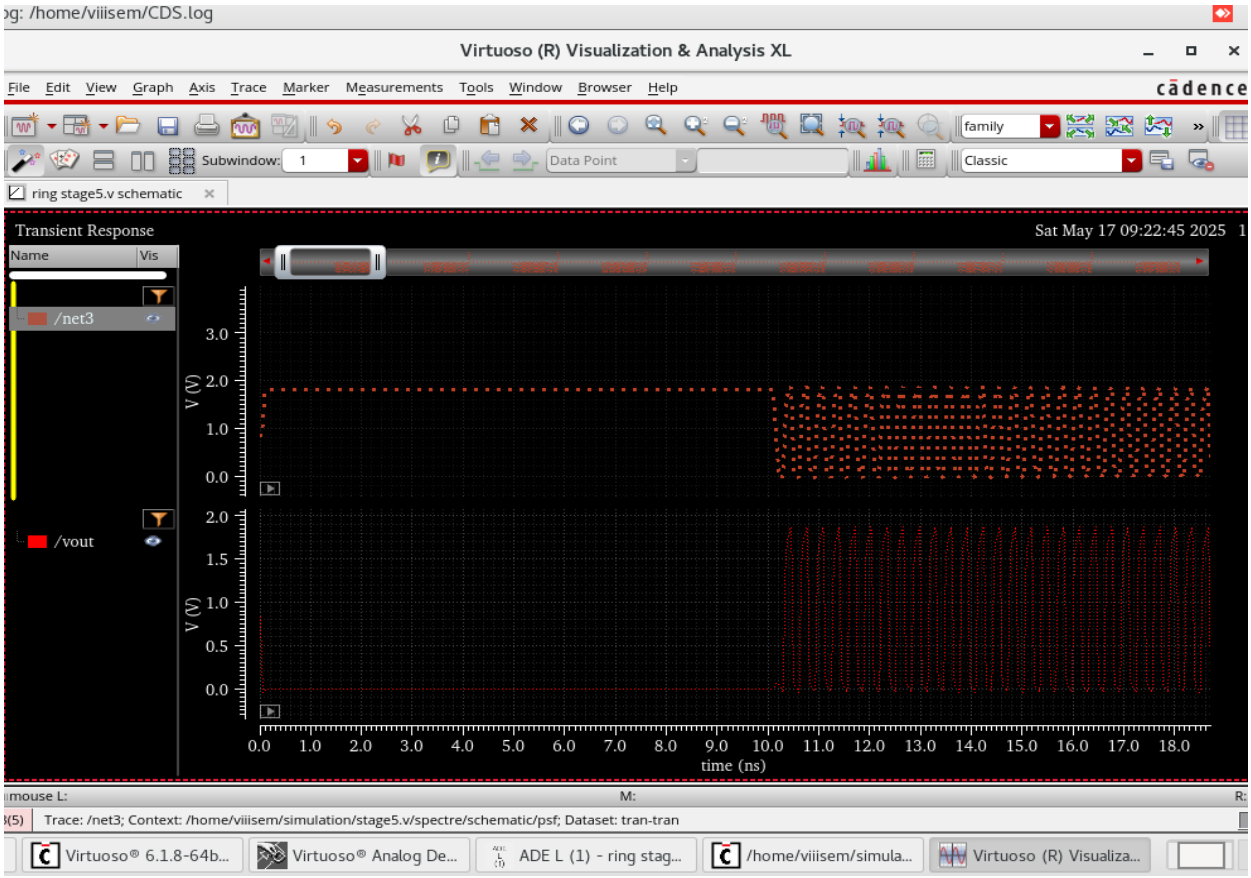

Figure 7. Output waveform of 5-stage ring oscillator

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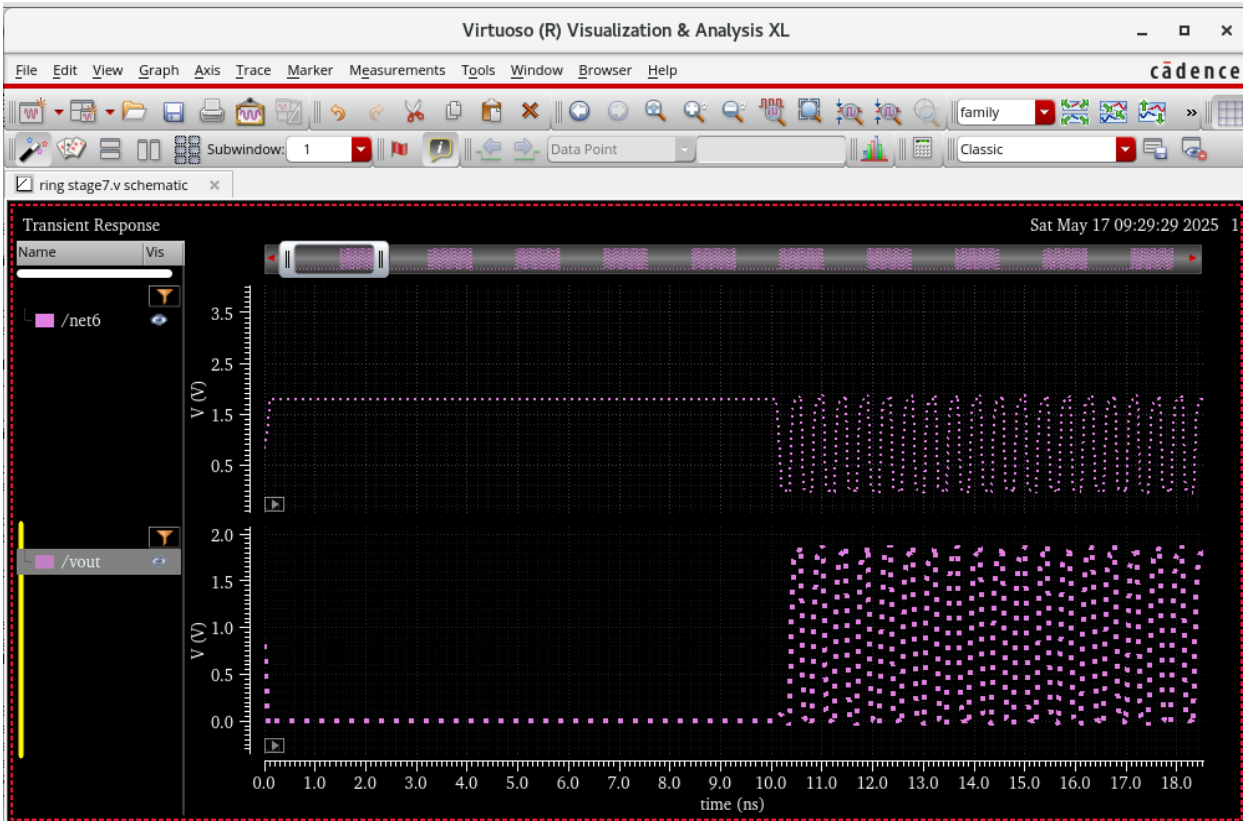

Figure 8. Output waveform of 7-stage ring oscillator

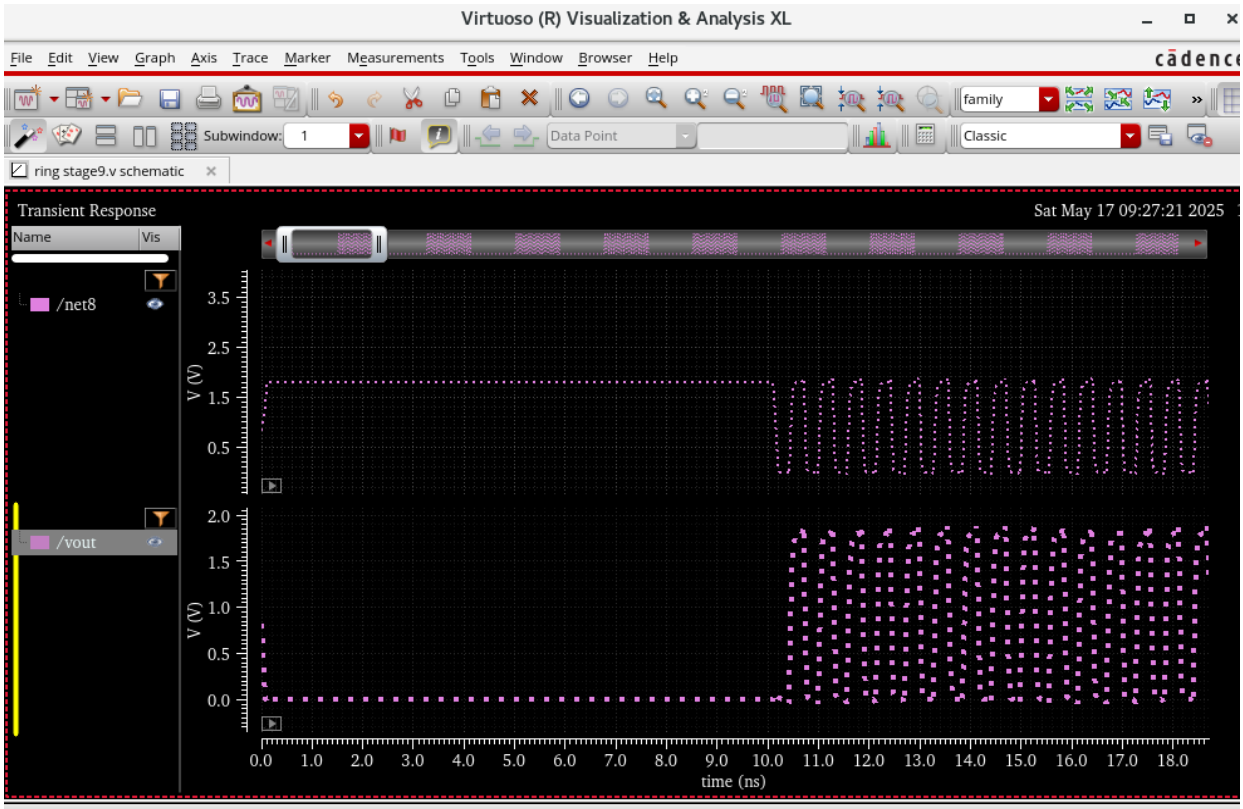

Figure 9. Output waveform of 9-stage ring oscillator

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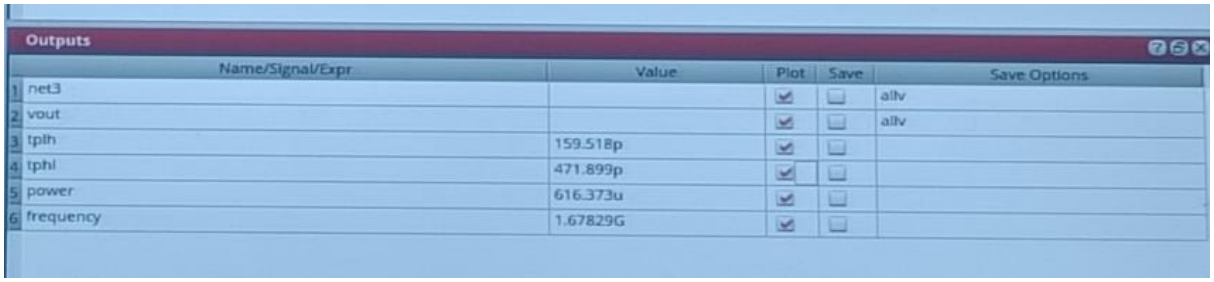
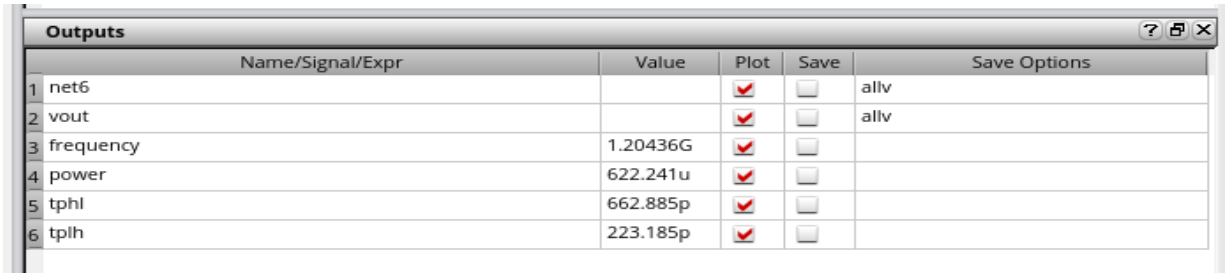


Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	net3		☑	☐	allv
2	vout		☑	☐	allv
3	tplh	159.518p	☑	☐	
4	tphl	471.899p	☑	☐	
5	power	616.373u	☑	☐	
6	frequency	1.67829G	☑	☐	

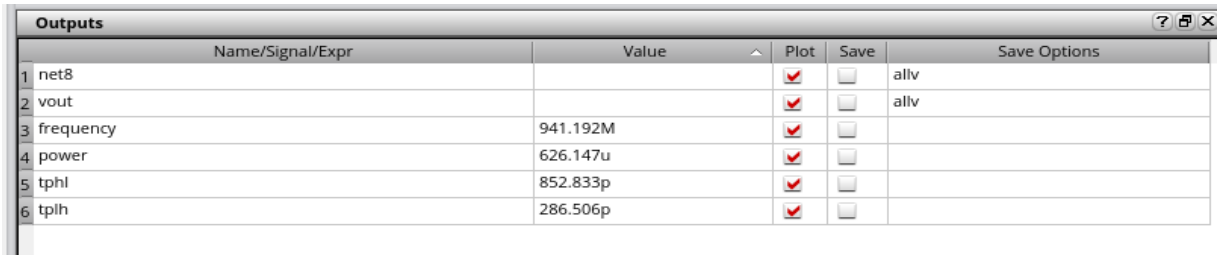
Figure 10. Delay, Frequency and Power calculation of 5 stage ring oscillator



Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	net6		☑	☐	allv
2	vout		☑	☐	allv
3	frequency	1.20436G	☑	☐	
4	power	622.241u	☑	☐	
5	tphl	662.885p	☑	☐	
6	tplh	223.185p	☑	☐	

Figure 11. Delay, Frequency and Power calculation of 7 stage ring oscillator



Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	net8		☑	☐	allv
2	vout		☑	☐	allv
3	frequency	941.192M	☑	☐	
4	power	626.147u	☑	☐	
5	tphl	852.833p	☑	☐	
6	tplh	286.506p	☑	☐	

Figure 12. Delay, Frequency and Power calculation of 9 stage ring oscillator

The important performance parameters like frequency, delay, and power consumption were measured for different stages of ring oscillator. In a ring oscillator, with increase in number of stages, the delay is increased. The power consumed by the 5-stage oscillator is minimum and from the table, it can be shown that power consumption is 0.34µW for 5-stage while it is 0.61µW for 9-stage ring oscillator. Also the frequency achieved is maximum 1032 MHz for 5-stage ring oscillator.

Parameters	5-stage	7-stage	9-stage
Power consumption	616.373µW	622.241µW	626.147µW
Average delay	315.7ps	443ps	569.65ps
frequency	1.678 GHz	1.204 GHz	941.192 MHz

Figure 13. Comparison of Performance Parameters for 5,7,9 Stages

VI. CONCLUSION

In this project, the CMOS design and performance characteristics of ring oscillators with varying numbers of stages were thoroughly analysed. The simulation results confirmed that the number of inverter stages significantly impacts key performance metrics such as oscillation frequency, power consumption, and propagation delay.

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It was observed that as the number of stages increases, the frequency of oscillation decreases due to the cumulative delay of each stage, while power consumption generally increases due to higher switching activity. The optimal number of stages depends on the intended application, balancing between frequency requirements and power efficiency. The analysis underscores the importance of stage selection in designing ring oscillators for specific use cases, particularly in VLSI circuits where low power and high speed are critical. Overall, the project demonstrates a successful implementation and evaluation of CMOS ring oscillators, providing valuable insights for further development in timing circuits and clock generation.

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