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Desgin of Low Power Asynchronous SAR ADC in CMOS Technology

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Abstract: This project presents the design of a low power Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) using asynchronous techniques. Traditional synchronous SAR ADCs suffer from clock-related power consumption and timing issues, especially at low sampling rates. By adopting an asynchronous architecture, this design eliminates the need for a global clock, thereby reducing dynamic power dissipation. The circuit employs event-driven control logic to trigger operations, resulting in improved energy efficiency. A capacitor-based DAC and a dynamic comparator are used to further minimize power usage. The proposed ADC achieves high resolution and low latency while maintaining a compact layout. Simulations are performed to validate the power-performance trade-offs. The design is suitable for low-power applications such as biomedical devices and IoT sensors. The project demonstrates how asynchronous design can significantly enhance SAR ADC efficiency for modern low-energy systems.

Keywords: SAR ADC, Synchronous SAR ADC, Energy efficiency, Capacitor-based DAC, Dynamic comparator, Compact layout, Simulations, Biomedical devices, IoT sensors

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are critical components in a wide range of electronic systems, enabling the interface between the analogy real world and digital signal processing units. As the demand for battery-powered and energy-efficient devices continues to grow—particularly in applications such as implantable biomedical systems, wireless sensor networks, and Internet of Things (IoT) platforms—designing low-power, compact, and high-resolution ADCs becomes increasingly important. Among the various ADC architectures, the Successive Approximation Register (SAR) ADC has emerged as a preferred choice for moderate-speed and medium-resolution applications due to its simple architecture, low power consumption, and scalability. However, traditional SAR ADCs are typically implemented using synchronous clocked control logic. This reliance on a high-frequency global clock results in unnecessary power consumption, increased electromagnetic interference (EMI), and challenges in achieving timing closure, especially at lower sampling rates.

To address these limitations, this work proposes the design of a low-power asynchronous SAR ADC using CMOS technology**.** The design eliminates the need for a global clock by employing event-driven asynchronous control logic**,** where each conversion step is triggered by the completion of the previous operation. This results in reduced dynamic power dissipation and improved energy efficiency. Additionally, the proposed ADC architecture incorporates a capacitor-based DAC for low leakage, and a dynamic comparator to avoid static power consumption during decision making. The asynchronous architecture not only minimizes unnecessary switching activity but also allows for natural data-dependent timing, which reduces conversion time variability and improves overall performance. The design achieves an optimal trade-off between resolution, speed, and power consumption while maintaining a small silicon footprint, making it highly suitable for applications where energy efficiency is paramount.

This paper presents the detailed design methodology, architectural features, control logic, and simulation results of the proposed SAR ADC. Key performance metrics such as Effective Number of Bits (ENOB), power consumption, conversion speed, and layout area are evaluated and discussed. Simulation and analysis are conducted using standard CMOS process technology, and results validate the potential of asynchronous SAR ADCs as a viable solution for next-generation ultra-low power electronic systems.

II. BLOCK DIAGRAM

The architecture of the proposed low-power asynchronous SAR ADC is illustrated in Fig. 1. The converter operates without a global clock, relying instead on event-driven handshaking to perform successive approximation. The design

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consists of the following key components: a sample-and-hold circuit, a comparator, an N-bit digital-to-analog converter (DAC), asynchronous SAR control logic, and an output register.

A. Sample-and-Hold Circuit

The analog input voltage VINV {IN} VINis first sampled and held by the sample-and-hold circuit. This block captures the instantaneous value of the input signal and maintains it constant throughout the entire conversion process. Accurate sampling is crucial for ensuring high resolution and noise immunity during conversion.

B. Comparator:

The comparator is a dynamic circuit that compares the held input voltage with the analog output of the DAC. Based on the comparison result, it generates a binary output that is fed into the SAR control logic. The use of a dynamic comparator helps reduce static power dissipation and contributes to the low-power objective of the design.

C. N-bit DAC:

The digital-to-analog converter (DAC) generates a reference voltage based on the current digital approximation stored in the SAR logic. A binary-weighted capacitor array or charge redistribution DAC is typically used for this purpose. The output of the DAC is compared with the input voltage in each successive approximation step to refine the digital result.

D. Asynchronous SAR Logic:

Unlike conventional SAR ADCs that rely on a high-frequency clock, the proposed design employs asynchronous SAR logic. This block controls the bit-by-bit conversion sequence through a self-timed, handshake-based mechanism. Each bit decision is triggered by the completion of the previous comparator operation, significantly reducing unnecessary switching and improving energy efficiency. This event-driven approach eliminates clock skew issues and enables adaptive timing based on process and environmental variations.

E. Output Register:

After completing all NNN comparison cycles, the final digital code is stored in the output register. The End-of-Conversion (EOC) signal is then asserted, indicating that the conversion is complete and the digital output DOUTD {OUT} DOUT is ready for use by downstream digital circuitry.

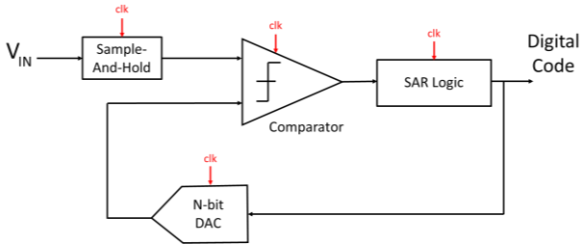

Fig 1. Block diagram

III. CIRCUIT IMPLEMENTATION

A. Sample and Hold circuit:

A Sample and Hold (S/H) circuit is used to capture and maintain the voltage of an analog signal at a specific instant, enabling accurate analog-to-digital conversion. The circuit samples the input signal when a clock signal is high, allowing the NMOS transistor switch to conduct and charge a capacitor to the input voltage. When the clock goes low, the switch turns off, isolating the capacitor which holds the sampled voltage steady during the hold phase.

The capacitor (typically very small, e.g., 1 pF) quickly charges to the input voltage but must maintain it without significant voltage drop, which is ensured by a buffer amplifier with high input impedance and low output impedance. This buffer prevents the capacitor from discharging due to load effects. By freezing the signal voltage during conversion, the Sample and Hold circuit enables precise digitization of rapidly changing analog signals, making it vital in systems like ADCs, digital oscilloscopes, and data acquisition units.

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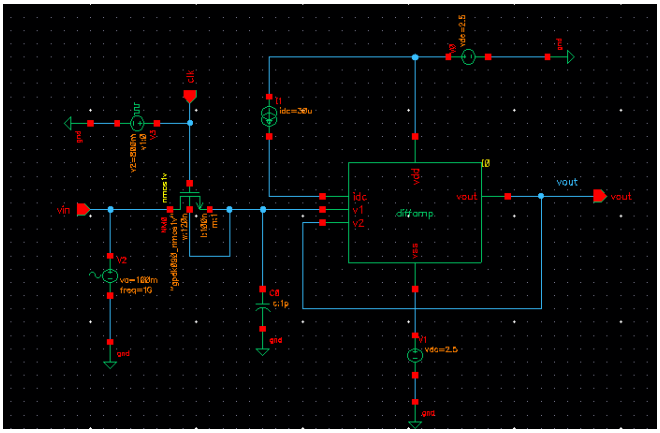

Fig 2. Schematic Diagram of Sample and Hold Circuit

B. Comparator

The comparator is among one of the main power consuming blocks in this architecture. So, most of the time of this work was spent on designing this block. The analysis was done in such a way so that the MOS transistors used in comparator remain in saturation, which is the main criteria for amplification. Also, the differential amplifier was used for its implementation so that the noise effect is reduced.

The comparator produces a logic output high or low based on the comparison of the analog input with the reference voltage. The comparator implemented in this work has better speed of operation and good resolution.

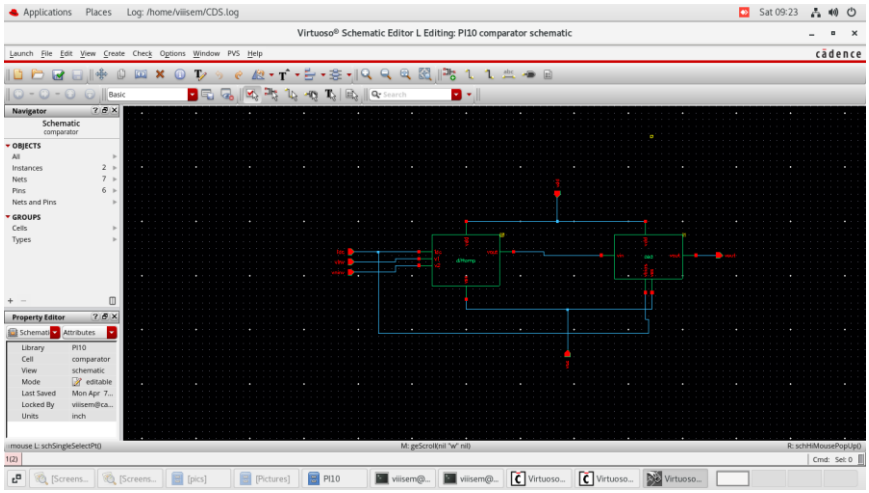

Fig 3. Schematic Diagram of Comparator

A differential amplifier amplifies the voltage difference between two input signals (V_1 and V_2). The basic schematic includes two transistors sharing a common emitter (or source) resistor, forming a balanced pair. It uses a current source at the emitter tail to ensure stable operation and high common-mode rejection. The collector (or drain) terminals are connected to load resistors or current mirrors. The output is usually taken between the two collectors, giving a differential voltage output. This circuit is widely used in analog systems like op-amps, ADCs, and sensor interfaces for accurate signal comparison.

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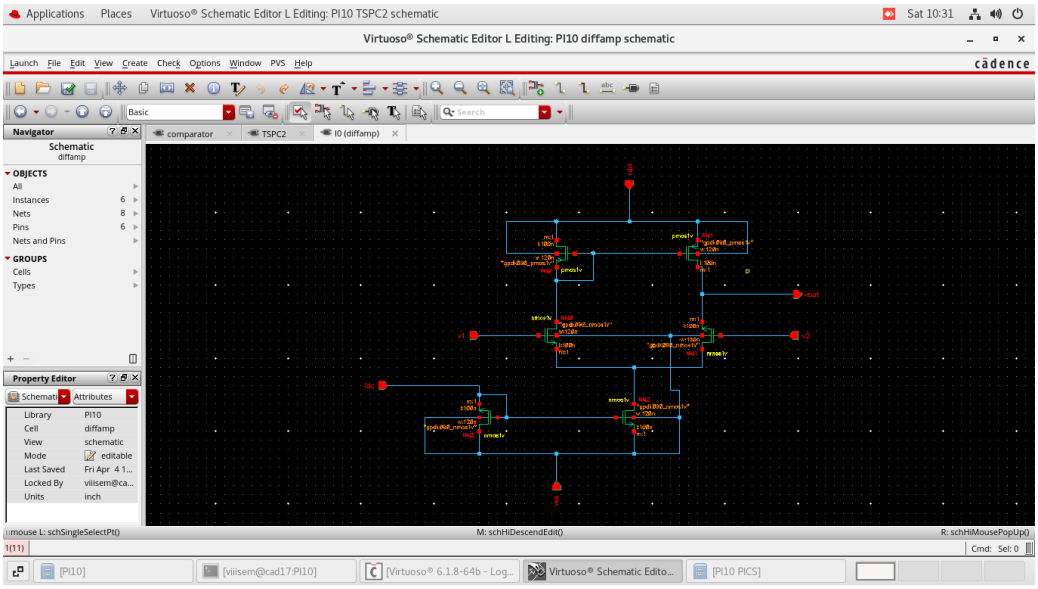

Figure 4. Schematic Diagram of Differential Amplifier

A common source amplifier is a basic MOSFET amplifier configuration used for voltage gain. The MOSFET's source terminal is connected to ground (common), the input is applied at the gate, and the output is taken from the drain. A drain resistor (RD) is used to develop the output voltage. A coupling capacitor is placed at the input to block DC and allow AC signals. A biasing network sets the operating point of the MOSFET in the active region. This amplifier provides high voltage gain and is commonly used in analog circuits.

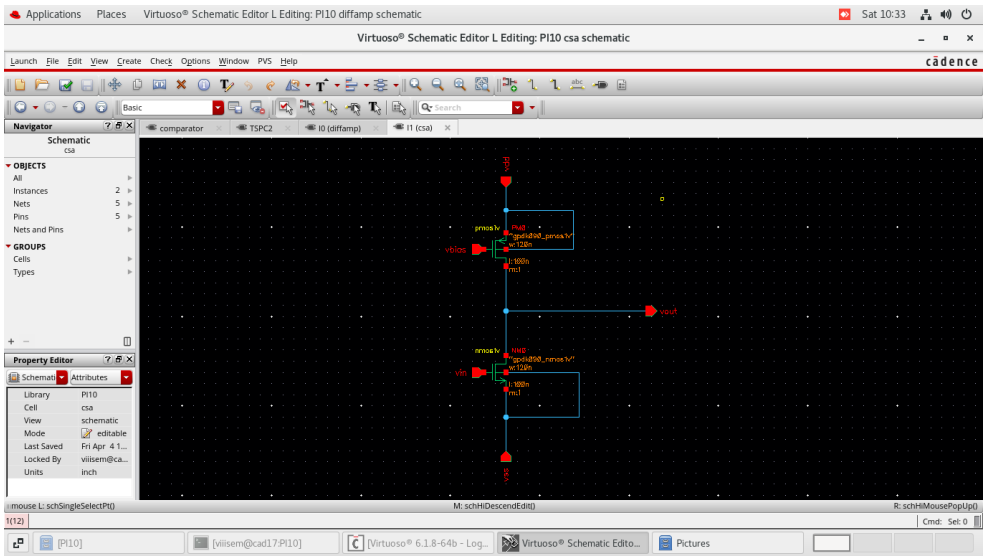

Fig 4. Schematic Diagram of Common source Amplifier

C. Digital to Analog Converter

There are many ways for implementing DAC such as weighted binary resistors, weighted capacitor method, split capacitor array, etc. each type has its pros and cons. In case of binary weighted resistor array type of DAC the area requirements increases as the number of bits increases. Also, the matching of resistor values setting becomes complex. The same problems occur in the weighted capacitor type of DAC; however, it consumes less area than the former type. Split capacitor method further reduces the area and power consumption, but it increases the parasitic capacitance. The DAC block was implemented using R-2R ladder network so as to improve precision. In this only two resistor values are used which simplifies the task of matching problem. Accuracy and precision depends on the values of resistors chosen.

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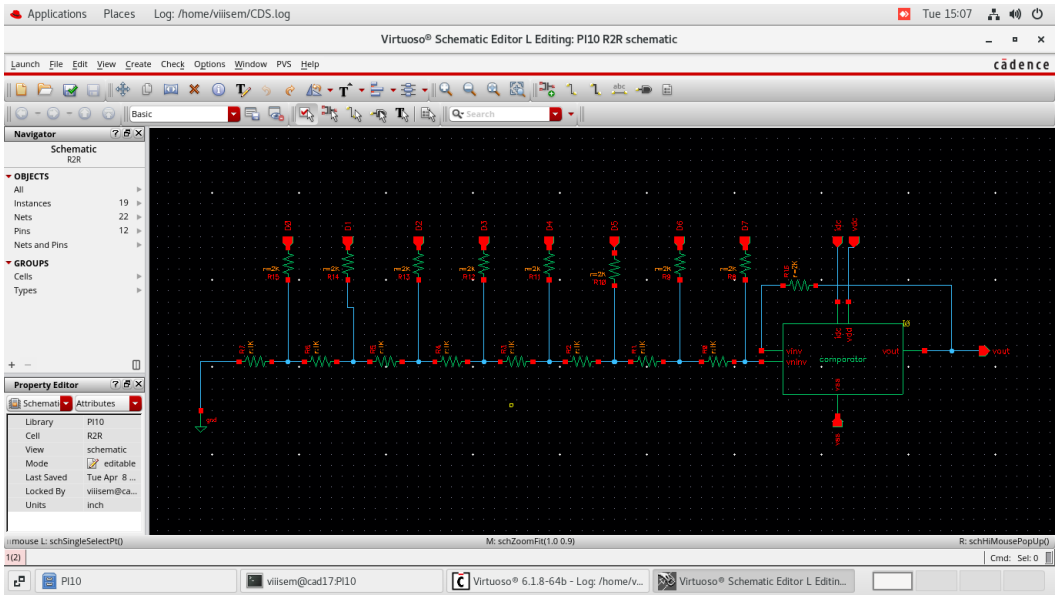

Fig 5. Schematic Diagram of R-2R DAC

The R-2R Digital-to-Analog Converter (DAC) uses only two resistor values: R and 2R, arranged in a ladder network. In an 8-bit R-2R DAC, 8 digital input bits control 8 switches that connect each ladder node to either a reference voltage (Vref) or ground. The weighted binary inputs are converted into an analog output voltage proportional to the input value. The schematic consists of a resistor ladder, switches controlled by input bits, and an op-amp as a summing amplifier. In a testbench, various 8-bit binary inputs are applied to verify the accuracy and linearity of the analog output. This design is simple, scalable, and widely used due to its efficiency and precision with minimal components.

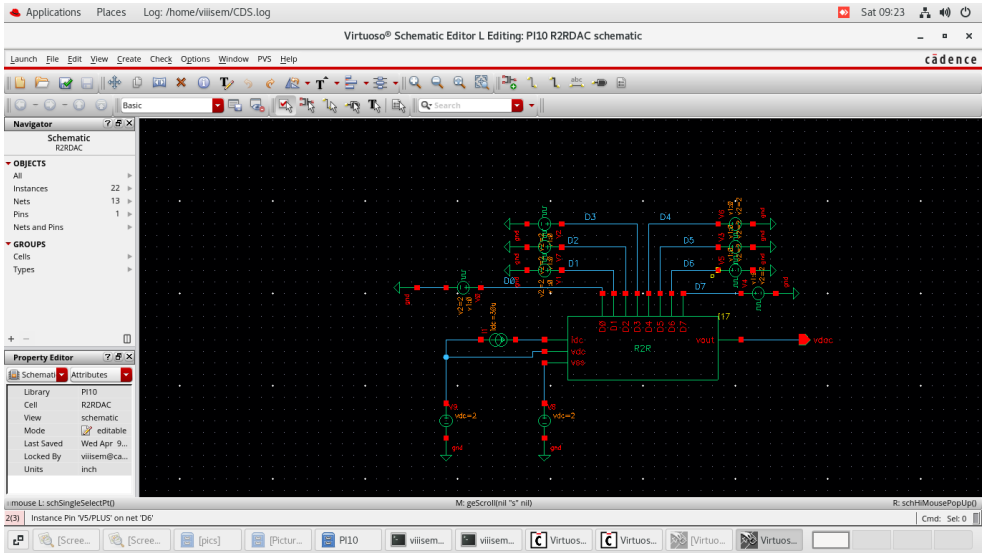

Fig 6. Schematic Diagram of R-2R DAC with 8 bit input (Test bench)

D. Successive Approximation Register Logic

Successive Approximation Register (SAR) control logic determines each bit successively. Basically the Successive Approximation (SA) register contains N flip flops for an N-bit ADC and some combinational logic. It implements the binary search algorithm for its operation. SAR ADC performs the binary search through all possible bits. Each bit has three possibilities: it can be set to '1', reset to '0', or maintains its value. The operation is briefly explained as:

At the start of conversion cycle, the SAR is reset by holding a start signal high. On the positive edge of first clock pulse MSB bit is set to '1' and other bits are reset ('0'). The DAC then generates analog equivalent of this digital word. The comparator compares the DAC output with the sampled analog input signal. If the DAC output is lower than the sampled

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input, the comparator gives LOW output and the SAR MSB will be reset ('0'). If the DAC output is higher than the sampled input, the comparator gives HIGH output and the SAR MSB will be retained and on the positive edge of the next clock pulse the next MSB will be set ('1'). The same process is repeated for the other bits until each bit of SAR is determined. As soon as LSB is tried the SAR forces the conversion complete signal HIGH to enable the latch to give the valid data in digital form. In this case "N+1" clock cycles are required for "N" bit ADC.

There are two approaches to designing the SAR logic. The first one consists of a ring counter and a shift register. In this case 2N flip flops are required. The other approach requires N flip flops and some combinational logic. In this paper second approach was used.

IV. SIMULATION RESULT

To verify the functionality and performance of the proposed Low-Power Asynchronous SAR ADC, simulations were performed using Cadence Virtuoso with a 45nm CMOS technology. The presented work has been implemented in Cadence Virtuoso in 180nm technology and different types of analysis viz: transient, ac, and dc analysis was performed for different sub-blocks separately. For evaluating the power consumed in each block, calculator option was used. Different waveforms 4216 that resulted after simulation are shown in the following figures (Fig.7 to Fig. 9). Fig. 7 shows the transient response of the Sample and Hold circuit (shown in Fig. 2) in which Vclk is the clock signal applied at the gate terminal of MOS transistor and it controls the on off state of the MOS switch. Vin is the input analog signal (that is to be sampled) and is applied at the source terminal of the MOS switch. Depending on the state of the clock or control signal the switch is on or off and it takes the samples of Vin accordingly, and hence at the output we get the sampled (Vs) signal. The power consumed by S/H block was almost zero. In Fig. 9 the response of the comparator (circuit diagram shown in Fig. 3) is plotted. One of the terminal is grounded and at the other terminal (inverting terminal) the input signal (Vin) is applied. The comparator compares the two inputs and at the output we get the amplified output accordingly. If the input at the inverting terminal is more than that at the non-inverting terminal, the output will go in negative cycle, and vice-versa.

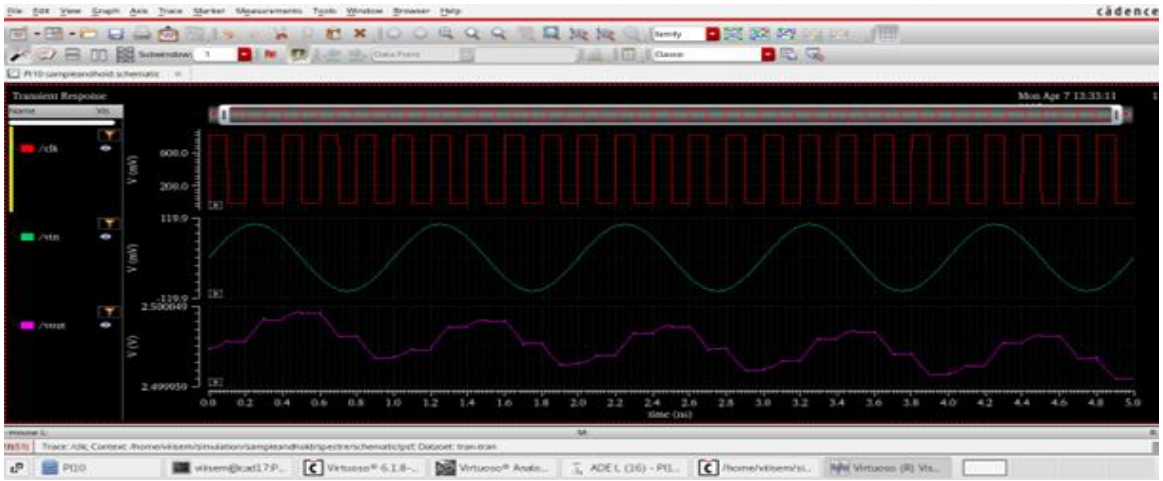

Fig 7. Output of sample and hold circuit

The waveform (shown in Fig. 8) shows the transient response of a Low-Power Asynchronous SAR ADC. It illustrates the timing of control signals (D3–D7) along with the output voltage (Vadc), confirming proper switching operation and ADC output generation over time.

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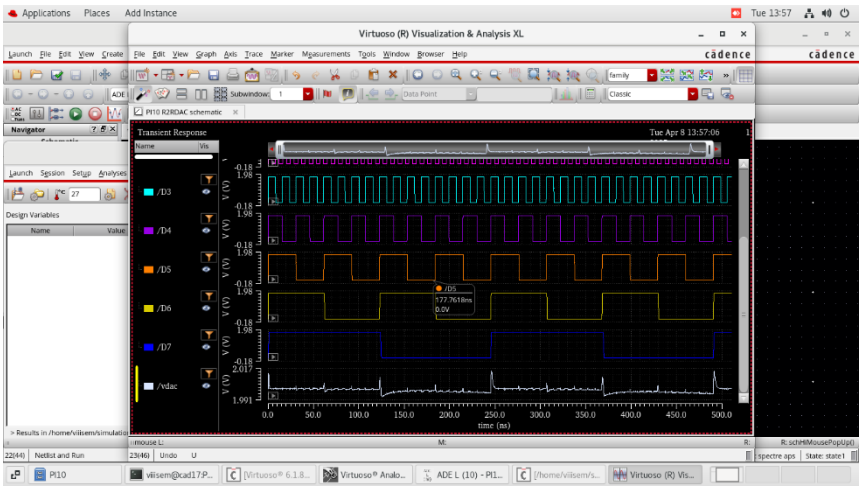

Fig 8. Output waveform of an R2R DAC

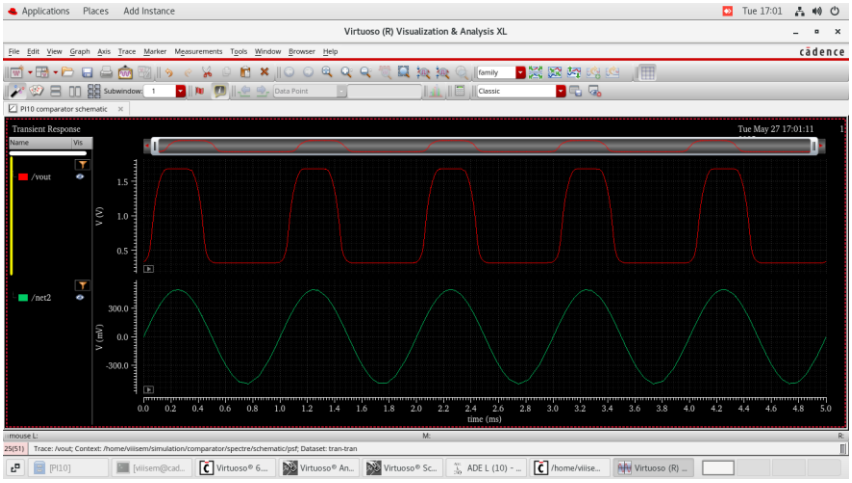

Fig 9. Output waveform of a comparator

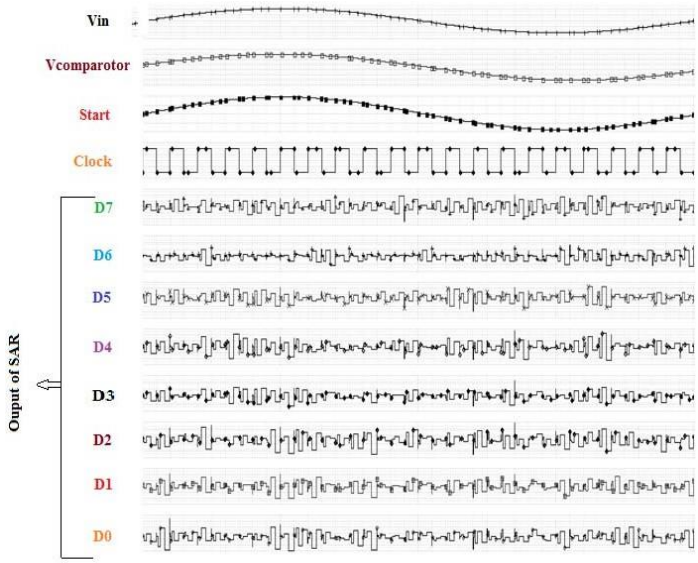

Fig 10. Transient Response of SAR ADC

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V. CONCLUSION

In this project, the design and implementation of a low-power Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) using asynchronous techniques in CMOS technology have been successfully presented. The asynchronous architecture eliminates the need for a global clock, significantly reducing power consumption and improving energy efficiency compared to conventional synchronous designs. The proposed ADC leverages CMOS technology, which offers advantages in terms of scalability, low leakage currents, and cost-effective integration. The designed SAR ADC achieves high resolution and accuracy while maintaining low power consumption, making it highly suitable for modern portable, biomedical, and IoT applications where energy efficiency is critical. This project highlights the potential of asynchronous techniques in advancing the performance of ADCs, contributing to the development of next-generation low-power electronic systems.

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