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Design and Implementation of FPGA controlled Nine Level Inverter

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Abstract: In this paper a nine-level staggered multi level inverter (MLI) by FPGA controller is presented. This inverter produces nine levels of AC output voltages with the effective gate signal design. The proposed inverter needs a single DC voltage supply with chain connection of four capacitors, five diodes, eight switches to synthesize output voltage levels and H-bridge cell. With single DC voltage source the present inverter eliminates the impartial allocation of DC voltage sources and switches. The switching losses and voltage stresses in the present converter are reduced. The total harmonic distortion (THD) in the output voltage is also less when compared to conventional topologies. The proposed work is first simulated in MATLAB/Simulink environment and then implemented using FPGA controller with VHDL interface.

Index Terms: Multilevel inverter; voltage balance; AC output voltage; Total harmonic distortion (THD); FPGA controller.

I. INTRODUCTION

Multi level inverter is a power electronics converter circuit which has many topologies to synthesize AC output voltage near to sinusoidal nature with less harmonic content. The basic MLI produces two levels of output AC voltage which is called two level inverter. It is also called as conventional inverter which operates at high frequency leading to high amount of voltage stress and THD [1].

The design of SVPWM based 2-level or 3-level inverter is complex and is only used in medium power applications[4]-[5] To overcome the disadvantages in basic two and three level inverters, a high level inverter with effective gate pulse pattern is presented. The present MLI elevates the drawbacks of basic two level and three level inverters and it is used in high power applications by increasing its power rating [6].
Overall the MLI has numerous advantages like increase in voltage levels, decrease in harmonic content, low switching loss and voltage stresses. These MLIs are employed in high and medium power loads [7]-[14].

The performance analyzation of various MLIs can be done by observing the THD in output voltage and the number of levels in output voltage. The conventional MLI topologies are single phase bridge inverter, cascaded H-bridge and diode clamped inverter. Among these The THD in single phase bridge inverter is less when compared to other MLIs. The cascaded H-bridge inverter also has THD more than diode clamped inverter [16].

The block diagram of proposed MLI is shown in Fig. 1.The advantages of proposed MLI is it has less number of power components as they are used in sequential repetition approach. Also it becomes easy to send pulse signal to power components [17].

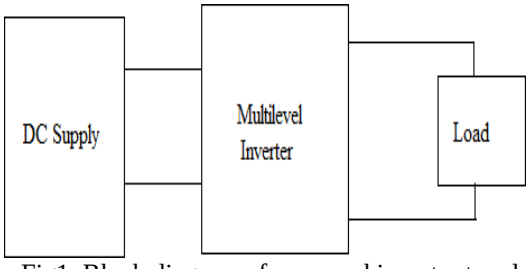

Fig1. Block diagram of proposed inverter topology

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II. SVPWM BASED MULTI LEVEL INVETER

A. 2-level SVPWM inverter

A 3-phase 2-level voltage source inverter (VSI) produces the output phase voltages in two levels i.e, +Vdc/2 or –Vdc/2 at any time as shown in Fig. 2

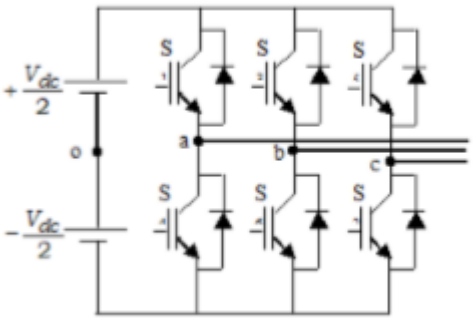

Fig.2 2-level SVPWM inverter

Here the required phase voltage is treated as Vref and it is synthesized using space vector pulse width modulation(SVPWM) algorithm.[4]

SVPWM based inverter produces eight space vectors from V_0, V_1,V_2…. through V_7 and they are designed as shown in Fig.3

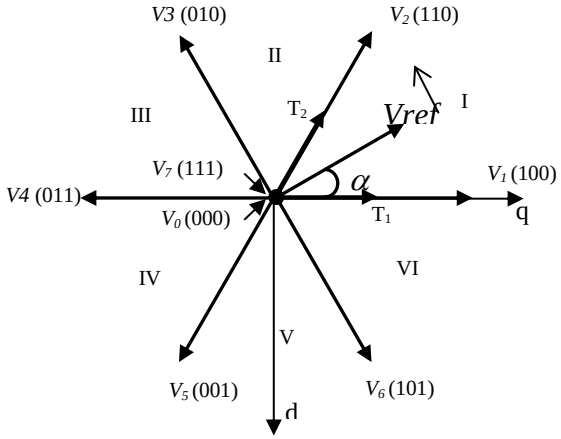

Fig. 3 Voltage space vectors of a 3-phase, 2-level VSI

The reference voltage vector (V_{ref}) or sample is the desired value of the fundamental components of output phase voltages, which is sampled at equal intervals of time, T_s referred as sampling time period. In each T_s, by using the active voltage vectors that are forming the boundary of the sector in which the sample lies and the zero voltage vectors over different time durations such that the voltage vector produced over T_s is equal to the V_{ref}. The principle of volt-time balance expression can be written for sector-I as in (1).

$$V_{ref}T_s = V_1T_1 + V_2T_2 + V_0T_0 + V_7T_7 \quad (1)$$

The inverter phase voltages at any instant are ±Vdc/2(two level voltages only)as shown in table. 1

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Table I. output phase voltages generated by a switching state

Switching state	Inverter phase voltages		
	V_{ao}	V_{bo}	V_{co}
V_0 (0 0 0)	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
V_1 (1 0 0)	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
V_2 (1 1 0)	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
V_3 (0 1 0)	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
V_4 (0 1 1)	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
V_5 (0 0 1)	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
V_6 (1 0 1)	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
V_7 (1 1 1)	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$

B.3-level SVPWM inverter

A dual two level inverter is implemented for MLI.This inverter is free from capacitor balancing issues and free from neutral point fluctuations.

The below figure 4 shows isolated dual two level inverter configuration which is capable of generating three level effective phase voltages (0,+Vdc/2,-Vdc/2) [5]

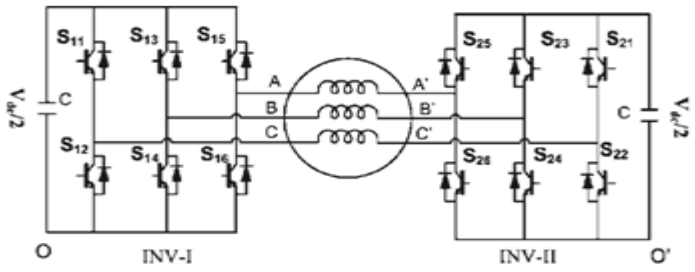

Fig.4. Dual two level isolated inverter

The synthesis of effective phase voltage is based on SVPWM algorithm. The following Figure 5 shows the SVPWM inverter based 2-level phase voltage(+Vdc/2 and –Vdc/2) [4]

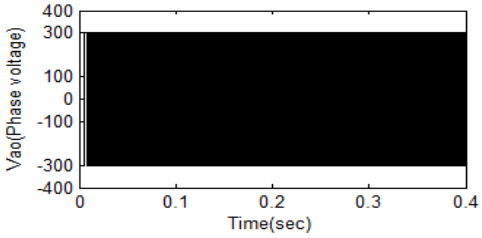

Fig. 5. 2-level output phase voltage

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The dual two level inverter is synthesized for three level output phase voltage(0,+Vdc/2 and –Vdc2)
As shown in figure 6 [5].

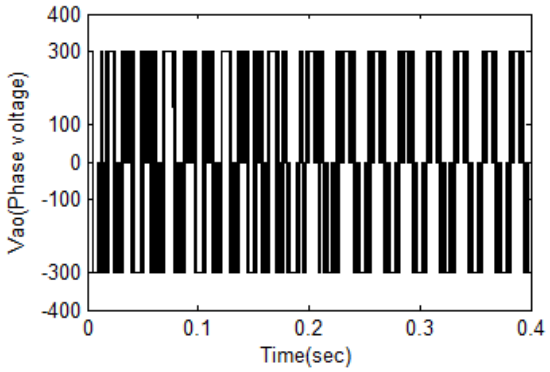

Fig. 6. 3-level output phase voltage

2 PROPOSED NINE LEVEL INVERTER CONFIGURATION

A. Circuit configuration

The proposed nine level inverter with single DC source is shown in Fig 7. The four capacitors across the DC source divides the voltage into equal parts. The voltage across each capacitor is observed as vdc/4. The nine output voltage levels which can be obtained in the output wave form are Vdc, 3Vdc/4, 2Vdc/4, Vdc/4, 0, -Vdc/4, -2Vdc/4, -3Vdc/4, -Vdc.

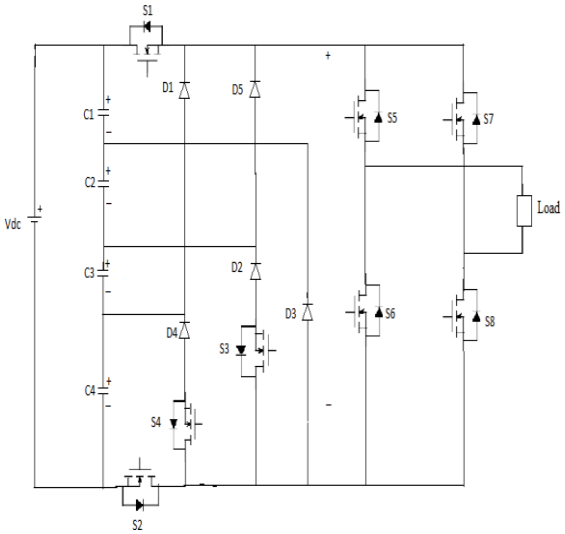

Fig7. Circuit configuration of a nine-level inverter

The polarity of the output voltage level depends on the configuration of the H- bridge cell [7].

B. SWITCHING SCHEME OF NINE-LEVEL INVERTER

The switching frequency of the output voltage is decided by selecting different pulse width modulation strategies[19]. Ther are different PWM strategies available for MLI configuration. In this paper, the required nine level output voltage is generated at the fundamental frequency. The design of the pulse generation circuit makes this topology differ from others to obtain the unique pulse pattern to turn on the switches at the proper instant [18]. Switches S1, S2, S3, and S4 need to be compulsorily unidirectional or else the output waveform will get distorted. The advantage of this circuit configuration is less number of switches [20]. Four DC sources utilized to generate nine-level MLI output results [15].
The switching pattern for a nine level inverter with reduced switches is shown in the following table.

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TABLE 2. SWITCHING TABLE FOR PROPOSED NINE-LEVEL INVERTER

Switches turn ON	Voltage Level
S1, S5, S8	Vdc
S2, S5, S8	Vdc/4
S3, S5, S8	2Vdc/4
S4, S5, S8	3Vdc/4
S7, S8	0
S1, S6, S7	-Vdc
S2, S6, S7	-Vdc/4
S3, S6, S7	-2Vdc/4
S4, S6, S7	-3Vdc/4

3. MATLAB SIMULATION AND RESULTS

The proposed nine-level inverter can be synthesized in MATLAB/Simulink environment. Input DC voltage sets to DC 40v, hence each capacitor voltage divides into DC 10v in this case. Frequency of ac output voltage set to 50 Hz. The switching scheme for this proposed topology is unique from others to obtain the unique pulse pattern to turn on the switches at the proper instant [13].

In the present work, the output voltage is obtained and measured without the filter. The output voltage waveform for this proposed topology without the filter is in staircase form. THD of the output voltage without the filter is found to be 11.37%. The Simulink block diagram of the proposed nine-level inverter with reduced switches is as shown in the below figure 8.

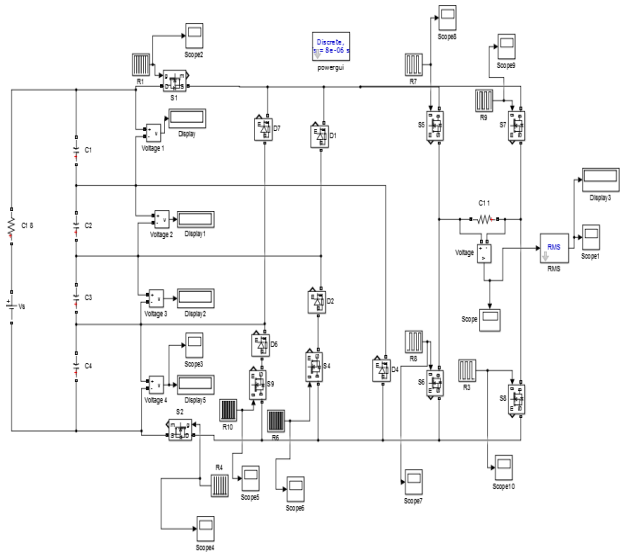

Fig 8. Simulink block diagram of the proposed nine-level inverter without filter

The figure 9 shows the simulation results of output voltage waveform without a filter in the staircase model for the proposed nine-level inverter.

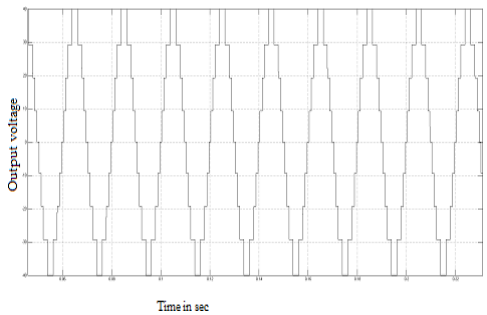

Fig 9. Simulation results of output voltage without a filter in the staircase model

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The THD of the output voltage is measured and shown in the Fig. 10. The THD is reduced as the number of output levels are increased. Here in this topology, the THD value of the output voltage without a filter is observed to be 11.37%.

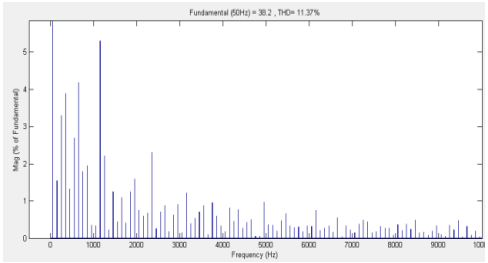

Fig10. THD of the output voltage without filter

4.HARDWARE IMPLEMENTATION

i.Block Diagram Description

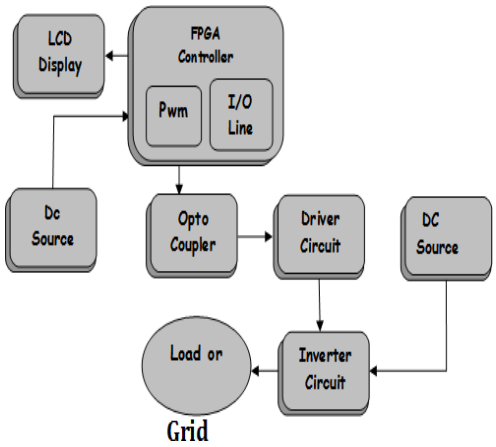

Fig 11. Block Diagram of Hardware implementation

The above Fig.11 shows the block diagram of the hardware implementation of nine-level inverter. The FPGA controller is for generating appropriate gate signals and the function of opto Coupler is to isolate the control circuit from the power circuit.

ii. Hardware description

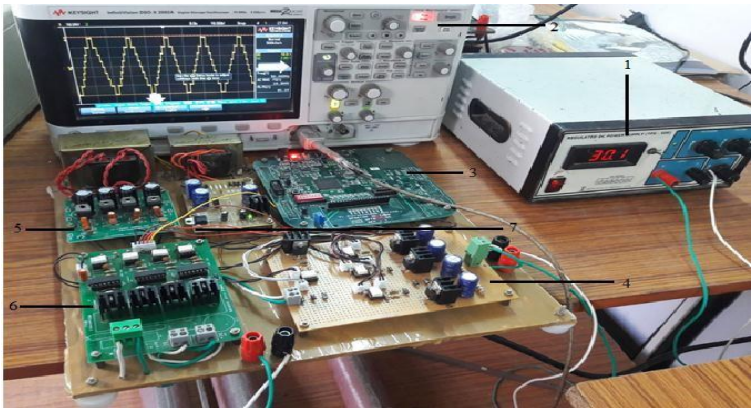

Fig 12 Hardware setup with inverter output

The hardware implementation of the nine level inverter using FPGA controller is shown in the above Fig. 12. The hardware setup is divided into different sections. They are

1. Input DC power supply
2. Digital signal oscillator
3. FPGA controller unit

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4. Driver unit
5. H-Bridge regulating unit
6. H-Bridge unit
7. FPGA & Driver regulating unit

Input AC signal is applied to the primary of the transformer and the transformer secondary has two outputs; one is 0-9V AC and another is 18-0- 18V.
Transformer secondary output is connected to the regulator through a full bridge rectifier and filtering capacitor. The diode is used for converting the AC voltage to DC voltage with AC ripples. Capacitor is used to remove the AC ripples. Regulator IC is for regulating the DC output voltage. The DC power supply energizes the driver circuit, FPGA controller and also act as input to the inverter.

The Practical Hardware set up gives nine-level inverter output which is shown in below Fig. 13

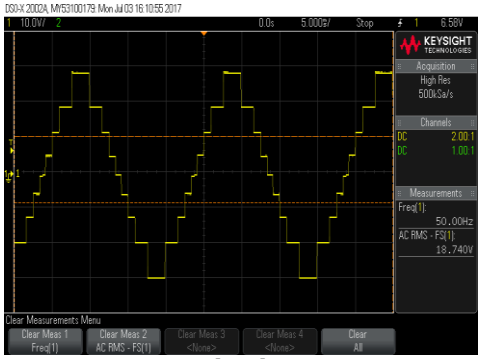

Fig13. Nine-level inverter output

Similarly practical hardware set up giving nine-level inverter current output is shown in below Fig. 14.

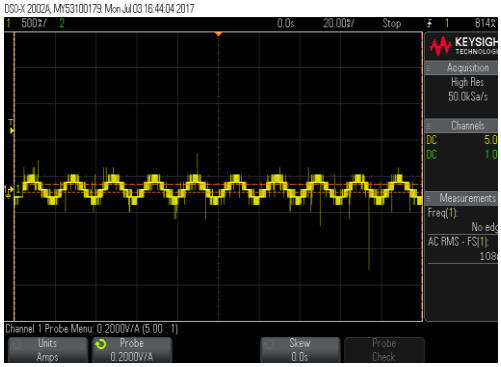

Fig14. Nine level inverter current output

The above two figures show the outputs of the nine-level inverter using a FPGA controller. The first one is voltage output waveform which is in staircase model and the second one is the current output which is also staircase form.

CONCLUSION

Thus, the performance of nine-level inverter, with a unique switching scheme is developed and practically implemented. To generate exact switching signals, the proposed system employs an FPGA controller. It produces nine-level output using the minimum number of switches. As a result, the proposed inverter can be a good substitute for conventional SVPWM inverters in the medium and high power rating applications.

FUTURE SCOPE

The scope of this work aims in the development of multilevel inverters with higher levels of output voltage and with the same number of switches with lower THD values. Also, the Photovoltaic source is used as a single dc input to the inverter system and which can be further improved using MPPT algorithms.

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