

for high-frequency and high-temperature can significantly enhance the speed and efficiency of integrated circuits. However, carbon nanotubes, graphene sheets can be produced at wafer scale, facilitating integration with existing CMOS manufacturing processes [7, 9, 12]. The graphene nanoribbon field-effect transistor (GNRFET), which utilizes narrow strips of graphene as the channel material, represents a significant advancement in nanoelectronics. GNRFETs, with their reduced size and improved electrostatic control, can offer higher performance and better EDP performance compared to conventional CMOS transistors. GNRFET model was designed for IoT devices, where each device may have one or more Graphene Nano-Ribbons (GNRs) [3-6].

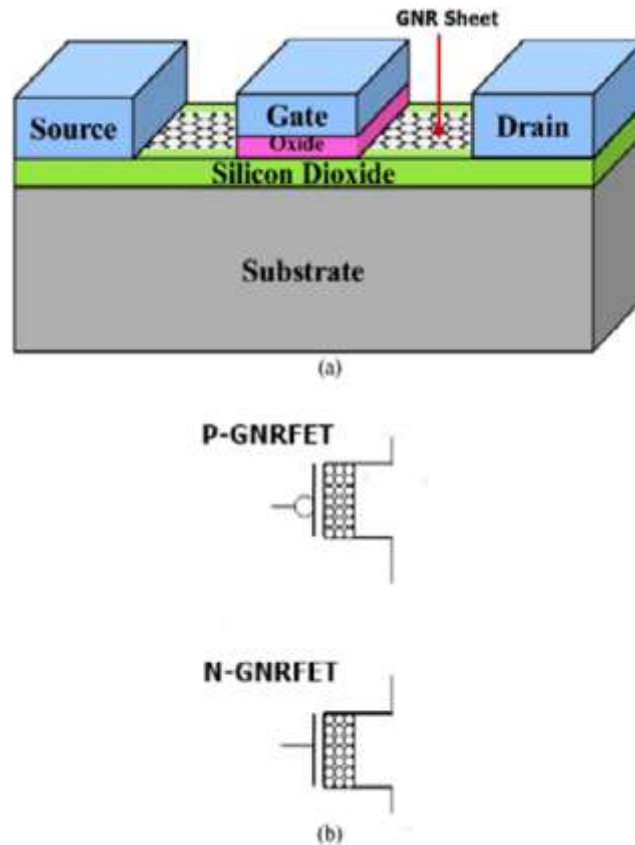


Fig. 2. (a) GNRFET Structure (b) GNRFET Symbol [3].

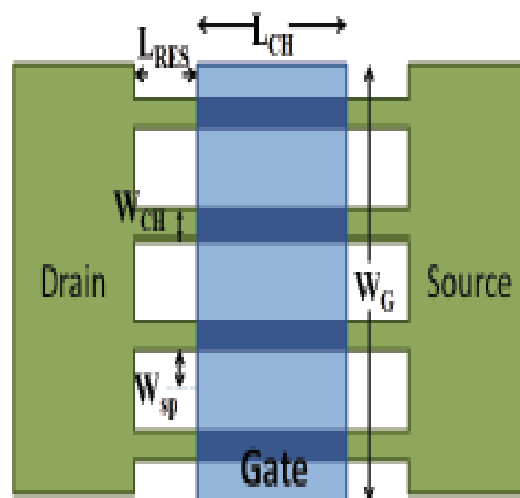


Fig. 3. The structure of a four-ribbon MOSFET-type GNRFET. A common drain and a common source are shared by the ribbons [3].

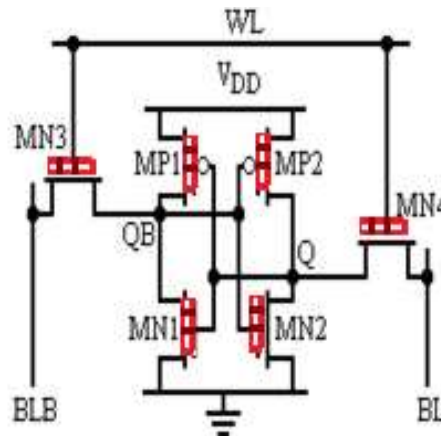


Figure 4: Proposed GNRFET based SRAM cell

III- SIMULATION AND ANALYSIS

Static Noise Margin of the SRAM cell depends on the cell ratio, supply voltage and also pull up ratio. For stability of the SRAM cell, good SNM is required that is depends on the value of the cell ratio, pull up ratio and also for supply voltage. Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation. Pull up ratio is also nothing but a ratio between sizes of the load transistor to the access transistor during write operation [11]. SRAM cell stability analysis is typically based on Static Noise Margin (SNM) investigation and SNM affects both read and write margin. This work represents the simulation of SRAM cells at different voltages and temperatures. All simulations of SRAM cells have been carried out at HSPICE tool.

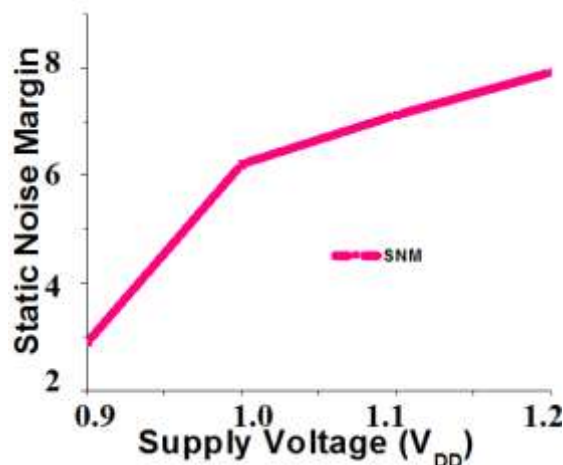


Figure 5 : SNM Vs Supply Voltage for Proposed GNRFET based SRAM

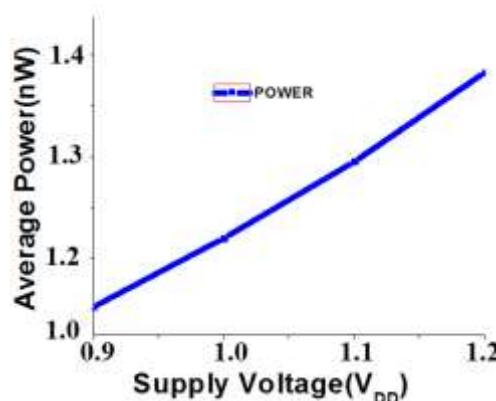


Figure 6: Average Power Vs Supply Voltage for Proposed GNRFET based SRAM

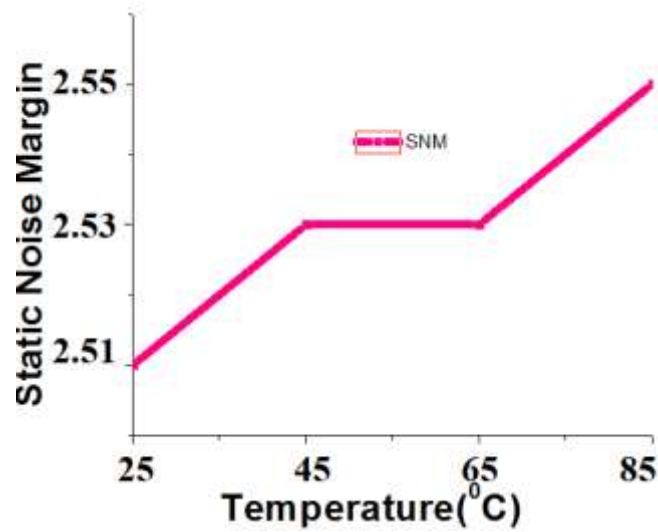


Figure 4: SNM Vs Temperature for Proposed GNRFET based SRAM

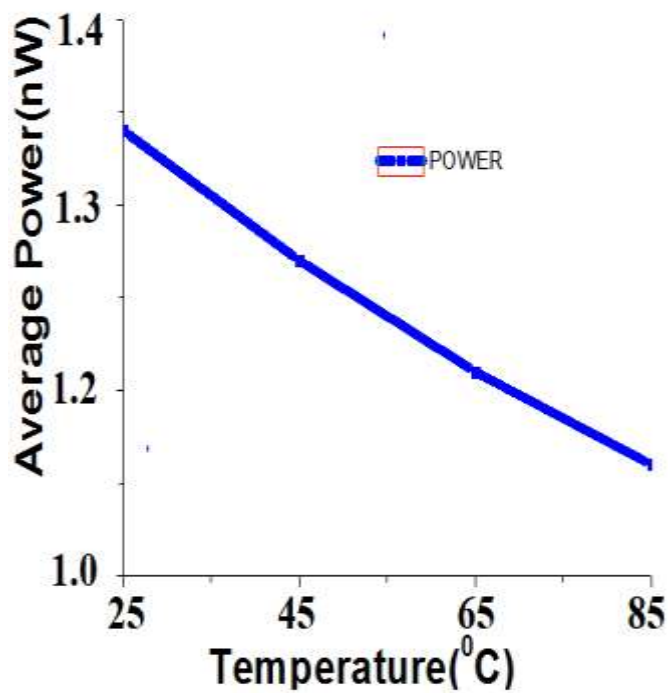


Figure 7: Average Power Vs Temperature for Proposed GNRFET based SRAM

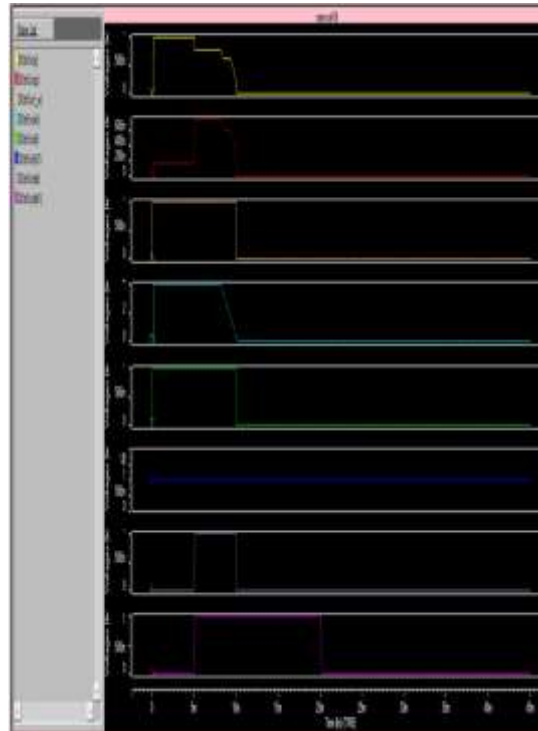


Figure 8: Waveforms at different node for Proposed GNRFET based SRAM

Table 1. Summary of the GNRFET Model used.

Device Types	n-type/p-type GNRFET
Device Dimensions:	
Channel Length	45nm
Channel Width (Minimum) per GNR	381.5nm
Number of GNRs / device	4
Oxide Thickness	2.5nm
Line Edge Roughness	20%
Doping Fraction	0.001

Table 2: Optimized Values of proposed SRAM using GNRFET

S. No.	Parameter	Value
1	SNM	6.7@1V
2	Average Power	2.24@1V
3	SNM	2.43@45°C
4	Average Power	1.25@45°C

IV CONCLUSION

In the Proposed GNRFET based SRAM, the Static Noise Margin analysis increasing with both supply voltage and temperature. The Power consumption is increasing with supply voltage but decreasing with temperature. The supply voltage also play vital role in SRAM cell stability during read mode of SRAM cell also by lower power supply may



reduce the leakage current for all cells in the memory. The word-line voltage, the bit-line voltage and the power-supply voltage all three voltages could be used to improve the SNM. GNR-FET reduces delay and improves speed and is highly efficient in terms of power dissipations, a key need of future Aeronautical Engineering and IoT applications. SNM is 6.7 at 1V, Average Power is 2.24 at 1V, SNM is 2.43 at 45°C, and Average Power is 1.25 at 45°C. These performance measuring parameters are sufficient for aeronautical applications in future IoT Devices.

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