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"USING ANTI-PARALLEL VOLTAGE SOURCES, A LOW-POWER MULTILAYER INVERTER WITH FEWER SWITCHES"

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Abstract: In this paper, a new cascaded multilevel inverter model is proposed. The anti-parallel voltage source unit is connected in series to execute the suggested model. Power switches connect the voltage sources in each of the separate units in parallel. By connecting further units, the output levels of the suggested model can be readily increased. Each unit has a different voltage magnitude than the others. The suggested model uses fewer power semiconductor switches, which lowers the total cost and complexity of the circuit. With the right input voltage magnitude assigned, the suggested inverter can produce high output steps with the fewest switches needed. Simulation results are used to validate the suggested multilayer inverter's performance. This is a description of the 63-level asymmetrical multilevel inverter simulation result.

I. INTRODUCTION

The multilevel inverter is widely utilized in many different applications, such as electric drive systems, FACTS devices, compensation equipment, interface devices, and converters. The benefits of these converter types—minimum switching losses, high power quality output, reduced electromagnetic interference, etc.Are drawing increased attention. Its ideal structure and modularity are the reasons for this. The multilayer inverter is a converter that takes a set of input dc voltage sources and outputs a stepped sinusoidal voltage.

The module that was released in employs complete bridge inverters to provide full stepped output and series/parallel voltage sources for positive stepped output. Each unit needs to be connected to the others in series. The architecture makes use of full bridge units coupled in series with voltage sources to provide output levels up to 125. However, a large number of switches will be utilized. Along with a full bridge inverter, the concept proposed in also makes use of the series parallel voltage sources technique. To connect voltage sources in series and parallel, extra switches are used. For a single unit, five switches are used. The switch count will grow in tandem with a level increase.

The main benefit of all these current topologies is that fewer input voltage sources may be needed, but more power semiconductor switches will be needed for a higher number of levels. The circuit gets more complex as the number of switches utilized in it increases. This is due to the fact that every switch needs to be managed by separate isolation and protection circuits. As the number of switches increased, so did the switching losses. For an efficient module, the number of switches must be decreased. This4 research proposes a new cascaded multilevel inverter module that may generate several output levels while utilizing the fewest power switches and driving circuits possible.

The suggested module is contrasted with a few current topologies according to the quantity of switches and sources utilized at each output level. The MATLAB Simulink environment validates the performance of the proposed 63-level cascaded multilevel inverter and provides simulation results.

II. PROPOSED METHOD

This chapter explains the suggested cascaded multilayer inverter's concept. Fig. 1 depicts the basic unit of the suggested model. Two power switches and two voltage sources make up each device. Through the power switches, the voltage sources are connected in an anti-parallel fashion. These switches regulate the output voltages of each individual unit. Every switch has a source connected to it that it controls. If the switches are not connected correctly, the power switch's anti-parallel diode will allow the input voltage to flow through it even when the switch is not in the ON position. There will be no voltage across the associated equipment while these two switches are in the OFF position.

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There are three states: –V1, +V1, and 0. Depicts the generalised model of the suggested multilevel inverter. The separate units are connected in series based on the output levels. Each unit's voltage magnitude needs to be assigned correctly.

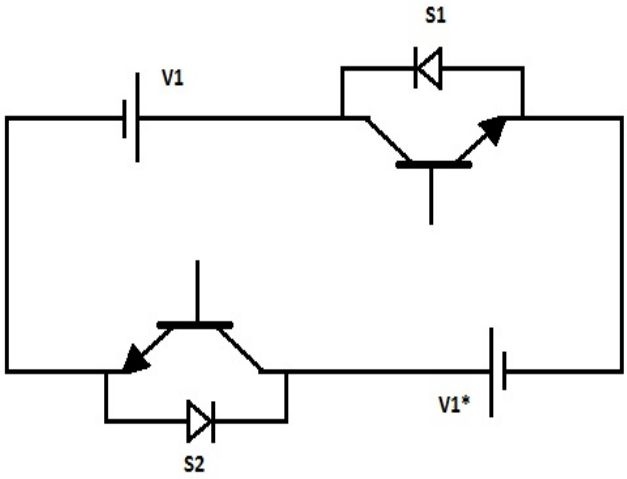

Fig 1: Basic unit of the proposed topology

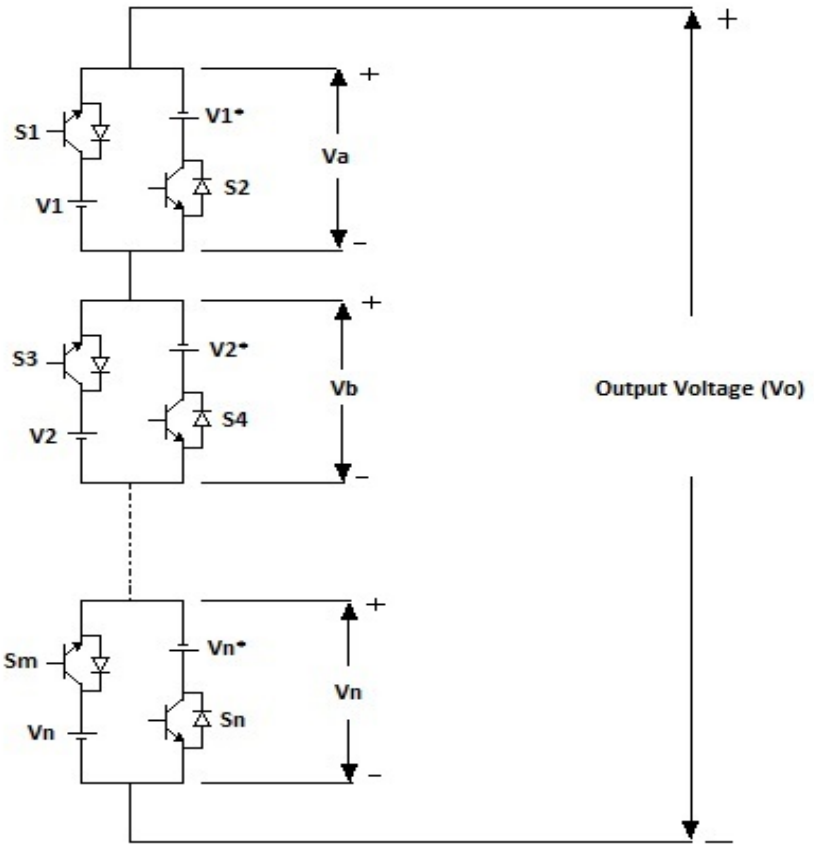

Fig 2: Generalized model of the proposed topology

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Without requiring a whole bridge inverter circuit, the output voltage can be readily obtained by employing the anti-parallel voltage source. In addition, compared to the current topologies, the suggested design has a few more voltage sources than the previous ones. However, the suggested converter uses a significantly smaller number of switches overall. Fig 2 depicts the usual configuration of the suggested 63 level asymmetrical multilevel inverter. Four antiparallel voltage source units are utilised in total for the 63-level model, and they are all coupled in series.

Eight input voltage sources are needed for the proposed inverter because two voltage sources are employed for each unit. The symbols V1, V1*, V2, V2*, V3, V3*, V4, and V4* represent the voltage inputs. The symbols V1, V1*, V2, V2*, V3, V3*, V4, and V4* represent the voltage inputs. Every unit should have an identical voltage input. In a similar manner, Va, Vb, Vc, and Vd stand for the different unit voltages. Since the individual units are coupled in series, the net output voltage, which is represented by the following equation, is the addition of the individual units Fig 3 shows that.

$$V_o=V_a+V_b+V_c+V_d$$

The magnitudes of the voltage input for proposed 63 level inverters are suggested as,

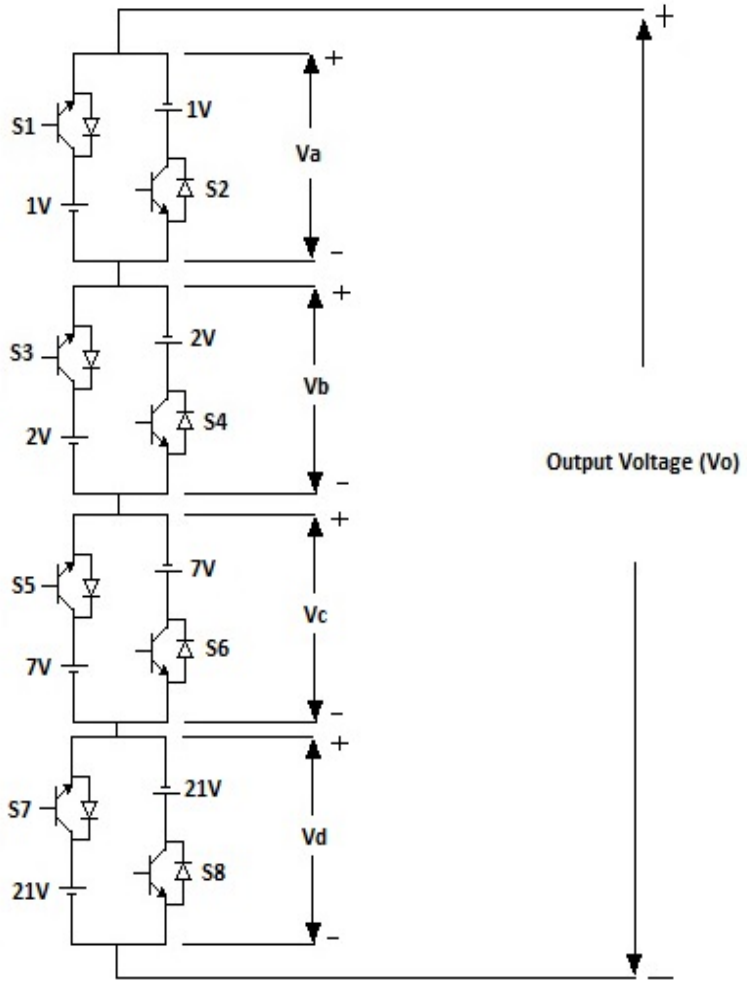

Fig 3: Proposed 63 level asymmetrical inverter

$V_1=1V_{dc}$
$V_2=2\ V_{dc}$
$V_3=7\ V_{dc}$
$V_4=21V_{dc}$

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Tab 1: Switching states of the proposed 63 level inverter.

Vo	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
31	1	0	1	0	1	0	1	0
30	0	0	1	0	1	0	1	0
29	1	0	0	0	1	0	1	0
28	0	0	0	0	1	0	1	0
27	0	1	0	0	1	0	1	0
26	0	0	0	1	1	0	1	0
25	0	1	0	1	1	0	1	0
24	1	0	1	0	0	0	1	0
23	0	0	1	0	0	0	1	0
--	--	--	--	--	--	--	--	--
--	--	--	--	--	--	--	--	--
--	--	--	--	--	--	--	--	--
7	0	0	0	0	1	0	0	0
6	0	1	0	0	1	0	0	0
5	0	0	0	1	1	0	0	0
4	0	1	0	1	1	0	0	0
3	1	0	1	0	0	0	0	0
2	0	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
-1	0	1	0	0	0	0	0	0
-2	0	0	0	1	0	0	0	0
-3	0	1	0	1	0	0	0	0
-4	1	0	1	0	0	1	0	0
-5	0	0	1	0	0	1	0	0
-6	1	0	0	0	0	1	0	0
-7	0	0	0	0	0	1	0	0
--	--	--	--	--	--	--	--	--
--	--	--	--	--	--	--	--	--
--	--	--	--	--	--	--	--	--
-23	0	0	0	1	0	0	0	1
-24	0	1	0	1	0	0	0	1
-25	1	0	1	0	0	1	0	1
-26	0	0	1	0	0	1	0	1
-27	1	0	0	0	0	1	0	1
-28	0	0	0	0	0	1	0	1
-29	0	1	0	0	0	1	0	1
-30	0	0	0	1	0	1	0	1
-31	0	1	0	1	0	1	0	1

Tab 1: shows that the eight power switches and eight voltage sources are needed in total for each 63-level module in the proposed inverter topology. The sequence is followed in controlling the voltage of each individual unit by properly switching them.

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With a step value of 1V, the suggested multilayer inverter may provide a voltage of 31V from peak to peak. Individual units have voltage outputs that range from the positive peak of the input voltage to the negative peak. The voltage levels of Va, Vb, Vc, and Vd are adjusted from positive to negative peak in accordance with the input voltage pattern. Switches S1 and S3 turn on in order to produce a voltage of 3 volts.

In a similar manner, the switches S2 and S4 enter the ON state to produce a voltage of -3V. Individual switches are operated to generate the required output steps. As per the proposed topology, the typical structure of the 125 level inverter is shown fig 4 . Its voltage magnitudes are suggested as,

$V_1=1V_{dc}$
$V_2=2\ V_{dc}$
$V_3=7\ V_{dc}$
$V_4=21V_{dc}$
$V_5=31V_{dc}$

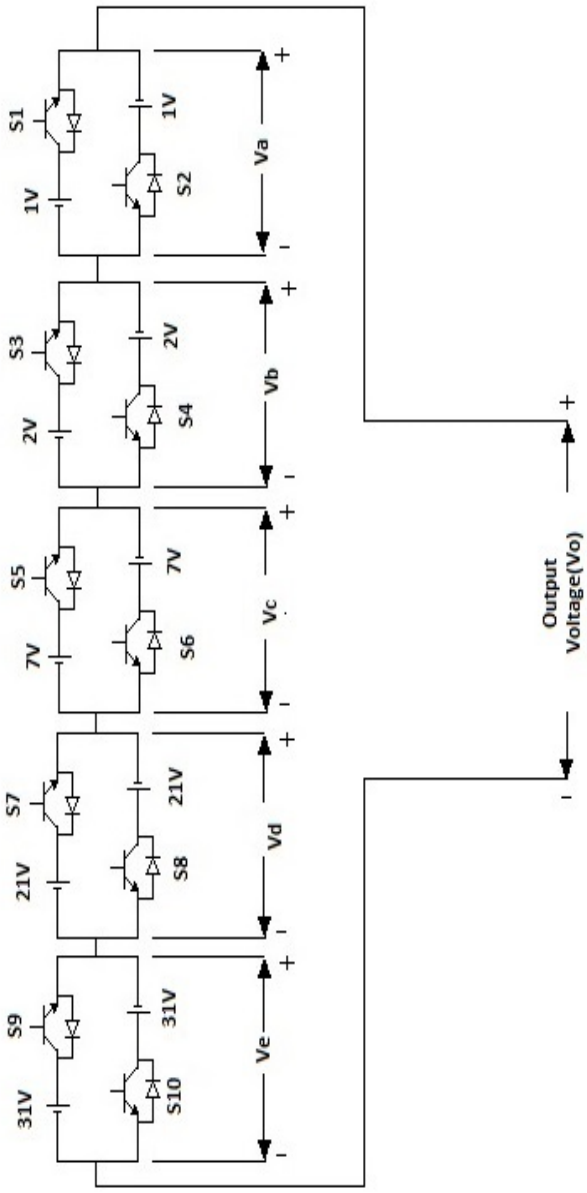

Fig 4: Structure of 123 level asymmetrical inverter

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III. SIMULATION AND RESULT

This chapter describes the Simulink modelling of the proposed multilevel inverter. Here, the MATLAB software platform is employed for simulation. The power switches must be turned on and off in accordance with the switching sequence in order to function properly. The switching table's sequence should be followed when creating the pulses that are applied to the power switches. Several modulation approaches have been employed to produce the pulses. Pulse width modulation is used to generate the switching signals. The two switches in each individual unit are activated in tandem. Displays the switching pulses that were produced. In the suggested topology, these pulses have been used as a gate input for the power switches fig 5 shows that,

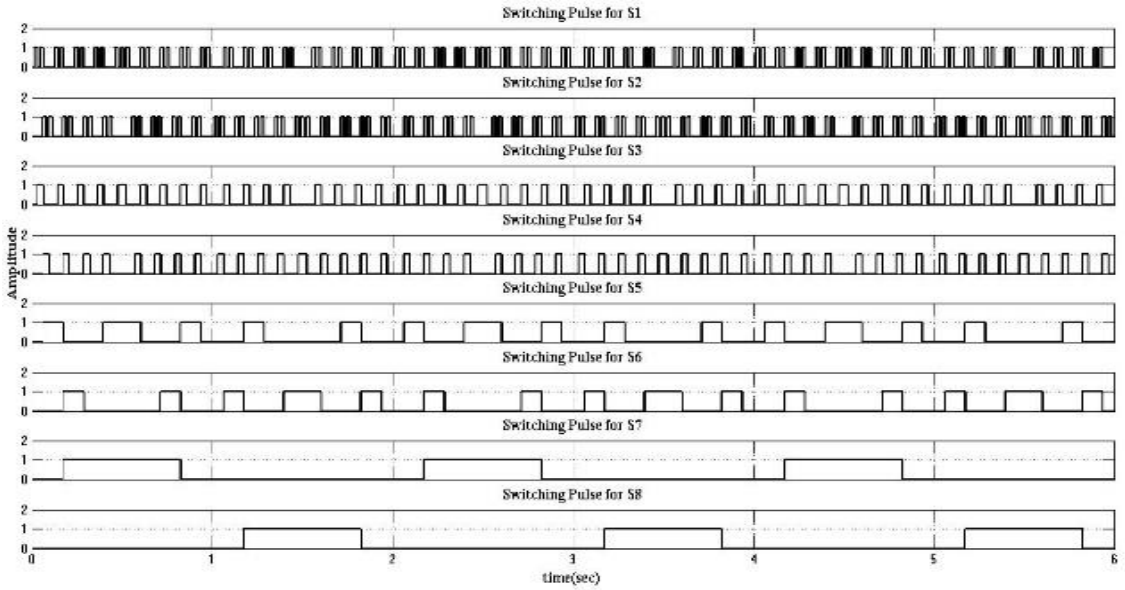

Fig 5: Switching pulses of proposed multilevel inverter

Switching pulses of multilevel inverter depicts the simulation model of the suggested multilayer inverter. As the voltage inputs are obtained in accordance with the suggested topology. The anti-parallel units' components work at a high switching frequency.

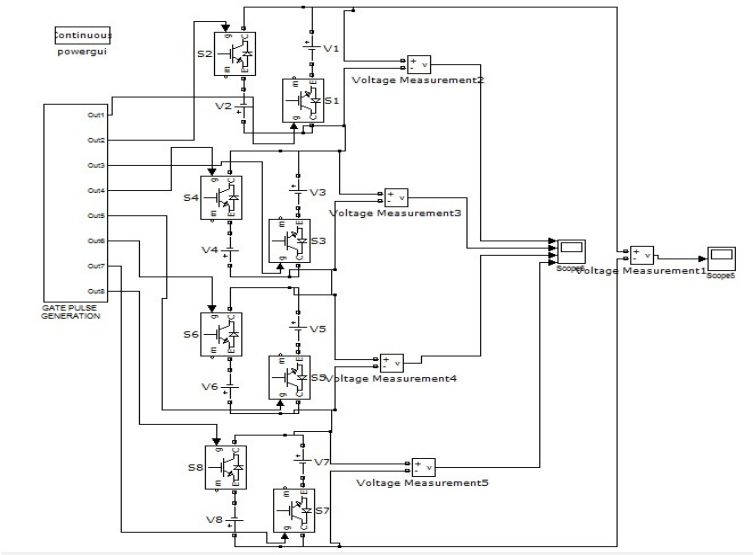

Fig 6: Simulation diagram of proposed multilevel inverter

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In these situations, IGBT switches are the ideal option. Fig 6: Voltage outputs of the different units. This output makes it evident that each unit's voltage output varies in three distinct states, which are explained by how the unit operates. When compared to conventional switches, the Va unit's switches are operated at a high frequency. Given that its voltage is considered the fundamental step voltage.

In comparison to the base unit, the subsequent units have lower switching frequencies. The voltage levels in each unit vary according to the switching frequencies. As a result, the voltages are adjusted in accordance with the power switches' switching speeds. Proposed module's output voltage. The net output voltage of the suggested module is calculated by adding these individual unit output voltages. Considering that they are all related in a series. Fig 7; voltage is varied from 0 to 31V with a step value of 1V, as per the notion that is given. The theoretical statement is followed in order to obtain the step. We don't talk about the harmonic analysis here. Fig 8; the harmonic content in the output voltage is reduced if the number of levels is increased.

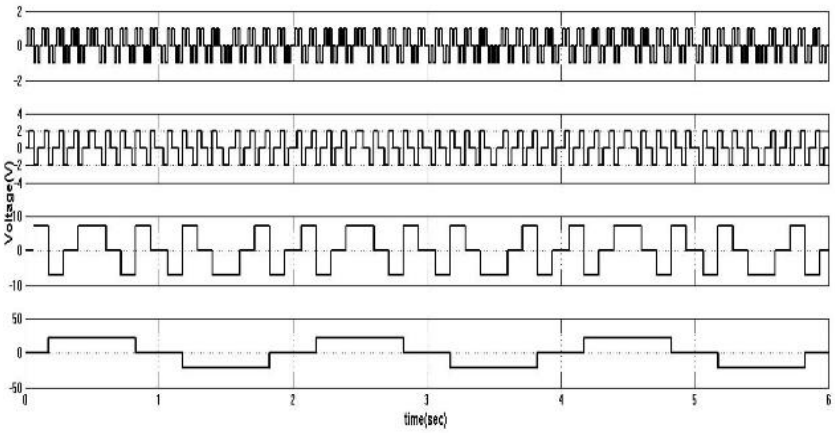

Fig 7: Individual units output voltage

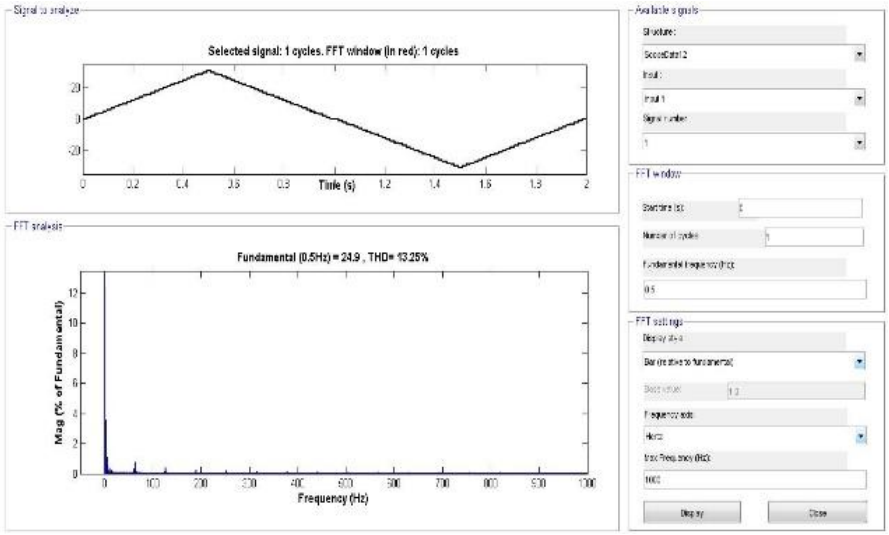

Fig 8: Simulated output voltage of 63 level inverter

IV. COMPARISON WITH EXISTING TOPOLOGY

The comparative study of the suggested multilevel inverter with current topologies is covered. The suggested module is contrasted with the electrical sources and power switches utilised in the current systems. In the architecture outlined in there are 49 level inverters that make use of 15 switches and 4 sources. The 125-level model, which makes use of eight switches and six sources. However, the suggested system's 123 level structure only needs 10 switches and 10 sources. The module presented in has six sources and 19 switches, with switches that are twice as fast than the suggested converter.

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Even with its 31-level structure, the architecture developed in uses a considerably higher number of switches. However, very high switches will be employed. The suggested module employs the fewest switches of all the compared topologies. Fig 9; as a result, the suggested system's structure will be rather straightforward. One of the key elements of the multilayer inverter design is this. Simultaneously, the suggested model makes extensive use of sources. It could also be decreased by employing other voltage techniques.

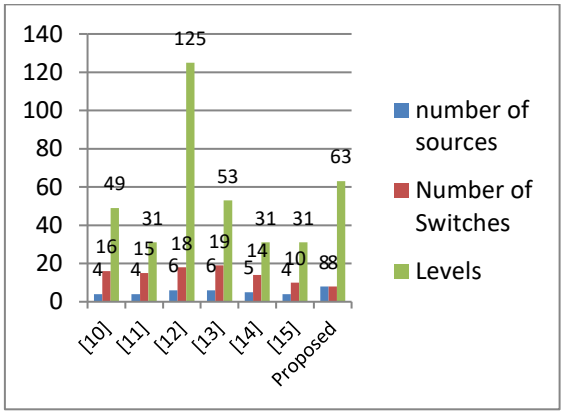

Fig 9; Comparison chart with the existing systems

V. CONCLUSION

A new anti-parallel voltage source cascaded multilayer inverter design is put forth. The simulated results validate the operation of the proposed multilevel inverter topology, which is intended for 63 level modules. The output of the suggested system is obtained in a clear manner as stated in the theoretical statement. Even with its large number of output levels, the suggested design employs a minimal number of power switches. The system's efficiency is increased by using minimum power switches, which lower the system's switching loss. The comparative graphic provides a clear explanation of the benefits of the suggested strategy.

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