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INNOVATIVE INTEGRATION OF LOW POWER, LOW NOISE AMPLIFIER (LNA)& DACFOR HIGH-PERFORMANCE CLOSED LOOP DEEP BRAIN NEURO-STIMULATOR (CDBS)USING CADENCE VIRTUOSO

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Abstract: The development of a low power, Low Noise Amplifier (LNA) and Digital to Analog converter (DAC) for integration into a Closed-loop Deep Brain Neuro-Simulator(CDBS) represents a critical step in advancing the field of neural interface technology. This report outlines the systematic design and implementation process of these vital analog and mixed-signal components using Cadence Virtuoso. The design encompasses circuit architecture selection, schematic design, noise analysis, low power optimization, layout design, simulation, verification, and post-layout considerations.

The report emphasizes the significance of achieving low power consumption and minimal noise while meeting strict performance requirements. The final LNA and DAC designs are subjected to comprehensive testing and integrated into the CDBS, ensuring their seamless operation within the closed-loop neuro simulation system. The result not only showcases the capabilities of analog and mixed-signal design but also highlights the essential role these components play in enabling precise, real-time neural interfacing and control in neuroscience research and therapeutic applications.

Keywords: Low Power, Neuro-stimulation, Closed-loop, Analog and mixed-signal design.

I. INTRODUCTION

All signals in natural operations are physical in origin. Biomedical signals have a low frequency and mill volt position noise. Detectors are used to transfer these signals into electrical signals. The detector device is demanded to descry biomedical signals produced by the body of the mortal, similar as electromyography (EMG), electroencephalography (EEG) and electrocardiography (ECG). Electric signals from the mortal body must be converted to digital signals after they've been detected.

Signal processing takes place in the digital realm. In all biomedical operations, an analogue to digital motor (ADC) is necessary for this conversion. DACs (Digital to Analog Transformers) are used in a wide range of operations, involving biomedical diagnostics, robotics and communication systems and so on.

When real- world signals are available, DACs are frequently used in utmost digital systems. Analog- to digital transformers (ADCs) convert real- time input swells which include pressure signal, analog signals similar as speech, sound swells, temperature data and film land into digital form.

These signal swells are converted back to analogue signal surge using Digital to analog motor after processing. Scientists have suggested for times that electroencephalographic (EEG) exertion may serve as a communication route between the brain and the computer

Since also, the desire for fresh functionality and conciseness from technology's electronics has increased. Given the significance of leading with bitsy natural signals, an amplifier must be designed which allows these signal factors compatible without fit like as Analog- to- Digital transformers for posterior computer processing.

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Picky modification of the raw signal, rejection of superimposed noisy disturbances and snooping signal surge, and protection from detriment attained by advanced frequency currents and voltage sore all needed for the amplifiers.

Figure1.1 depicts the DBS idea, in which abio- amplifier (called as a Low- Noise- Amplifier (LNA)) and its associated control along with processing of the signal and its interface electronics admit neural impulses and give stimulation at the same time.

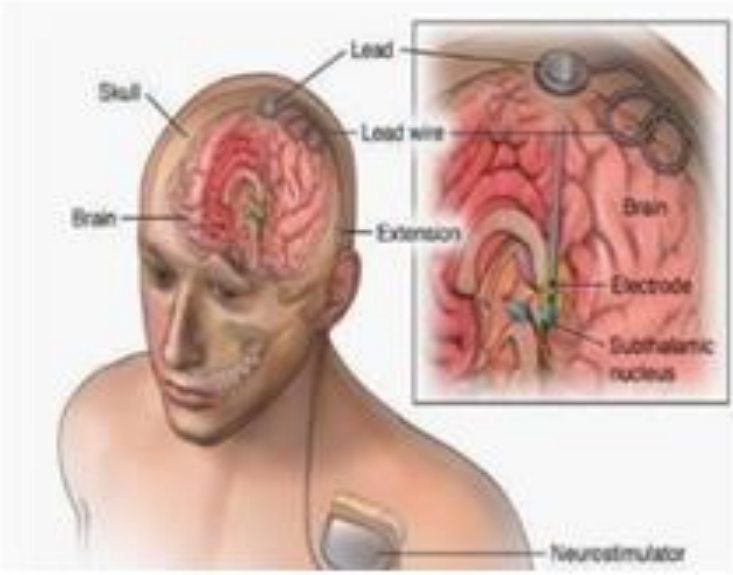

Figure1: Deep brain Stimulation Concept.

The effectiveness of the CDBS hinges significantly on the performance of its low-power, Low-Noise Amplifier (LNA) and Digital-to-Analog Converter (DAC), both engineered with meticulous attention to detail and precision. The LNA serves the critical role of amplifying faint neural signals captured by the DBS lead, necessitating a topology that strikes a delicate balance between maximizing gain and minimizing noise.

Often, the common-gate topology emerges as the preferred choice for its commendable attributes of high gain and low noise Figure. Meanwhile, the DAC undertakes the task of converting digital stimulation pulses into analog signals, demanding high resolution and minimal power consumption. Here, the R-2R DAC topology emerges as a favored option, renowned for its ability to deliver on these performance metrics.

II. METHODOLOGY

The integration of Low Power, Low Noise Amplifier (LNA) & DAC within a Closed Loop Deep Brain Neuro-Stimulator (CDBS) using Cadence Virtuoso parallels the streamlined efficiency of the Standard Serial Peripheral Interface (SPI). Much like SPI conserves resources with its four lines, the LNA and DAC optimize functionality while minimizing power consumption and noise.

Operating in harmony, the LNA acts as the master, amplifying neural signals, while the DAC, akin to the slave, converts digital control signals into precise analog outputs for neural stimulation. Synchronized by clock signals, this communication ensures accurate neural interfacing, reflecting the elegant simplicity of SPI's serial data transmission process.

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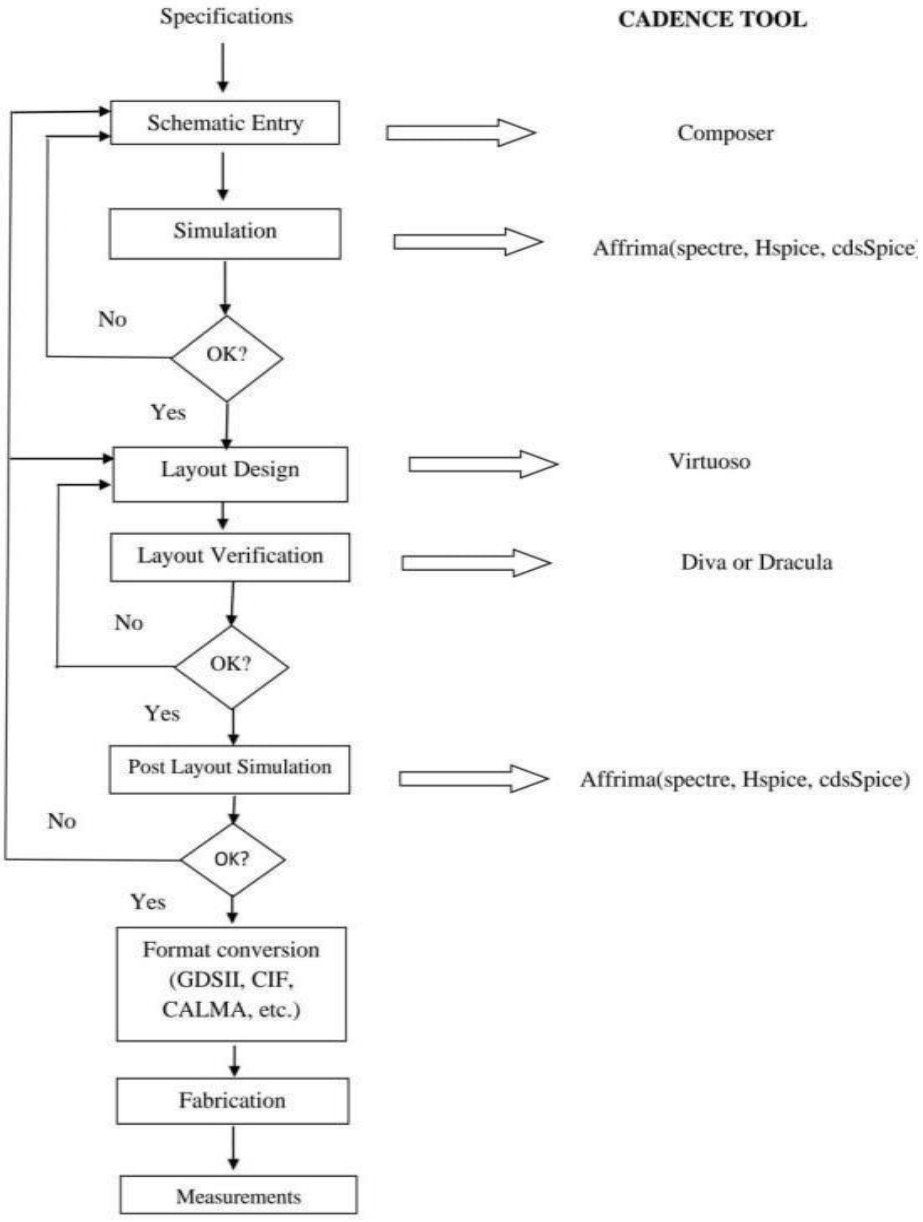

Figure2: Methodology of analog design flow of components

Through meticulous design and implementation, these components exemplify the intersection of analog design and neuroscience, paving the way for advanced therapeutic applications in deep brain stimulation. The cohesive integration of these components within the CDBS underscores their vital role in enabling precise, real-time neural interfacing and control, essential for advancing both research and the rapeutic intervention sin neuroscience.

Step 1: The circuit design of schematic is made by composer of cadence schematic editor.
Step 2: The design schematic must be proved by using save and check option.
Step 3: If existence of an error, design must be edited and saved for continuing the step.
Step4: This step has the symbol creation. Creation of
Symbolism very cardinal step; on account of once symbol created the named, design can be used in schematics of different design, wherever it is needed. At last, design will be saved.
Step5: Here must and should repeat the step 3
Step 6: Environment test setup will be created. This gives for design inputs, supply of power and connections of ground. The design will be saved.
Step7: Again, thestep3mustberepeated.

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Step 8: Analog of design environment will be created and CADENCE SPECTRE using simulation of circuit. This step involves such as dc analysis, ac analysis and transient analysis etc. And it gives result of simulation in the format of waveform.
Step 9: From the output waveform we can verify and calculate different parameters such as delay and power. In this window first we go to tools option, in that click on calculator option. TOOLs CALCULATOR option used.
Step10 : Comparison for obtaining the result
Step 11: After the specifications of circuit design and simulations carried layout and layout of post designs.
Step 12: Design verification and processing in the direction of chip design fabrication.

a. Procedure

To utilize Cadence tools for writing Verilog code and verifying its coverage, follow these steps. First, establish the project environment within Cadence, ensuring proper tool installation and license activation. Then, create or open a project to begin design entry. Utilize the Verilog HDL (Hardware Description Language) to code your design within Cadence's environment.

Once the Verilog code is written, simulate the design using tools like NC-Verilog to assess its functionality and performance. During simulation, track code coverage metrics to ensure comprehensive testing of the design.

Analyze the coverage results to identify untested portions of the Verilog code, allowing for refinement and optimization of the design as needed. Through this process, designers can iteratively develop Verilog designs within Cadence, ensuring thorough testing and verification of their functionality.

b. Specifications

The specifications for the Low Noise Amplifier (LNA) and the R-2R Digital-to-Analog Converter (DAC) are crucial for ensuring optimal performance in various systems. The LNA must provide a minimum gain of 20 dB while maintaining a noise Figure below 3 dB and consuming no more than 1 watt of power. This ensures effective signal amplification with minimal added noise and power consumption.

Meanwhile, the DAC needs to have a resolution of at least 12 bits, keep the Total Harmonic Distortion (THD) below 1%, and also consume a maximum of 1 watt of power. These specifications are vital for accurate conversion of digital signals to analog with high fidelity and efficiency. Meeting these requirements ensures the reliable operation of systems such as communication systems, audio processing equipment, and instrumentation setups.

Table1: Specifications Table.

Component	Parameter	Type	Unit
Low Noise Amplifier	Gain	At least 20	dB
	Noise Figure	< 3	dB
	Power consumption	< 1	mW
R-2R Digital-Analog Convertor	Resolution	At least 12	Bits
	Total Harmonic Distortion (THD)	< 1	%
	Power consumption	< 1	mW

III. RESULTS AND DISCUSSION

In Closed Loop Deep Brain Neuro-Stimulators (CDBS), Low Noise Amplifiers (LNAs) are essential for accurately amplifying weak neural signals while minimizing noise enabling precise neural activity detection and therapy adjustments. These LNAs contribute to improved therapeutic outcomes by facilitating real-time neural feedback processing, ultimately enhancing the precision and efficacy of CDBS treatments for neurological disorders. Their role in minimizing noise ensures reliable signal amplification, crucial for maintaining the integrity of neural stimulation protocols.

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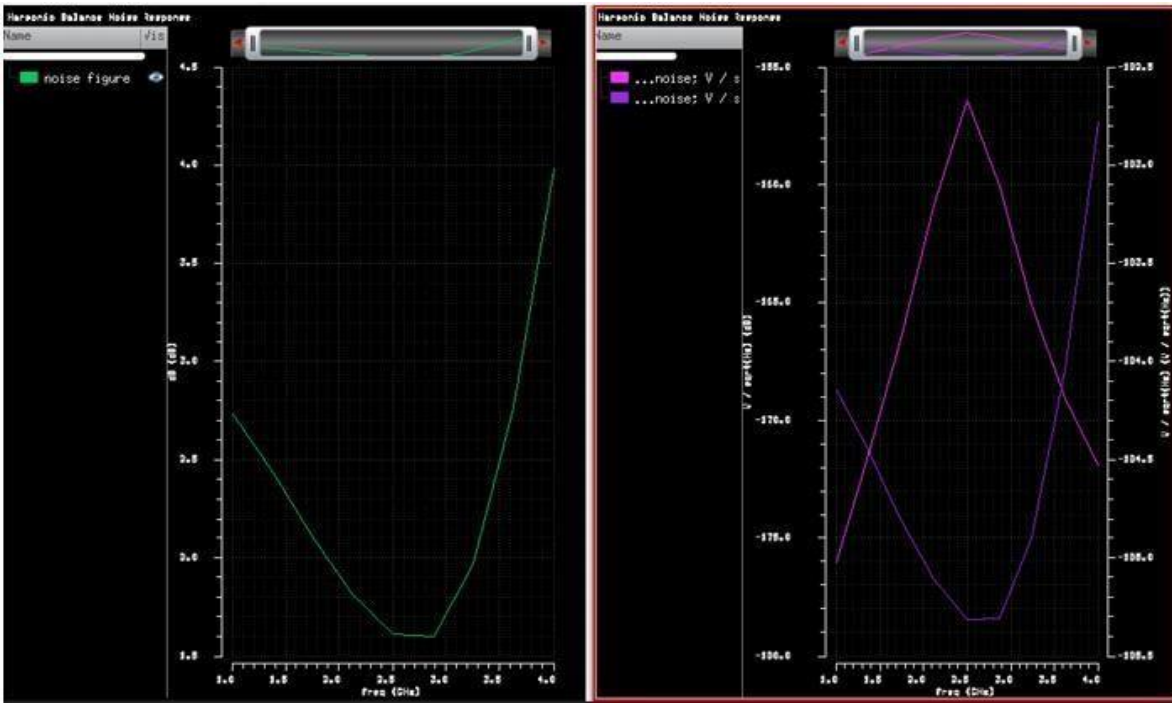

Figure3: Waveform of NF(Noise Figure),Input and Output Noise.

In Closed Loop Deep Brain Neuro-Stimulators (CDBS), R-2R Digital-to-Analog Converters (DACs) convert digital control signals into precise analog voltages, enabling accurate modulation of neural stimulation parameters. By providing fine-grained control over stimulation waveforms, R-2RDACsplayapivotalrolein tailoring therapy delivery to individual patient needs in CDBS applications. These DAC sensure high-resolution adjustments of stimulation levels, contributing to the customization and optimization of therapy regimens for neurological disorder management within Closed Loop Deep Brain Neuro-Stimulators (CDBS). Their precise conversion capabilities facilitate real-time adaptation to neural activity, enhancing the responsiveness and effectiveness of CDBS treatments.

Figure 4: R-2R DAC waveform.

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The proposed design stands out for its remarkable achievement in reducing leakage power across various technology nodes, offering a significant improvement over conventional design. Specifically, in the case of Low Noise Amplifiers (LNAs), the proposed design implemented at 90nm technology demonstrates a leakage power of 2.124 µW. Comparatively, the conventionaldesignsat45nm and180nm exhibit higher leakagepowersof1.308 µWand2.48 µW, respectively.

Table2: Comparison table of LNA and DACin different technologies.

Design	Technology (nm)	Analog circuits					
		LNA			DAC		
		Area (mm^2)	Average power (uW)	Leakage power (uW)	Area (mm^2)	Average power (uW)	Leakage power (uW)
Conventional Design-1	45	-	283.8	1.308	-	296.5	0.588
Conventional Design-2	180	-	710.6	2.48	-	675.81	1.689
Proposed Design	90	0.039	345.7	2.124	0.054	305.2	1.153

This showcases the superior efficiency and power management capabilities of the proposed LNA design, especially notable in the 90nm technology node. Similarly, for the R-2R Digital-to-Analog Converters (DACs), the proposed design at 90nmtechnology impressivelyachievesaleakagepowerof1.153µW.

In contrast, the conventional designs at 45nm and 180nm register higher leakage powers of 0.588 µW and 1.689 µW, respectively. This highlights the consistent trend of the proposed design in minimizing leakage power across different technology nodes.

Table3: Comparison of LNA and DA Cinanalog and digital circuits using 90nm technology.

Proposed Design (90nm)				
Specifications	Analog circuit		Digital circuit	
	LNA	DAC	LNA	DAC
Area	$0.039mm^2$	$0.054mm^2$	$194.5233um^2$	$175.5994um^2$
Average power	345.7uW	305.2uW	0.08494Nw	0.05650nW
Leakage power	2.124uW	1.153uW	0.01511nW	0.00717nw

The table compares the area and average power consumption of low noise amplifiers (LNAs) and digital-to-analog converters (DACs) designed using a 90nm process.

- Area: The LNA has a smaller area ($0.039mm^2$)than the DAC ($0.054mm^2$).
- Average Power Consumption: The LNA has higher average power consumption (345.7µW)than the DAC (305.2 µW).

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IV. CONCLUSION

To enhance the proposed design's efficiency, we should conduct a comprehensive power analysis, encompassing total power consumption with a focus on dynamic power components. Additionally, comparing performance metrics like gain and signal-to-noise ratio against conventional designs will reveal crucial trade- offs between power consumption and performance.

It's essential to analyze scalability across diverse process technologies, particularly in smaller feature sizes like 7nm, to anticipate performance and leakage power variations. Exploring application-specific optimization can further tailor the design for lower power consumption while maintaining adequate performance standards. Finally, initiating fabrication and real-world testing on silicon will provide empirical data to validate theoretical benefits observed from simulations. However, within the specific scenario of the 90nm process, while the LNA design achieves a smaller footprint, it concurrently exhibits higher average power consumption compared to the DAC

V. FUTURE WORK

To enhance the proposed design's efficiency, we should conduct a comprehensive power analysis, encompassing total power consumption. Additionally, comparing performance metrics like gain and signal-to- noise ratio against conventional designs will reveal crucial trade-offs between power consumption and performance. It's essential to analyze scalability across diverse process technologies, particularly in smaller feature sizes like 7nm, to anticipate performance and leakage power variations. Application-specific optimization can further the design for lower power consumption while maintaining adequate performance standards. However, within the specific scenario of the 90nm process, while the LNA design achieves smaller footprint, it concurrently exhibits higher average power consumption compared to the DAC.

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