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Verification of AMBA-APB Protocol using UVM

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Abstract: Through the use of the Universal Verification Methodology (UVM), the project ”Verification of AMBA-APB Protocol using UVM” seeks to guarantee the stability and dependability of the Advanced Microcontroller Bus Architecture - Advanced Peripheral Bus (AMBA-APB) protocol. The goal of this project is to create a thorough verification environment that makes use of UVM to thoroughly verify that complex digital systems that adhere to the AMBA-APB protocol are compliant. The project aims to improve verification efficiency, encourage reusability, and enable comprehensive protocol compliance testing through the utilization of UVM. As a result of this research, more dependable and interoperable digital systems will be developed, which is important for the development and application of contemporary electronic gadgets.

Keywords: AMBA, VLSI, VIP, SoC, APB, UVM, Design Verification.

I. INTRODUCTION

One of the primary methods for producing integrated circuits (ICs) is very large-scale integration, which involves merging millions of transistors into a single chip. When microcircuit chips were widely used in the 1970s, VLSI technology was developed. It allows for the development of massive semiconductor and telecommunication technologies. Prior to the development of VLSI (very large-scale integration) technology, the majority of integrated circuits (ICs) could only carry out a certain number of tasks.

A CPU, ROM, RAM, and additional logic circuits make up the electronic circuit. These are all combined into a single chip using VLSI technology. An integrated circuit, or SoC, combines every component onto a single chip. On a single chip substrate, it combines analog, digital, mixed signal, and additional radio frequency functions. Now, the electronics industry frequently uses SoCs because of their reduced power consumption. System on-Chip (SoCs) applications are also heavily utilized by embedded system applications.

System on chip (SoC) refers to the ability to coordinate millions of semiconductors on a single chip thanks to the enormous advancements in VLSI innovation. For SoC applications, the AMBA APB Protocol is completely designed and verified. APB and other low-performance execution transports are interfaced with a multitude of elite transport components, such as AHB, ASB, and AXI, among others, that make up AMBA Bus. In order to communicate with slaves such as UART, TIMER, Keypad, and INTERRUPT CONTROLLER, among others, APB uses low peripheral bandwidth.

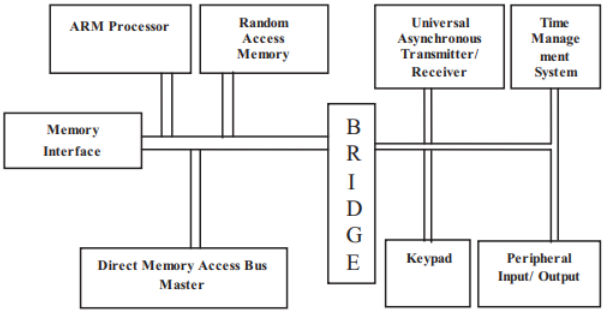

Figure 1: AMBA Bus Architecture diagram.

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Table 1
Research Summary and Methodological Analysis

Author(s)	Paper Title	Publication Year	Methodology Result
Dhanush M, Dr. Sunil T D, Kenton Lee, and Dr. M Z Kurian	"Apb Protocol Coverage-Based Verification using Uvm"	2022	Successful verification using UVM, 91.47% coverage
Anushka Dwivedi and Dr. Anand Jatti	"Design and Implementation of AMBA APB Protocol using System Verilog"	2022	Successful verification using System Verilog
Dhanush M, Dr. Sunil T.D, and Dr. M. Z. Kurian	"An Overview on Advance Peripheral Bus Design using System Verilog"	2022	Verification using Verilog, use of assertions
Shaik Sulthana, Aravinth G, Harisuvedha G, and Ananda Gopal Mukherjee T	Coverage-Based Verification of APB Protocol using UVM	2021	Comprehensive coverage and error-free verification
Prameeth.H, Aayushii Goswami, Prajwal.M, Vikas.N.G, and Dr. Rachana.S. Akki	"System Verilog/UVM Verification of AMBA APB Protocol"	2021	Successful UVM-based verification
J. Mukunthan	"Design and Implementation of AMBA APB Protocol"	2021	Verification using QUESTASIM, comprehensive testing
Vaishnavi R.K, Bindu.S, and Sheik Chandbasha	"Design and Verification of APB Protocol using System Verilog and UVM"	2019	Simulation confirms functional correctness
Shankar, Dipti Girdhar, and Neeraj Kr. Shukla	"Design and Verification of AMBA APB Protocol"	2014	Simulation results show functional correctness
Kommirisetti Bheema Raju and Bala Krishna Konda	"Design and Verification of AMBA APB Protocol"	2017	Implementation using VHDL, FPGA configuration
Padmaprabha Jain and Satheesh Rao	"Design and Verification of AMBA-APB Protocol"	2021	Description of AMBA-APB protocol
K. Swetha Reddy, P. Soujanya, and D. Kanthi Sudha	"Asic Design and Verification of Amba Apb Protocol using Uvm"	2020	ASIC design, UVM-based verification

II. METHODOLOGY

Understanding the structure and function of the AMBA APB Architecture's many components is crucial for carrying out design verification. As seen in Figure 2, we quickly go over the different APB signals, how AMBA APB Master and Slave work, the three APB operating modes, and read and write transactions in this section. We implement a suitable verification technique after comprehending the many UVM features and after having a solid understanding of the numerous intricacies and essential design components of the AMBA APB protocol. Finally, we perform the regression to get and explain the findings.

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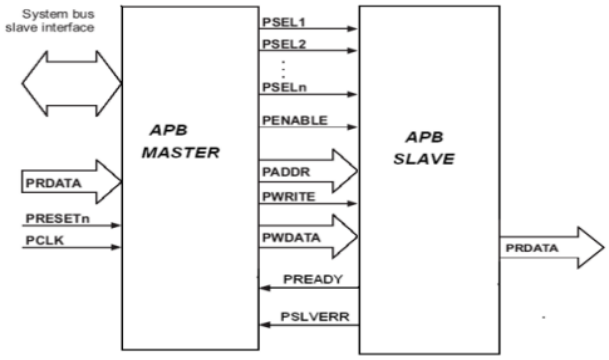

Figure 2: Interfacing of APB Master & Slave

Table 2: List of APB signals

Signal	Signal Description
PCLK	Clock. The rising edge of PCLK times all transfers on the APB.
PRESET	System bus equivalent Reset. The APB reset signal is active LOW.
PADDR	32 bit. address bus
PSEL	The slave device is selected and that a data transfer is required.
PENABLE	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	Access when HIGH.
PWDATA	32 bits. Write data .PWRITE is HIGH.
PREADY	Ready. To extend an APB transfer.
PRDATA	32 bits. Read data. PWRITE is LOW.
PSLAVERR	Slave error. This signal indicates a transfer failure,

STATES OF OPERATION FOR APB

IDLE, SETUP, and ACCESS states are the three states. The fundamental state machine that depicts how a peripheral bus operates is shown in Figure 3.

IDLE: is the initial state of the peripheral bus.

SETUP: The bus enters the SETUP state to activate the select signal, PSELx, for transmission. After one clock cycle in SETUP, it always moves to the ENABLE state on the next rising clock edge.

ENABLE: During SETUP to ENABLE transition, PENABLE activates while address, write, and select signals remain stable. After one clock cycle in ENABLE, the bus returns to IDLE if no further transfers are needed; otherwise, it proceeds directly to SETUP for the next transfer. However, during ENABLE to SETUP transition, address, write, and select signals might malfunction

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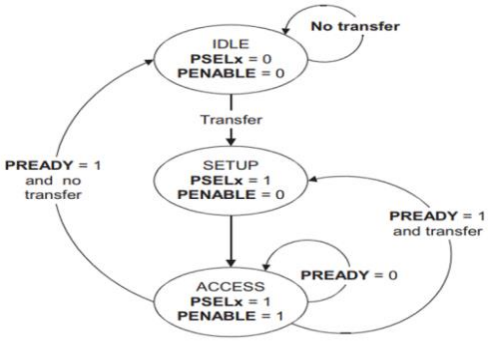

Figure 3: Operating States of APB

Process of Implementation

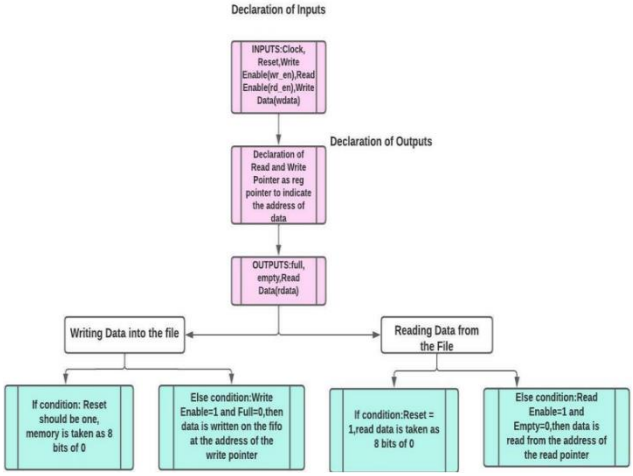

Figure 4: Flow-Chart representing read-write operation

The Advanced Peripheral Bus (APB) protocol is integrated into the AMBA (Advanced Microcontroller Bus Architecture) family of bus architectures. Testing is done on the Design Under Test (DUT), which creates a communication channel between the slave (design) and master (test bench). It is built with the reusable System on Chip (SoC) methodology, which is essential for solving modern VLSI problems. In order to connect peripherals like timers and keypads to the bus design, APB optimises power, cost, and bandwidth. The APB protocol, which includes multiple write transactions and single and multiple write transactions with and without waits, must be designed and implemented. An important step in VLSI design is verification, which seeks to identify RTL (Register Transfer Level) design flaws early on to avoid problems later on. Verification takes a lot of time therefore it usually takes up 70% of the total time.

III. CONCLUSION

In conclusion, the comprehensive literature review on the "Verification of AMBA APB Protocol using UVM" highlights the paramount importance of this research area within the domain of Very-Large-Scale Integration (VLSI) and System-on-Chip (SoC) design. The papers under scrutiny collectively emphasize the critical role of the AMBA APB protocol, serving as a vital bridge between high-bandwidth buses and low-bandwidth peripherals in modern SoC systems. This protocol's robust and accurate functionality is imperative for seamless communication within intricate VLSI architectures.

The inclusion of simulation results and coverage reports in many of the papers corroborates the functional correctness of the AMBA APB protocol. These tangible outcomes validate the successful verification efforts and comprehensive testing that researchers have conducted to confirm the protocol's reliability and accuracy.

Ultimately, the reviewed literature collectively contributes to the field of VLSI technology, serving as an invaluable resource for VLSI designers, embedded systems engineers, and individuals interested in microcontroller bus architectures. As technology continues to advance, the insights and knowledge imparted by these scholars are essential

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in meeting the ever-growing demands of VLSI and SoC design. Their work plays a pivotal role in creating more robust, efficient, and dependable integrated circuits to support the evolving landscape of modern electronics.

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