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Implementation of VDTA-Based Universal Filter in 180nm Technology

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Abstract: This paper presents a single Voltage Difference Transconductance Amplifier (VDTA) based active filter design with a supply voltage of ± 900mV. The circuit configuration uses an nMOS transistor as an active resistor.

The Cadence Virtuoso tool is used to obtain gain and phase characteristics, noise calculation, and frequency response under various temperatures. Filter response was observed by varying different values of capacitors. The proposed circuit was implemented in gpdk180nm technology with a power consumption of 910.5µW and an area is 2867.99µm^2.

Keywords: Active Resistance, Active Filters, Universal Filter, VDTA.

I. INTRODUCTION

Active filters can be frequently used as a base in analog signal processing. In contrast to RLC filters, they are more integrable and hence are much in demand for several tasks such as control and instrumentation systems, broadcasting systems, computer systems, telephone circuitry, and video signal processing [1].

Furthermore, the current literature contains various minimal configuration voltage-mode (VM) multi-input-single-output (MISO) universal filter designs employing both capacitors as input terminals for predefined connections [2- 13].

However, the complexity of their internal active building blocks and excess transistors might lead to increased silicon area during on-chip construction.

Over the last few decades, analog circuit designs have widely used conventional Operational amplifier (op-amp) blocks. However, op-amps have several drawbacks, such as a relatively low slew rate, limited bandwidth, and complex circuitry. As a result, alternative active building blocks [14] have emerged in recent years to address these issues [15-20].

VDTA voltage has two gain stages thus it provides an electronic tuning ability that meets the requirement for low power and compact CMOS implementation. There has been much research on VDTA based filter design in communication and signal processing applications [19]-[23].

Normally, filters are designed using passive components with active blocks. In this paper, a single VDTA-based band pass filter, a low pass filter, and a high pass filter are designed with three capacitors and an active resistor. An nMOS transistor is used to implement active resistance. It operates in the triode region.

The advantage of active resistance is that it occupies a smaller area and allows the filter to be tuned electronically.

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II. DESIGN IMPLEMENTATION

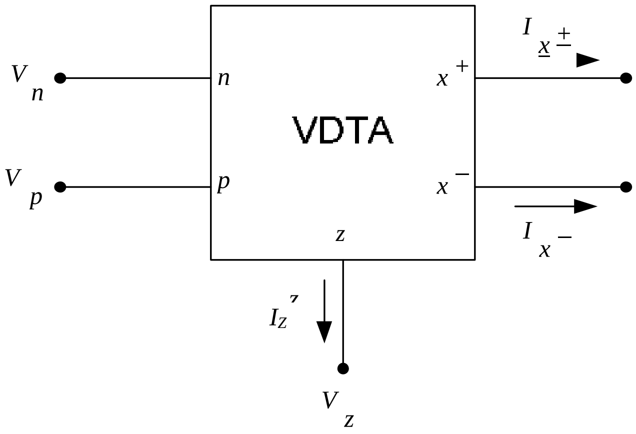

Figure 1: Symbol of VDTA active Block.

In Figure 1, the block diagram of the VDTA is displayed with Vp and Vn as input terminals, and x + and x - being the output. The CMOS implementation is illustrated in Figure 2; it has both an input and output transconductance stage. The former converts the differential input voltage (Vp -Vn) to current Iz, while the latter changes voltage Vz at terminal z to current Ix. All ports have a high impedance value, with relations between them outlined below.

$$\begin{bmatrix} Iz \\ Ix+ \\ Ix- \end{bmatrix} = \begin{bmatrix} gm1 & -gm1 & 0 \\ 0 & 0 & gm2 \\ 0 & 0 & gm2 \end{bmatrix} \begin{bmatrix} Vp \\ Vn \\ Vz \end{bmatrix}$$

Where gm1 and gm2 are the input and output transconductance (TC) gains of VDTA. The first TC gain transforms the difference in incoming voltage into the current at the Z (Intermediate) port. The second TC gain converts the voltage at the Z input to an output current gm2.

$$gm1 = \frac{g_1\, g_2}{g_1 + g_2} + \frac{g_3\, g_4}{g_3 + g_4}$$

$$gm2 = \frac{g_5\, g_6}{g_5 + g_6} + \frac{g_7\, g_8}{g_7 + g_8}$$

Where gi implies transconductance of ith MOS transistor, which is given below.

$$gi = \sqrt{I_{Bi}\mu C_{ox}\left[\frac{W}{L}\right]}$$

Where IBi implies the bias current of the ith transistor, μi implies the carrier mobility and Cox is the gate oxide capacitance per unit area. W and L are the width and length of the ith transistor.

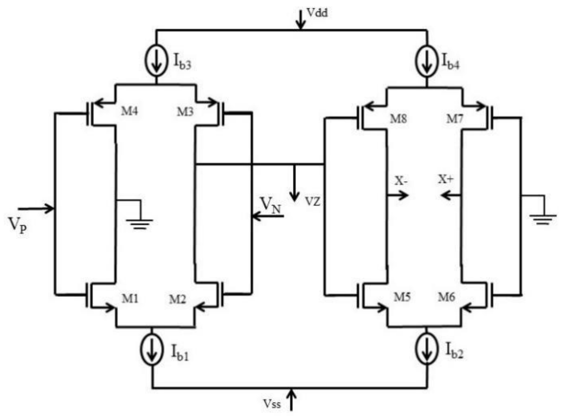

Figure 2: CMOS implementation of VDTA

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A CMOS implementation of the proposed Universal filter is shown in Figure 2. All simulations are performed using gpdk180nM CMOS technology.

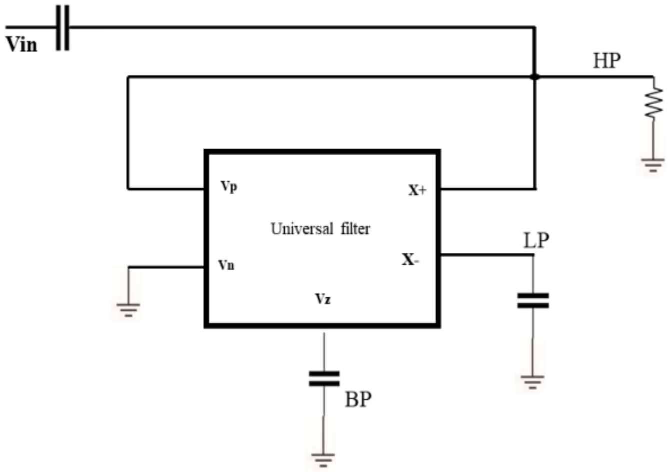

Figure 3: Voltage mode Filter design

In Figure 3, a single VDTA conveys the characteristics of High Pass, Low Pass, and Band Pass filters. The proposed configuration replaces these passive resistances with nMOS active resistance (Ron). This renders the filter programmable by varying the gate voltage of the nMOS transistor, while simultaneously occupying less area in its layout.

III. SIMULATION RESULTS

Figure 3 shows the proposed Universal Filter structure realized with CMOS transistors. The circuit is simulated in the Cadence Virtuoso tool using gpdk 180nm technology. Standard nMOS and pMOS transistors with aspect ratios of 16.64µm/360nm and 3.64µm/360nm are employed.

The supply voltage is 1.8V, with Vdd being +900mV and Vss being -900mV. Active resistance operates in the linear region with 550mV gate voltages. To get 1.57 KΩ resistance, the NMOS transistor's W/L ratio is 1.2µm/180nm. C1, C2, and C3 capacitances are all of 100nF, 1mF and 1pF respectively. VDTA element DC transfer characteristics are shown in Figure 4 and the power consumption of the Universal filter is calculated at about 910.5µW.

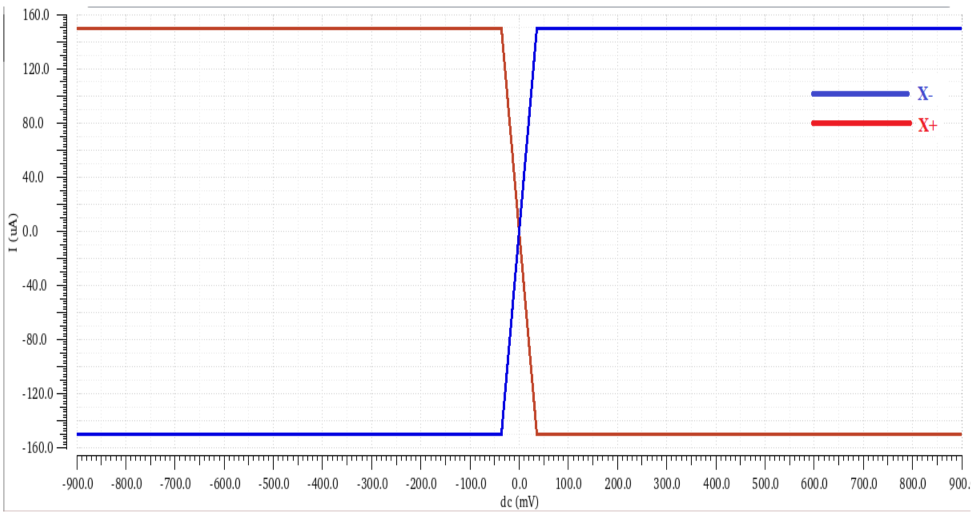

Figure 4. DC Characteristics of VDTA

The Universal filter shown in Figure 3 receives a sinusoidal signal with an amplitude of 1V peak to peak at 1MHz. The simulated gain and frequency responses of the Universal filter are shown in Figure 5.

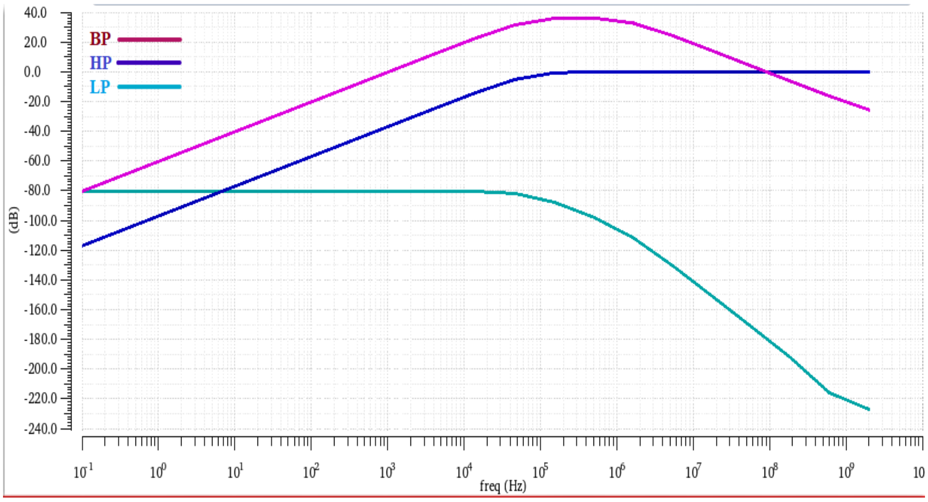

Figure 5. High pass, band pass, and low pass output of VDTA filter.

High pass (HP), Low pass (LP), and band pass (BP) filters have cutoff frequencies of 110.15KHz, 738.86KHz and1.55MHz respectively. Capacitances C1, C2, and C3 are 100n F, 1mF, and 1p F and Ron is 1.2 KΩ. The simulated gain and frequency responses of the Universal filter are shown in Figures 6,7 and 8.

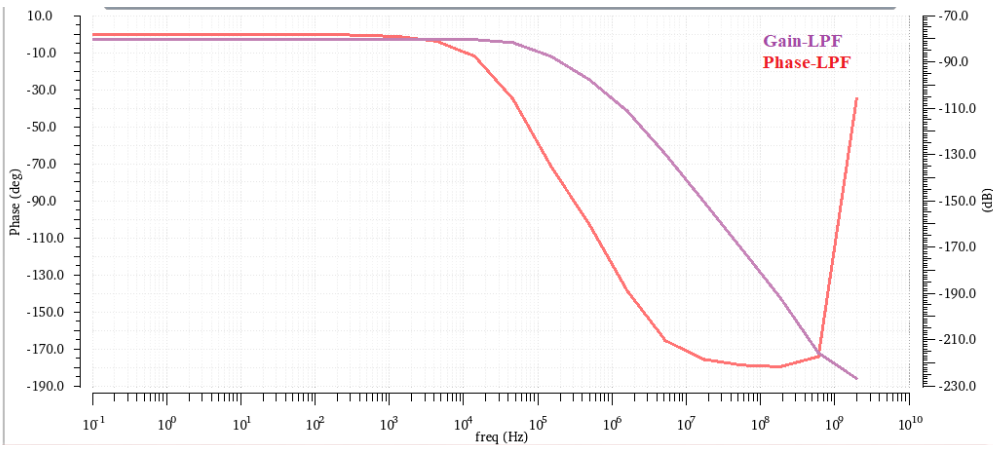

Figure 6. Gain and phase response LPF

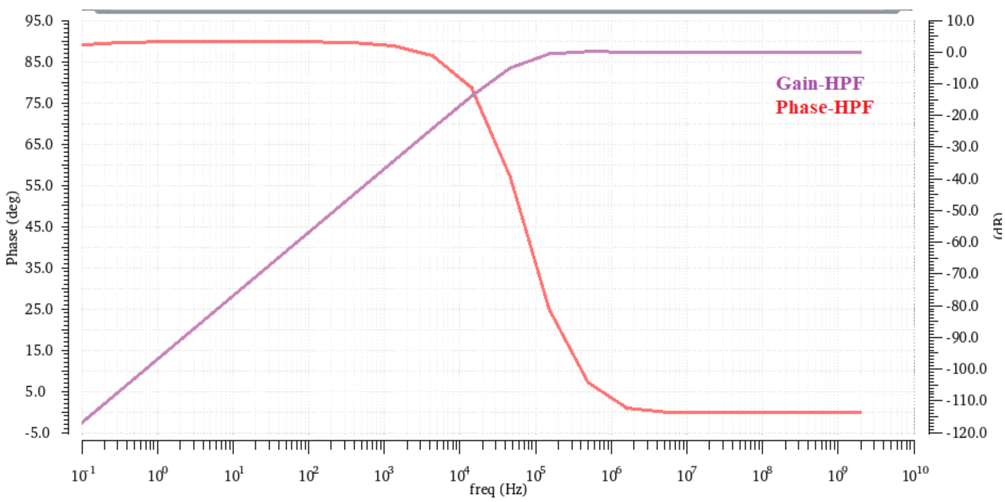

Figure 7. Gain and phase response HPF

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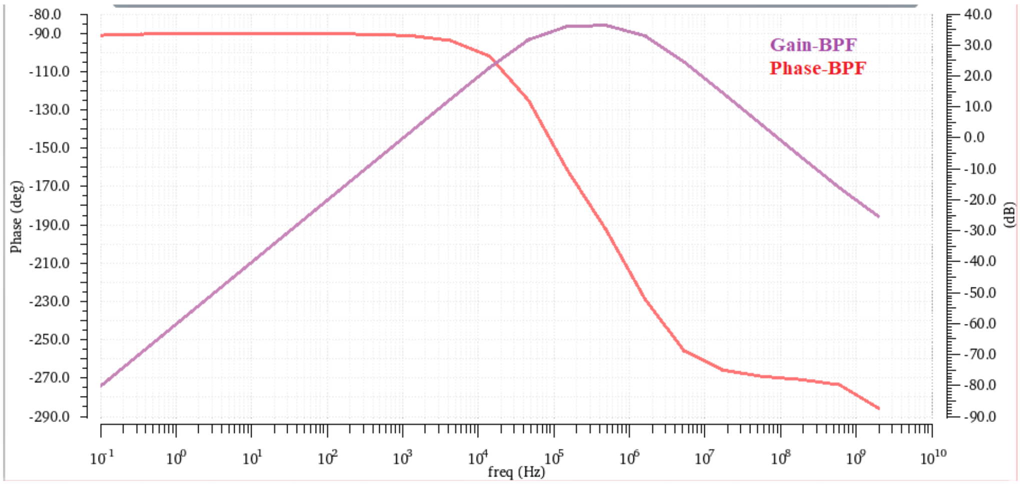

Figure 8. Gain and phase response BPF

The proposed Universal filter's temperature performance is simulated over a range of temperatures that vary from 0 C to 100 C. Figure 9,10 and 11 illustrates the change in frequency response as a function of temperature. As can be seen from the figures, both the gain and phase of the filter remain at acceptable levels at different temperatures. In addition, the output noise voltage of the proposed Universal filter is simulated. The filter circuit has an output noise voltage of 1.694nV/Hz at a frequency of 1 MHz as shown in Figure 12.

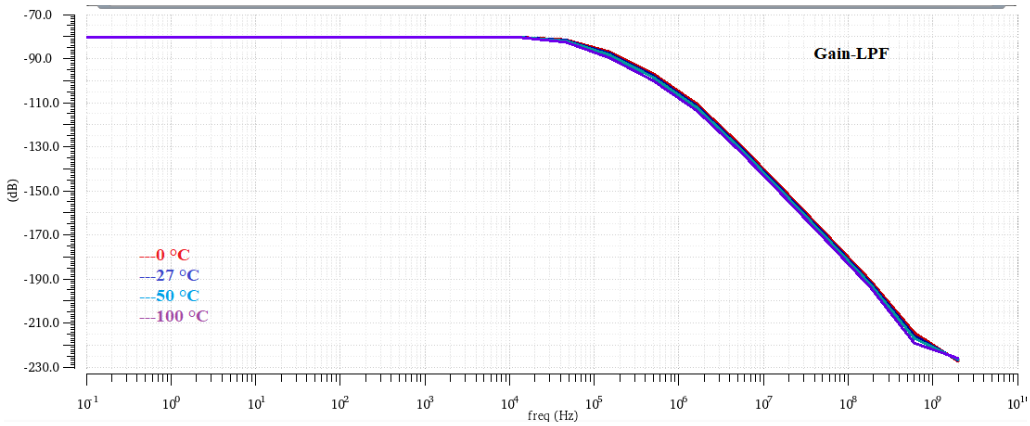

Figure 9. Frequency response of the LPF for various temperatures

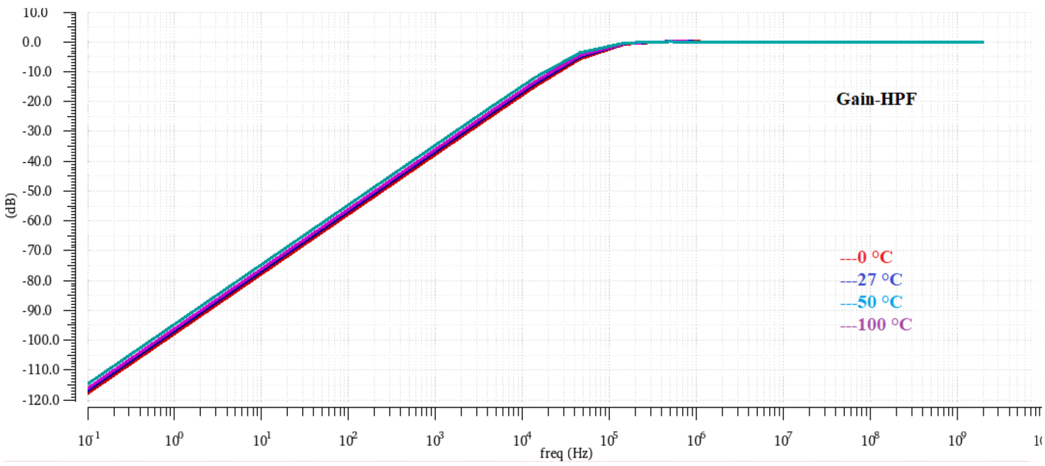

Figure 10. Frequency response of the HPF for various temperatures

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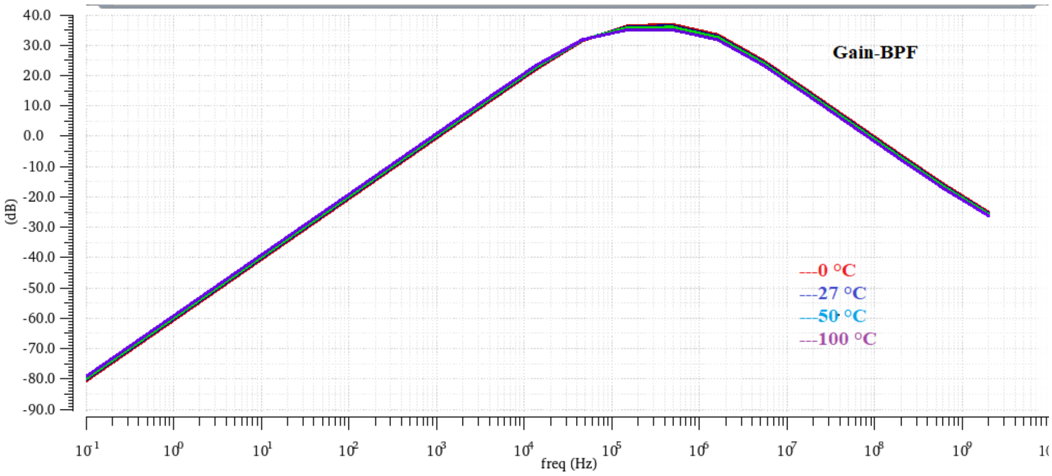

Figure 11. Frequency response of the BPF for various temperatures

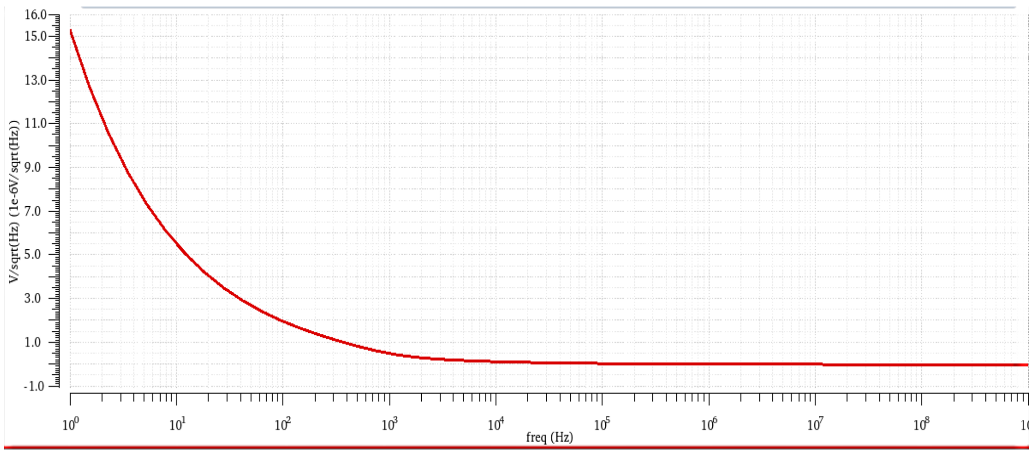

Figure 12. Output noise voltage of the universal filter

Figure 13,14 and 15 illustrates the change in frequency response as a function of different capacitors. As can be seen from the figure, both the gain and phase of the filter remain at acceptable levels at different capacitors. With different capacitor values, the cutoff frequencies of the Universal filter can be observed and shown in Table 1.

Table 1 shows the performance of the Universal filter at different capacitor values and the cutoff frequency of the Low Pass (LP), High Pass (HP), and Band Pass (BP) Filters. Figure 16 shows the layout design of the proposed VDTA and the area consumed is 2867.99 μm^2.

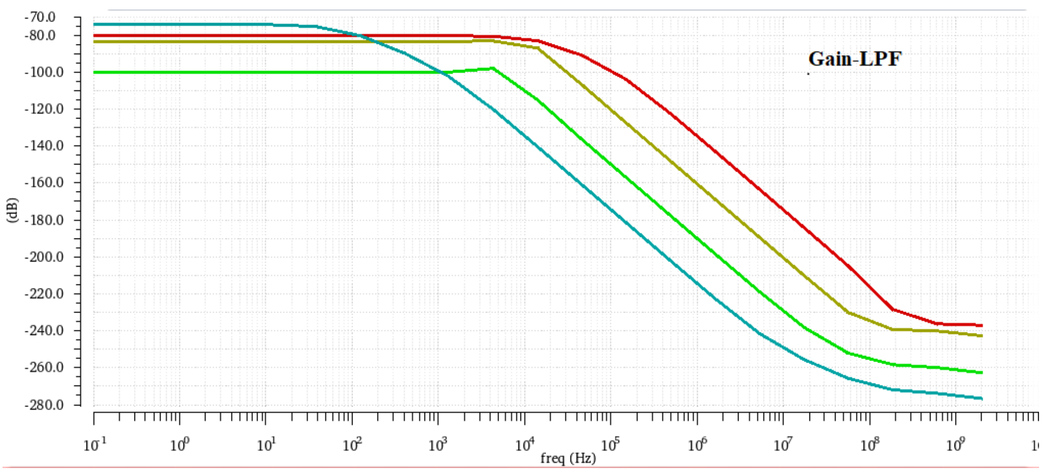

Figure 13. Frequency response of the LPF for different capacitors

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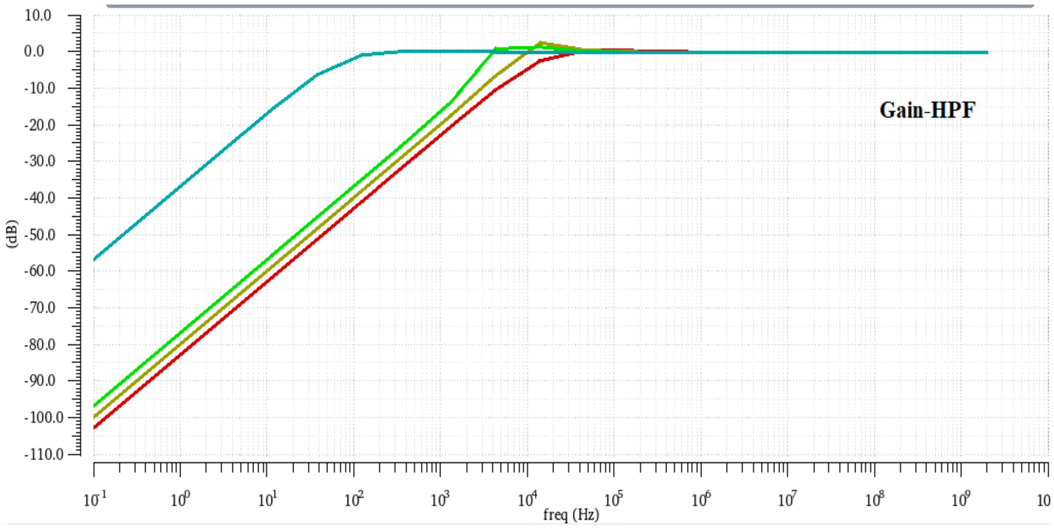

Figure 14. Frequency response of the HPF for different capacitors

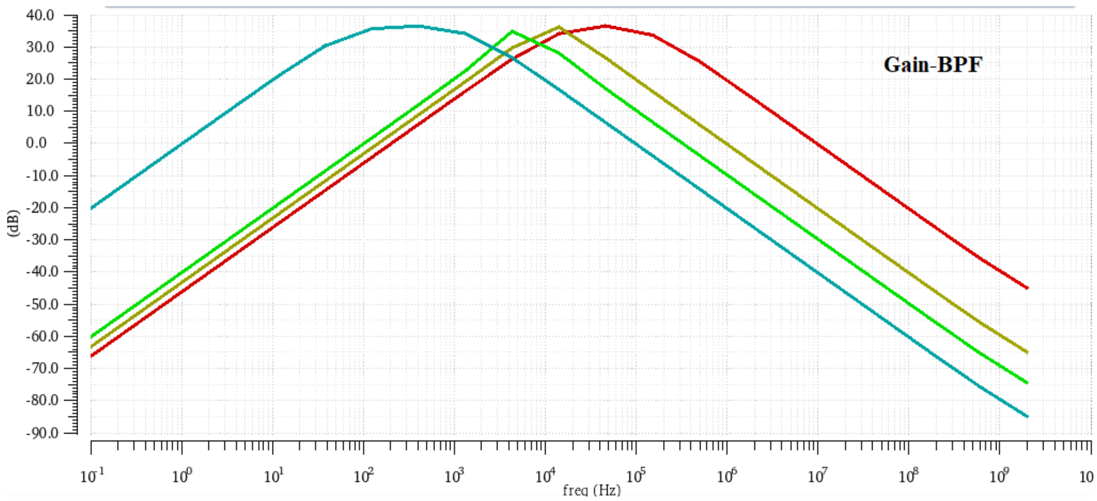

Figure 15. Frequency response of the BPF for different capacitors

TABLE 1: PERFORMANCE OF UNIVERSAL FILTER

High pass filter	Lowpass filter	Band pass filter	Cutoff frequency Of HP	Cutoff frequency Of LP	Lower Cutoff frequency Of BP	Higher Cutoff frequency Of BP
500nF	5mF	10pF	13.03KHz	15.66KHz	13.13KHz	168.8KHz
700nF	10mF	100pF	6.96KHz	12.86KHz	9.00KHz	23.29KHz
1uF	100mF	300pF	2.99KHz	9.51KHZ	3.22KHz	8.00KHz
100uF	500mF	1nF	0.08KHz	0.07KHz	0.09KHz	1.46KHz

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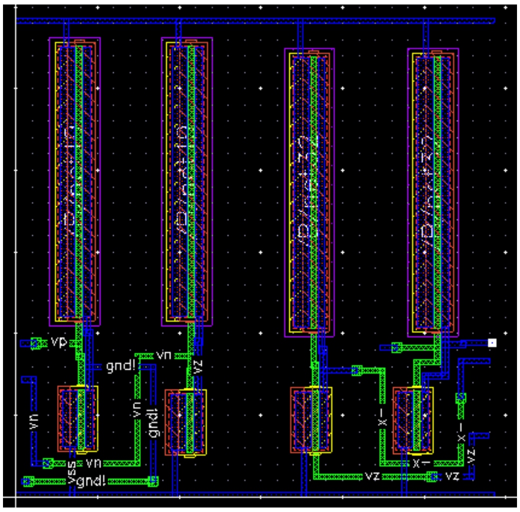

Figure 16. Layout of VDTA

IV. CONCLUSION

This paper provides High Pass (HP), Low Pass (LP) and Band Pass (BP) filters with a cut-off frequency of 110.15 KHz, 738.86 KHz, and 1.55 MHz.with a single VDTA-based filter, low power and compact CMOS implementation requirements are met. By replacing passive resistance with NMOS active resistance, the filter occupies less space and provides high noise immunity. It also provides tuneability to the filter.

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