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Power efficient timing error tolerant circuit design based on clock pulse correction

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Abstract: Timing error is now getting increased attention due to the high rate of error-occurrence on semiconductors. Even slight external disturbance can threaten the timing margin between successive clocks since the latest semiconductor operates with high frequency and small supply voltage. To deal with a timing error, many techniques have been introduced. Nevertheless, existing methods that mitigate a timing error mostly have time-delaying mechanisms and too complex operation, resulting in a timing problem on clock-based systems and hardware overhead. In the proposed work a novel timing-error-tolerant method that can correct a timing error instantly through a simple mechanism is demonstrated. By modifying a clock in a flip-flop, the proposed system can recover a timing error without the loss of time in the clock-based system.

Furthermore, in order to reduce power consumption in the stages were operation is not performed, gating mechanism is used to reduce the unwanted transition. Clock Gating computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It has however a big advantage of avoiding the tight timing constraints of earlier methods, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gaters. Due to the compact mechanism, the proposed system has low hardware overhead in comparison with existing timing-error-tolerant systems that can recover the error instantly. To verify our method, the proposed circuit is designed using Verilog HDL and simulated by Modelsim. Further, synthesis and power analysis is performed using Xilinx ISE.

Keywords: Error-tolerant systems, soft error, timing error, clock gating.

I. INTRODUCTION

The timing-error rate is increased as the clock frequency is increased. Since the clock period is getting minimized, critical paths in the circuit are susceptible to timing errors [1], [2]. Furthermore, variations on the CMOS process, power supply, and temperature impact the performance of modern integrated circuits, which results in the high incidence of timing errors.

As the supply voltage decreases, the delay of the circuit can drastically change between the typical case and the worst case of process, voltage, and temperature (PVT) conditions [3]. With the 0.4-V operation, the logical path with the worst case is 12x slower than that with the typical case [4]. Moreover, transistor aging issues are critical for the occurrence of timing errors [5], [6]. Due to the negative-bias temperature instability (NBTI) in CMOS, the threshold voltage is lowered, which finally increases the path delays of logics. Hence, a timing-error-tolerant method is highly required in order to implement reliable systems.

The timing error occurs because of the delay in combinational circuits that are located between the memory elements. After the edge of the clock, the delayed data cannot be stored in the memory element properly. To deal with the timing error, many related methods have been proposed [7]. One of the representative methods of timing-error-tolerant systems is the temporary error-detection system [7], [8]. By comparing the output of a flip-flop with a delayed output, it detects the transient timing error that is propagated from the input with low hardware overhead.

However, it only detects an error with a delayed time and cannot correct the error. Based on the previous system with the delaying technique, other systems have been proposed for timing-error detection and correction in the microprocessor design [9], [10]. They compare an input of a flip-flop and an output of a flip-flop with an XOR gate. By using XOR gates and memory elements, the output is corrected when a fault signal is flagged.

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II. RELATED WORK

Stefanos Valadimas, Yiorgos Tsiatouhas and Angela Arapoyanni, (2016) in the paper "Timing Error Tolerance in Small Core Designs for SoC Applications", described the idea of local error detection and correction technique is based on a new bit flipping flip-flop. Whenever a timing error is detected, it is corrected by complementing the output of the corresponding flip-flop. The proposed solution is characterized by very low silicon area and power requirements compared to previous design schemes in the open literature.

Mehrzad Nejat, Bijan Alizadeh and Ali Afzali-Kusha, (2015) in the paper "Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance Improvement of Low-Power Digital Circuits Prone to Variations" proposed dynamic flip-flop (FF) conversion method of time borrowing (TB) for improving the performance of digital systems prone to variations. An improved structure that mitigates timing problem by automatically closing the window after the arrival of late data. This method was compared with soft edge FF and dynamic clock stretching through simulations on different ITC'99 benchmarks.

Mehrnaz Ahmadi, Sahand Salamat and Bijan Alizadeh, (2019) in the paper "A Timing Error Mitigation Technique for High Performance Designs" described a dynamic flip-flop conversion (DFFC) is a time borrowing method which converts the critical flip-flops into transparent latches to allow timing slacks pass between pipeline stages of given circuits. However, our previous DFFC methods suffer from false error prediction. It means even when there is no setup time violation, our previous method incorrectly issues timing error.

Yiqun Zhang, Mahmood Khayatzadeh, Kaiyuan Yang, Mehdi Saligane, Nathaniel Pinckney, Massimo Alioto, David Blaauw and Dennis Sylvester, (2018) in the paper " iRazor: Current-Based Error Detection and Correction Scheme for PVT Variation in 40-nm ARM Cortex-R4 Processor" presented iRazor, a lightweight error detection and correction approach, to suppress the cycle time margin that is traditionally added to very large scale integration systems to tolerate process, voltage, and temperature variations. iRazor is based on a novel current-based detector, which is embedded in flip-flops on potentially critical paths. The proposed iRazor flip-flop requires only three additional transistors, yielding only 4.3% area penalty over a standard D flip-flop.

Hakan Baba and Subhasish Mitra, (2009) in the paper "Circuit Failure Prediction and Its Application to Transistor Aging" proposed a circuit failure prediction that predicts the occurrence of a circuit failure before errors actually appear in system data and states. This is in contrast to classical error detection where a failure is detected after errors appear in system data and states. Circuit failure prediction is performed during system operation by analyzing the data collected by sensors inserted at various locations inside a chip.

Martin Omaña, Daniele Rossi, Nicolò Bosio and Cecilia Metra, (2013) in the paper " Low Cost NBTI Degradation Detection and Masking Approaches" described a performance degradation of integrated circuits due to aging effects. Negative Bias Temperature Instability (NBTI) is becoming a great concern for current and future CMOS technology. In this paper, two monitoring and masking approaches that detect late transitions due to NBTI degradation in the combinational part of critical data paths and guarantee the correctness of the provided output data by adapting the clock frequency is proposed.

III. TIMING-ERROR-TOLERANT SYSTEM

A new timing-error-tolerant system that can correct timing error is developed. When a timing error causes a delayed arrival of an input on a flip-flop, the proposed system can detect a delayed input of the flip-flop, and the flip-flop passes through the data by making a transparent window. As described in Fig. 1(a), the proposed system consists of a "transition detector" and "master clock generator."

The "transition detector" detects the input transition of a flip-flop, and it produces a pulse of the error-flagged signal. Based on the output of the transition detector, the "master clock generator" produces a pulse for a certain period only when a clock is high. While a pulse is "1," the flip-flop passes the input to the output since the pulse makes a transparent window by controlling a clock of master in the flip-flop.

Thus, the abnormal data that are stored in the flip-flop can be restored with delayed normal data. To avoid hold time violation, a pulse is generated with a minimum time, which is required for the setup time.

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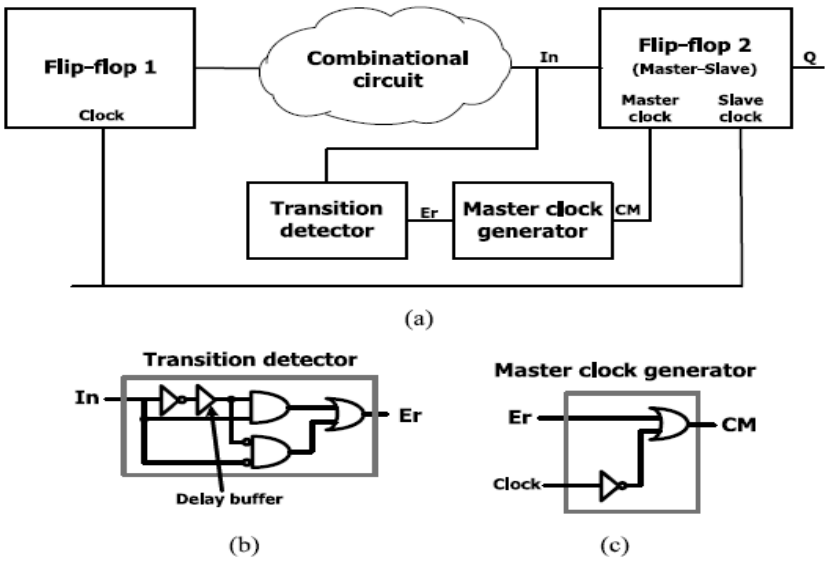

Fig. 1. Circuit of the proposed timing-error-tolerant system. (a) Circuit diagram of the proposed system. (b) Circuit of transition detector. (c) Circuit of the master clock generator.

As shown in Fig. 2, the recovery process of a timing error in the proposed system is fully addressed. When a timing error occurs on the input data of the flip-flop 2, it stores abnormal data to the output Q due to the delayed input data. After the delayed normal data have arrived on the input of flip-flop 2, the transition detector that is located between a combinational circuit and the flip-flop 2 generates an error pulse. The transition detector detects both a rising edge of the data and a falling edge of the data by using an inverter and the AND gate.

Furthermore, by implementing a delay buffer in the transition detector, the transition detector generates a customized period of a pulse, which maintains the transparent window for enough time. The master clock generator makes a clock of the master (CM) based on the error pulse and clock. Due to the OR gate and inverter in the master clock generator, a CM is high for a certain period of time after a timing error occurs. While the CM is high, the flip-flop 2 becomes transparent, and the delayed normal input is stored through flip-flop 2.

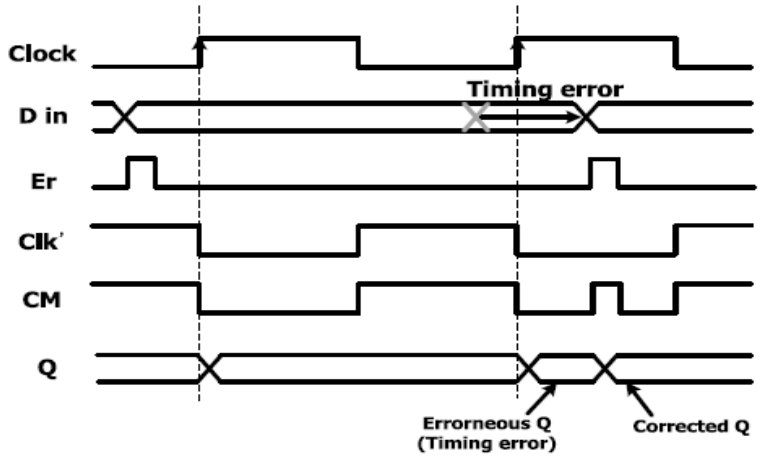

Fig. 2. Operation of the proposed system when a timing error occurs.

Thus, the erroneous output Q is corrected with the normal input. Since the timing error mostly occurs after a rising edge of the clock, the proposed system detects and corrects the timing error, while the clock is high. The proposed method is applied to the critical paths where the delay of the combinational circuit is longer than the half time of the clock period. The proposed error tolerant circuit with time-borrowing circuit and clock gating circuit is shown in Fig. 3.

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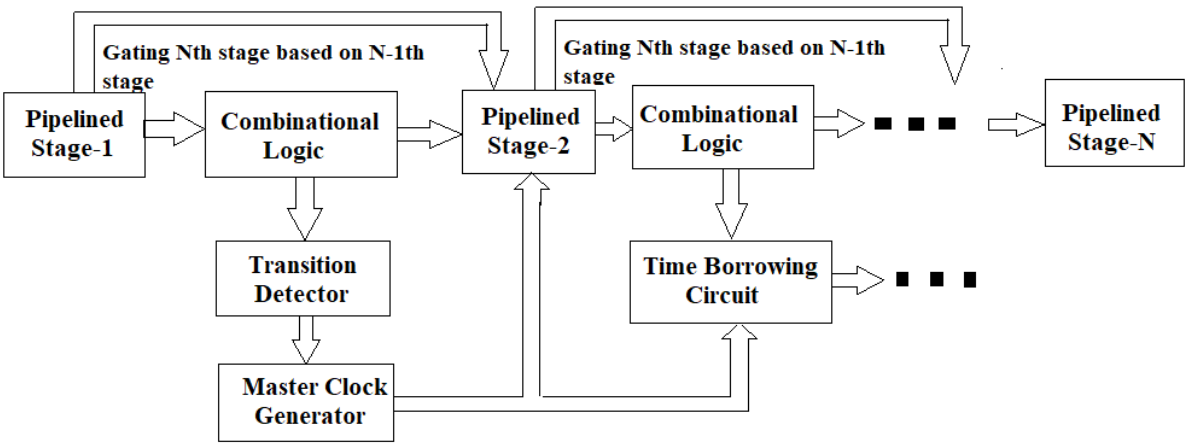

Fig. 3. Proposed Timing-error-tolerant circuit.

A.Time-Borrowing Technique

Using the information acquired from the timing analyzing tool, the critical paths of the circuit and the setup-time information of each element in the circuit are determined. We make full use of such results to choose the best location for our proposed system. If a single-stage error occurs, the delayed arriving data signal is recovered because the master latch is transparent for the pulse period. However, if a successive-stage error occurs due to the lack of setup time in the second-stage flip-flop, the delayed arriving data signal in the second stage cannot be stored because of the setup-time violation. To deal with the successive-stage error, we devised the time-borrowing technique. The time-borrowing circuit is provided in the second stage, as shown in Fig. 3.

As shown in Fig. 4, the operation of a time-borrowing circuit is addressed. When a timing error occurs on the input data of the first stage, the CM signal is set to "1," which also induces the CM_SR high level. After CLK is fallen, Q is set to "1." While the Q signal sets the high period, the delayed CLK (CLKDD) is chosen as the main CLK for the second stage. After all, the new CLK maintains a transparent window for enough time. A CM is high for a certain period of time after a timing error occurs. Thus, the delayed data can be stored as normal data. The time-borrowing scheme can be used on any location that has a short setup time for the flip-flop.

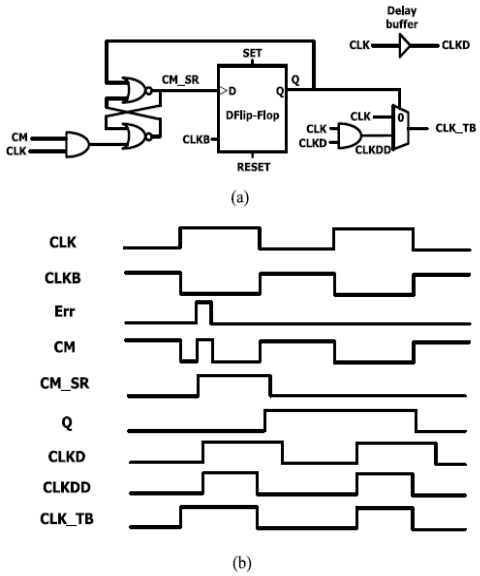

Fig. 4. Time-borrowing technique. (a) Time-borrowing circuit structure. (b) Operation of the time-borrowing system.

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IV. POWER EFFICIENT CLOCKING MECHANISM

Clock gating is very useful for reducing the power consumed by digital systems. Three gating methods are known. The most popular is synthesis-based, deriving clock enabling signals based on the logic of the underlying system. It unfortunately leaves the majority of the clock pulses driving the flip-flops (FFs) redundant.

A.Auto gated FF

The basic circuit used for LACG is Auto-Gated Flip-Flip as shown in Fig.5. The FF's master latch becomes transparent on the falling edge of the clock, where its output must stabilize no later than a setup time prior to the arrival of the clock's rising edge, when the master latch becomes opaque and the XOR gate indicates whether or not the slave latch should change its state. If it does not, its clock pulse is stopped and otherwise it is passed. A significant power reduction was reported for register-based small circuits, such as counters, where the input of each FF depends on the output of its predecessor in the register. AGFF can also be used for general logic, but with two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

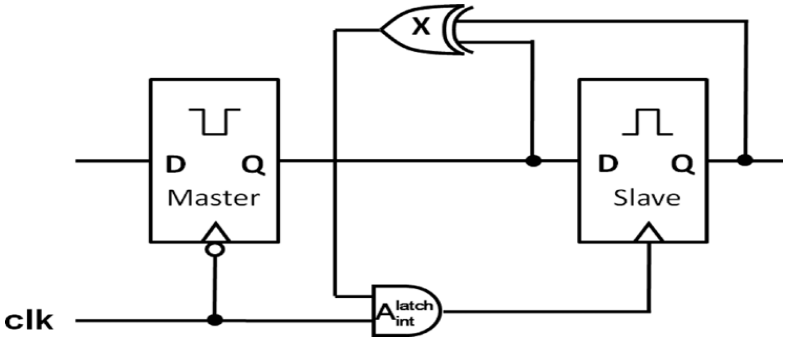

Fig.5 An auto-gated flip-flop.

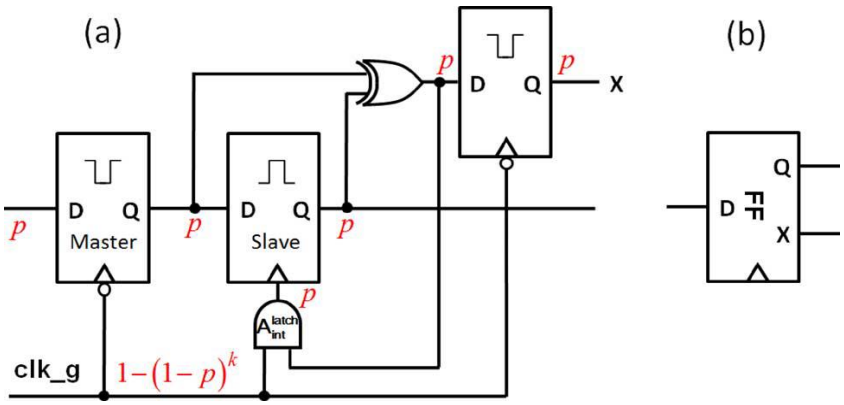

Fig.6 Enhanced AGFF with XOR output used for LACG.

LACG is based on using the XOR output in Fig.6 to generate clock enabling signals of other FFs in the system, whose data depend on that FF. There is a problem though. The XOR output is valid only during a narrow window of around the clock rising edge, where and are the FF's setup time and clock to output contamination delay, respectively. After a delay the XOR output is corrupted and turns eventually to zero.

To be valid during the entire positive half cycle it must be latched. Fig.6b is the symbol of the enhanced AGFF with the XOR output. The power consumed by the new latch can be reduced by gating its clock input. Such gating has been proposed in and it involves another XOR and OR gates, useful for high clock switching probability.

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V. EXPERIMENTAL RESULTS

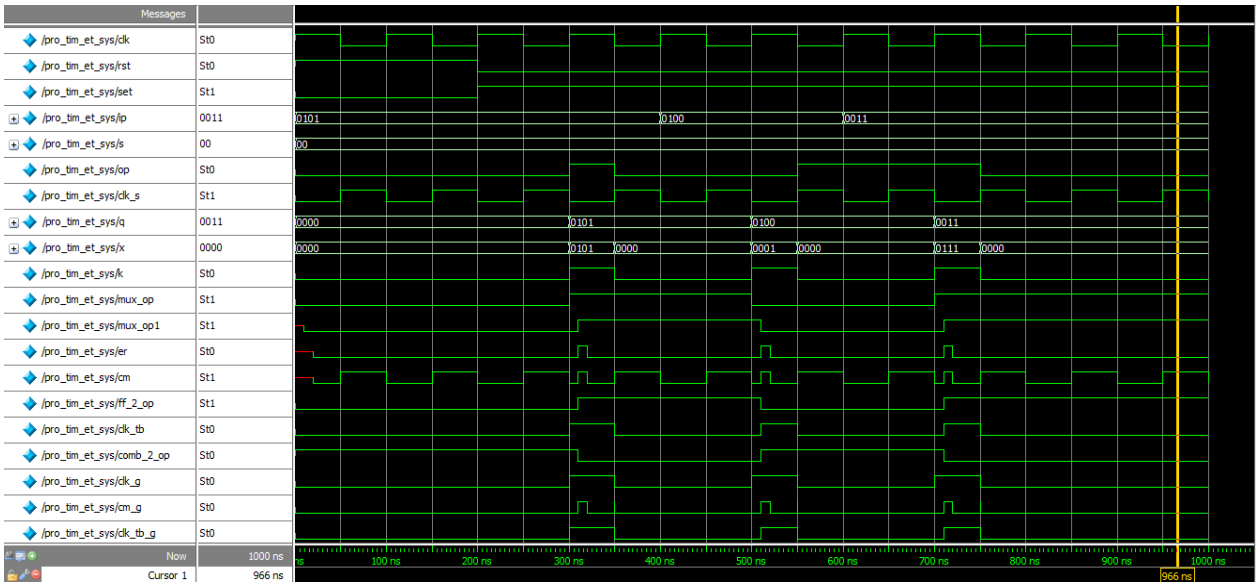

Fig.7 Simulation result of proposed timing error tolerant system

Fig.7 shows the simulation of the waveform which contains IP as the input of the transition detector and CLK, ER is the input of the master clock generator simulated using Modelsim software. CM is the output of master clock generator which acts as master clock of the next FF. The "transition detector" detects the input transition of a flip-flop, and it produces a pulse of the error-flagged signal. Based on the output of the transition detector, the "master clock generator" produces a pulse for a certain period only when a clock is high. Thus, the abnormal data that are stored in the flip-flop can be restored with delayed normal data. To avoid hold time violation, a pulse is generated with a minimum time, which is required for the setup time. The clock signal CLK_TB act as a gated clock which is inactive during clock gating mode. To deal with the successive-stage error, the time-borrowing technique is used. Fig. 8 shows the power comparison of timing error tolerant system designed using power gating technique and compared with existing method.

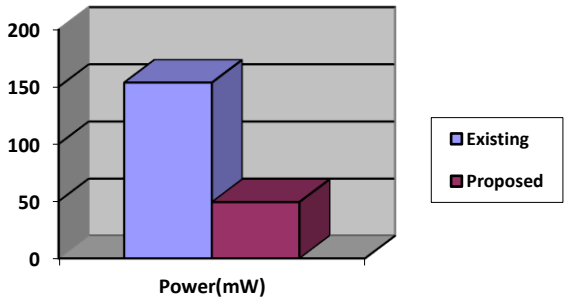

Fig. 8 Power comparison

VI. CONCLUSION

A timing-error-tolerant method that can correct a timing error immediately with a compact circuit structure is proposed. In the critical path, the abnormal data transition after the edge of the clock can be detected and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing technique that deals with the successive-stage error is introduced. If the timing error occurs in the second stage successively, modified CLK maintains the transparent window during enough period of time for timing-error tolerance without changing system CLK. Further to eliminate unwanted transition clock gating is incorporated into the error tolerant design. Compared with existing systems, it is proven that the proposed system has a better performance with a lower hardware overhead in large size of circuits along with low power consumption.

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