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DESIGN OF APPROXIMATE ADDER FOR IMPROVING PERFORMANCE OF A SYSTEM IN IMAGE PROCESSING APPLICATIONS

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Abstract: In the previous full adder circuits, it is occupying more area and power consumption. In this project the adder circuit is designed by using the minimum number of gates and error tolerant adders to reduce the power consumption and to use the areaefficiently. The two versions of 16-bit ETA's wereused. Such as Low power and area efficient Error Tolerant Adder (LETA) and Improved Low power andarea efficient Error Tolerant Adder (ILETA). It uses the Most Significant Bit (MSB) to access the data. In our proposed system we have used the Digital Image Processing (DIP), and this have used in imaging processing and image blending algorithm is implemented and it is simulated by using XILINX with the mentioned advantages. In these proposed ETA's, the most significant bit (MSB) segments are realized in same approach, whereas the least significant bit (LSB) segment of LETA and ILETA arerealized using a proposed IFAs and existing modified full Adder (MFA), respectively. The proposed and existing Error Tolerant Adders (ETA) are implementedusing asynthesized in a Synopsys electronic design automation (EDA) Tool using Taiwan Semiconductor Manufacturing Company (TSMC) 65nm technologyand Verilog hardware description language (HDL). A new performance metric namely power and error product (PEP) is suggest in order to evaluate the approximate adders in terms of error and power metrics. It is found that the proposed ILETA achievesa low PEP of 1.05×10 2 compared with other ETA's.

I. INTRODUCTION

Arithmetic and logic unit has been the important unit in any electronic devices. In the recent evolution, for an arithmetic and logic unit to be notable it needs to have an efficient algorithmic operation such as Additions and Multiplication. They take part in a critical role in the applications of digital signal processing and image processing. The arithmetic and logic operations in DSP are performed by using arithmetic units such as multipliers and adders. These arithmetic units decide the performance of the processors and computational complexity. Hence, optimization of these arithmetic units is necessary to enhance the performance of DSP processors. Among the carry select adders and a existing multi-bit adderis the fastest with complexity in hardware. The adders canbeperceive with lesser complexity in hardware by adopting approximate computing. For a Multiplier and adder to be effective and efficient in terms of performance which needs to be high speed or consume less power or to be time effective. Reduction in delay produce the overall computation time decrease. Area and delay are the two major conflicting constraints.

The adders are basic units in designing DSP processors, hardware level of abstraction is adopted for designing approximate adders or multipliers. The key feature in designing an approximate full adder (AFA) is to reduce the carry propagation time and hardware reduction.A survey of approximate adders is presented in previous studies. Approximate mirror adders (AMAs) are realizedwith lesser number of transistors. This results in reduction ofcircuit complexity, dynamic power dissipation and node capacitance. Three exact full adders are formulated by adopting the low power and area efficient error tolerantadder (ILETA), and the performances are evaluatedbased on structural and error analyses.

II. PROPOSED SYSTEM

2.1. ERROR TOLERANT ADDERS:

In this proposed system we have used the 1-bit imprecise full adder with less gate count And Two versions of 16-Bit ETA's so that it requires low power consumption and low area. AFAs are used forrealizing. By this system adders exhibit (55%, 50%) reduction in power consumption and achieve significant reduction in area (68%, 61%). Further, in this work, a new performance metric namely power and error product (PEP) is proposed in order to evaluate the approximate adders in terms

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of power anderror metrics. It is establish that the proposed ILETA achieves a low PEP of 1.05×10-5 compared with other ETAs. To study the potency of the proposed ETAadders in image processing application.

The LETA is established by using a MFA and a modified half adder (MHA) in the imprecise part. In MHA, the sum is equal to EXOR of both the inputs andthe carry signal is equal to the input of the MHA. The MHA make a one-bit error in the carry signal.

A low power and area efficient carry select adder (LCSLA) is utilized in the MSB segment of the proposed LETA. The LCSLA is implemented by using 1 multiplexer and7 basic gates1 multiplexer. Hence, the precise of LETAis carry out with 88 basic gates, and imprecise part is implemented with 60 basic gates. 148 basic gates are required to implement LETA, which exhibit significant reduction in area. The error probability is close to HSETA.

The ILETA is formulated with a proposed 1- bit IFA in the imprecise part and precise part of the ILETA is identical to the LETA. The advantage of ILETA is that it requires only 40 basic gates for precise part and 88 basic gates for imprecise part with regards to its counter models. The logical gate count calculation 15 of existing error tolerant adders, namely the ET_CSLA, SAET_CSLA, HSETA, HPETA, and proposed error tolerant adders, namely the LETA and ILETA, are compared with the Conv CSLA.

Advandages:

1) This system requires less number of gates andtransistors.
2) It requires lower area.
3) It reduces the low power consumption

2.2 IMPRECIES FULL ADDER:

The full adder is used to add three 1- bit double figures X1, X2, and carry X3. The full adder has three input countries and two affair countries i.e., sum and carry. In this squishy full adder the combination of OR, And NOTgates were used then to add the given inputs.

Different types of exact multi-bit high speed adders similar as a ripple carry adder, carry look ahead adder, carry select adder, and carry skip adder are realized in the literature. Among all the exact adders, carry select adder remains asa highspeed adder with area above. The debit of areaover head in a carry elect adder (CSLA) is overcome by espousing approximate computing and also named aserror tolerant carry elect adder (ET_CSLA). analogous tothis consummation, colorful error tolerant adders are realized in the literature.

TheET_CSLA12 is formulated by using the AFA as a structure block. For A 16- bit ET_CSLA, it requires 28 AFA and 15 multiplexers. A1- bit AFA requires 6 introductory gates, whereas one 21 multiplexer requires 4 introductory gates. Hence, total gate count requires toapply the 16-bitET_CSLA is 228 introductory gates andis given. The ET_CSLA is enforced with roughly 50 lower gates compared to the exact carry elect adder (conventional CSLA (Conv CSLA)).

The LETA is established by using a MFA and a modified half adder (MHA) in the in accurate part. In MHA, the sum is equal to EXOR of both the inputs andthe carry signal is equal to the input of the MHA. The MHA produces a one- bit error in the carry signal. A low power and area effective carry elect adder (LCSLA) is employed in the MSB member of the proposed LETA. The LCSLA is enforced by using 7 introductory gates and 1multiplexer. Hence, the accurate part of LETA is enforced with 88 introductory gates, and inaccurate part is executed with 60 introductory gates. 148 introductory gates are needed toapply LETA, which shows significant reduction in area.

In the below table,

1. 'X1' and' X2' are the input variables. These variables means the two significant bits which are going to be added.
2. 'X3' is the third input which represents the carry. From the previous lower significant position, the carrybit is raised.
3. The 'Sum' and 'Carry' are the output variablesthat determine the output values.

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TABLE 1.1 IFA Truth Table

INPUTS			**EXACT OUTPUTS**	
X1	**X2**	**X3**	**CARRYX1**	**SUM** $\overline{X1}$**(X2 +X3)+(X2.X3)**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

SOP form can be obtained with the help of K-map as:

X1 \ X2X3	00	01	11	10
0	0	0	0	0
1	1	1	1	1

CARRY : X1

X1 \ X2X3	00	01	11	10
0	***0***	***1***	***1***	***1***
1	*0*	*0*	***1***	*0*

SUM :X1(X2+X3)+(X2.X3)

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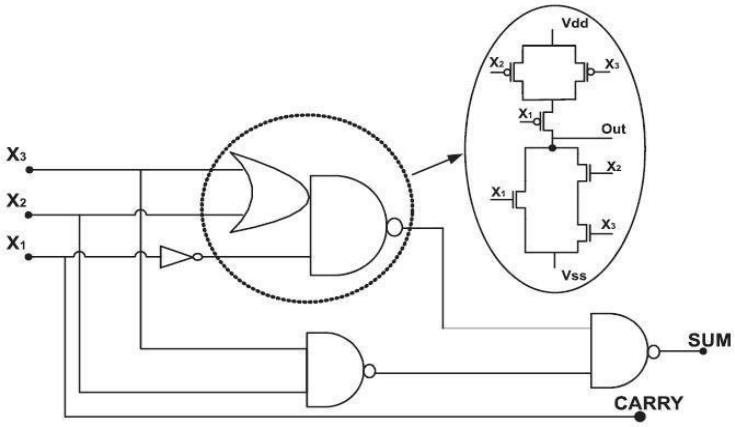
Circuit diagram:



Show this abstraction by proposing various imprecise or approximate Full Adder (FA) cells with reduced complexity at the transistor level, and make use of them to design approximate multi-bit adders. In addition to the intrinsic reduction in switched capacitance, our techniques result in remarkably shorter critical **paths,authorizing voltage scaling.** We design architectures forvideo and image compression algorithms using the proposed approximate arithmetic units, and evaluate them to demonstrate the efficacy of our approach. Post-layout simulations designate area r savings of up to 37% and power savings of up to 60% with an insignificant loss in output quality, when differentiated to existing implementations.

2.3 SOFTWARE DESCRIPTION

2.3.1 XILINX

Xilinx ISE (Integrated Synthesis Environment) is a discontinued software tool from Xilinx for analysis and synthesis of HDL designs, which essentially targets development of embedded firmware for CPLD integrated circuit (IC) product families and embedded firmware for Xilinx FPGA. Use of thelast declared edition from October 2013 continues for in-system programming of legacy hardware designs containing older CPLDs and FPGAs otherwise grieving by the replacement design tool, Vivado Design Suite.

ISE allows the developer to synthesize ("compile") their designs, perform timing analysis and examine RTL diagrams, simulate a design's reaction to individual stimuli, and arrange the target device with the programmer. Other components shipped with the Xilinx ISE include the Embedded Development Kit (EDK), a Software Development Kit (SDK) and Chip Scope Pro. The Xilinx ISE is primarily used for circuit design and synthesis, while ISIM or the Model Sim logic simulator is usedfor system-level testing. As commonly performed inthe commercial electronic design automation sector, Xilinx ISE is tightly-coupled to the architecture of Xilinx's own chips (the internals of which are highlyproprietary) and cannot be used with FPGA products from other vendors. specified the highly exclusive nature of the Xilinx hardware product lines, it is rarely possible to use open source alternatives to tooling if directly from Xilinx, although as of 2020, some exploratory attempts are beingmade.

2.3.2 SYNTHESIS AND SIMULATION DESIGNGUIDE

The Synthesis and Simulation Design Guide provides a general overview of designing Field Programmable Gate Array (FPGA) devices using a Hardware Description Language (HDL).It includes design hints for the novice HDL user, also for the experienced user who is designingFPGA devices for the first time. Before using the Simulation and Synthesis Design Guide, you should be familiar with the operations that are common to all Xilinx tools.

The Simulation and synthesis Design Guide does notaddress certain topics that are major when creating HDL designs. The design samples in this Guide were:

1) Created with VHDL and Verilog.
2) Xilinx endorses Verilog and VHDL equally. VHDL may be extra tough to learn than Verilog and usuallyrequires extra explanation.

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a. Compiled with several synthesis tools
b. Targeted for the ensuing devices:

- Spartan -3
- Spartan-3E
- Spartan-3A
- Spartan-6
- Virtex-4
- Virtex-5

2.3.3 HARDWARE DESCRIPTION LANGUAGE (HDL):

1)This chapter reports Hardware DescriptionLanguage (HDL).
2)Advantages of Using a Hardware DescriptionLanguage (HDL)to Design FPGA Devices
3)Designing FPGA Devices with HardwareDescription Language (HDL) Designers use an HDL to describe the behaviour and structure of system and circuit designs.
4)Perception FPGA architecture allows you to create HDL code that successfully uses FPGA system features. To learn more about designing FPGA devices with HDL:
a. apply in training classes provided by Xilinxand by synthesis tool vendors.
b. analysis the HDL design samples in thisGuide.
c. Download design examples from XilinxSupport.
5)Take advantage of the many other resourcesprovided by Xilinx, including:

a. Documentation
b. Tutorials
c. Service packs
d. Telephone hotline
e. Answers database

2.3.4 ADVANTAGES OF USING A HDL

Using a Hardware Description Language (HDL) to design high-density FPGA devices has the followingadvantages:

1) Top-Down Approach for Large Projects
2) Functional Simulation preliminary in theDesign Flow
3) Synthesis of Hardware Description Language(HDL)Code through Gates
4) Early Testing of Various DesignImplementations
5) Reuse of Register Transfer Level (RTL)Code.

2.3.5 COMMON CODING STYLE

Xilinx recommends that your design team accept on a coding style at the starting of your project. An accepted coding style allows you to understand and read code written by your team members. Ineffective coding styles can resentfully impact synthesis andsimulation, resulting in slow circuits. Because portions ofexisting Hardware Description Language (HDL) designs are often used in new designs, you should follow coding standards that are understood by the majority of HDL designers. This Guide describes recommended coding styles that you should establish before you begin your designs.

1) utilize Xilinx naming conventions for naming signals, variables, and instances that are converted into nets, buses, and symbols.
2) keep away from Verilog keywords (such as module, reg and wire) even when coding in VHDL.
3) A user-generated name should not hold a forward slash (/). The forward slash is generally used to indicate ahierarchy separator.
4) Names should hold at least one non-numericcharacter.
5) Names should not hold a dollar sign ($).

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6) Names should not use less-than (<) or greater-than signs (>). These signs are sometimes used to indicate a bus index.
7) Device construction names (like CLB, IOB ,andPAD , Slice)
8) allocated pin names (such as CLK and INIT)
9) GND and VCC
10) UNISIM elementary names such as BUFG, DCM and RAMB16
11) Do not use pin names like P1 or A4 for component names
12) For language-specific naming restrictions, see the Verilog reference manuals and VHDL. Xilinx does not suggested using escape sequences as illegal characters.

If you plan of action to import schematics, or to use varied language synthesis or verification, use thebulk restrictive character set.

2.3.6 NAMING GUIDELINES FOR SIGNALSAND INSTANCES

Naming conventions help you achieve:

1) Maximum line length
2) Coherent and legible code
3) allocation for varied VHDL and Verilogdesign
4) Consistent HDL code
5) Do not use reticent words for instance orsignal names.
6) Do not outstrip 16 characters for the length ofsignal and instance names, whenever conceivable.
7) Create signal and instance names that throwback their connection or cause.
8) Do not use varied case for any specific nameor keyword. Use either all capitals or all lowercase.

III. SIMULATION OF CIRCUITS

A. 16-bit CSA using FA1:

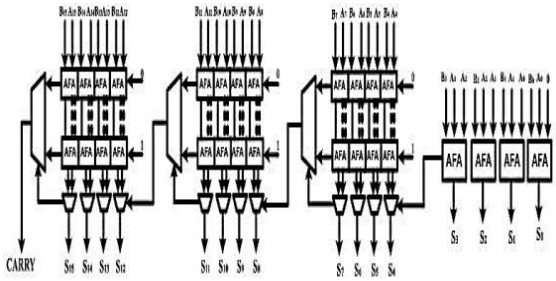

Fig. 2.1 16-bit FA1 Block diagram

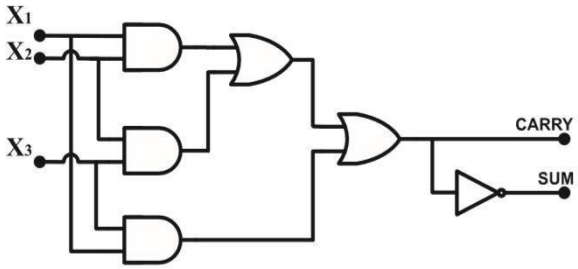

Fig. 2.2 16-bit FA1 Circuit diagram

The ET_CSLA, it may be observed that the ET_CSLA12 is formulated by using the AFA as a building block. For A16 – bit ET_CSLA, it requires 28AFA and 15 multiplexers. A1-bit AFA requires 6 basic gates, where as one 2:1 multiplexer requires 4 basic gates. Hence,total gate count requires to implement the 16-bitET_CSLA is 228 basic gates.The ET_CSLA is implemented with approximately 50% lesser gates compared to the exact carry select adder (conventional CSLA [ConvCSLA].

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B. 16-bit CSA using FA2 :

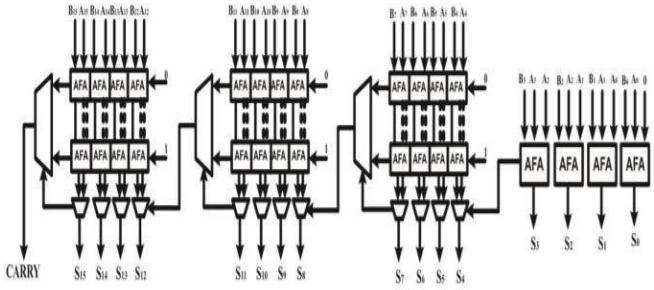

Fig. 2.3 16-bit FA2 Block diagram

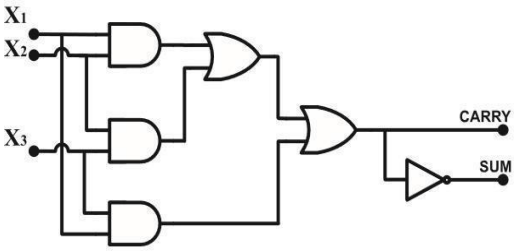

Fig.2.4 16-bit FA2 Circuit diagram

A significant approximation error tolerant carry select adder (SAET_CSLA) 12 is implemented to improve the error probability of ET_CSLA. The input operand to a 16-bit SAET_CSLA adder is segregated into a least significant bit (LSB) segment and most significant bit (MSB) segment. The LSB segment is termed as inaccurate part because their result in less weight in the output, and the MSB segment is termed as accurate part. In the SAET_CSLA, the in accurate and accurate part is realized by using the AFA and Conv CSLA, respectively.

C. 16-bit CSA using FA3:

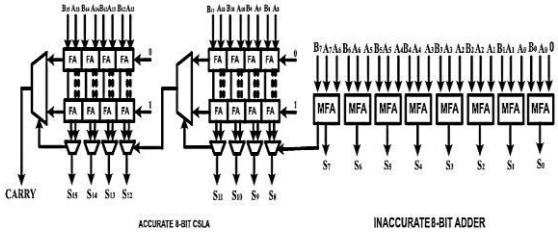

Fig.2.5 16-bit FA3 Block diagram

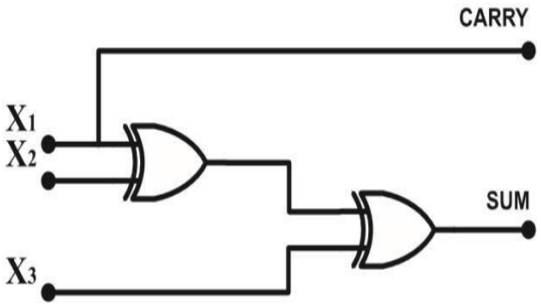

Fig.2.6 16-bit FA3 circuit diagram

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The hardware connivance of the SAET_CSLA is decreased in a high-speed error tolerant adder (HSETA). 15 The in accurate part is designed by using 64 basic gates whereas the accurate part is realized by using 248 gates and it basic gates are utilized or realize HSETA.

The inaccurate part of a 16-bit high- performance error tolerant adder (HPETA) 14 isdesigned by cascading several MBAFA, and the accurate part is based on ConvCSLA and ripple carry adder. The gate count of HPETA is 224 basic gates, it is far less compared with other existingerror tolerant adders.

D. 16-bit CSA using FA5:

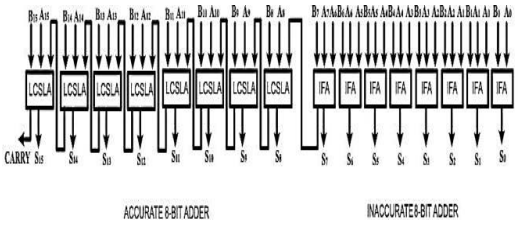

Fig.2.9 **16**-bit FA5 Block diagram

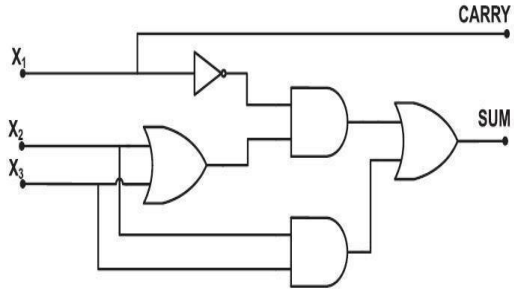

Fig.2.10 16-bit FA5 circuit diagram

The ILETA is prepare with a proposed 1-bit IFA in the inaccurate part and accurate part of the ILETA is similar to the LETA. The superiority of ILETA is that it requires only 40 basic gates for accurate part and 88 basic gatesfor inaccurate part with consider to its counter models. The logical gate count calculation15 of existing errortolerant adders, namely the ET_CSLA, SAET_CSLA, HSETA, HPETA, and proposed error tolerant adders, namely the LETA and ILETA, are compared with the ConvCSLA.

E. 16-bit CSA using FA6:

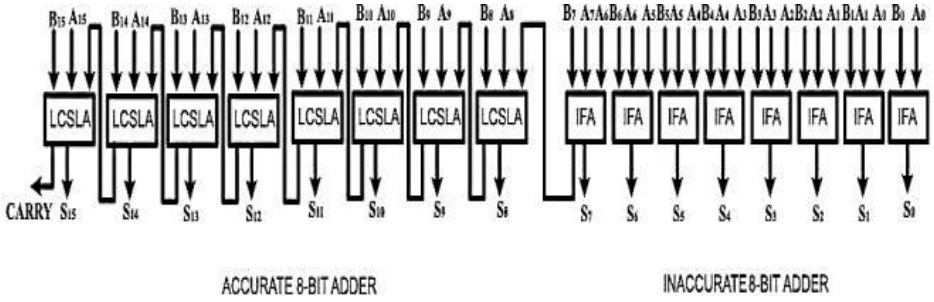

Fig.2.11 16-bit FA6 Block diagram

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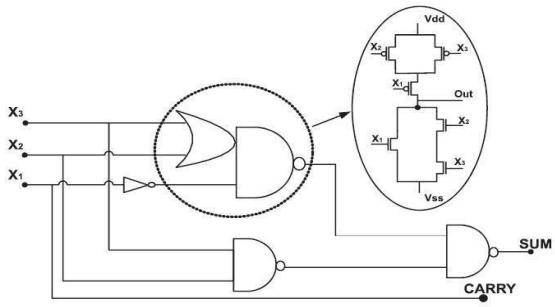

Fig.2.12 16-bit FA6 Circuit diagram

The Transistor level schematic of proposed IFA using 2- NAND gates 1-OAI logic,and 1-NOT gate. In that OAI logic requires 6 transistors, NOT gate requires 2 transistors, and NAND gate requires 4 transistors. as a consequence, the proposed IFA needs 16 transistors in total, which is smaller whendifferentiated to the transistor count of existing AFAs.

COMPARISON OF RESULT:

S.NO.	TYPE	NO. OF LUTS	SPEE D (NS)	POWER (UW)	ADP	PDP	AP P
1.	Conventional(CSA)	24	13.308	0.12	319.39	1.60	2.88
2.	FA1	24	14.568	0.093	349.63	1.35	2.23
3.	FA2	25	12.845	0.087	321.13	1.12	2.18
4.	FA3	20	9.061	0.074	181.22	0.67	1.48
5.	FA4	20	9.061	0.068	181.22	0.62	1.36
6.	FA5	20	9.061	0.054	181.22	0.49	1.08
7.	FA6	20	9.061	0.051	181.22	0.46	1.02

Post layout simulation Screenshot Result:

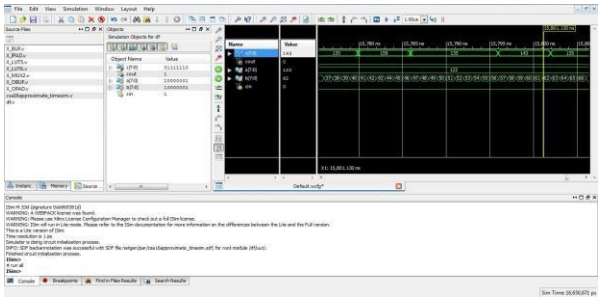

Fig.2.13 Post layout simulation Screenshot

Result 1. Simulation result:

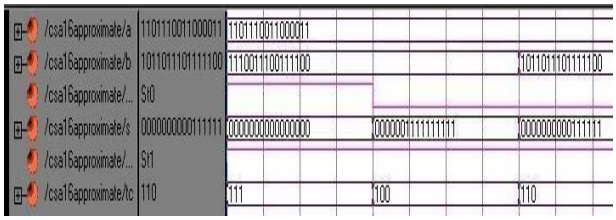

Fig.2.14 Simulation result Screenshot 1

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2.Simulation result:

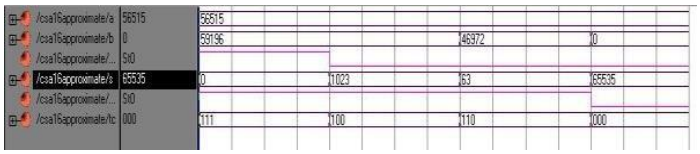

Fig.1.15 Simulation result Screenshot 2Technology Schematic Screenshot:

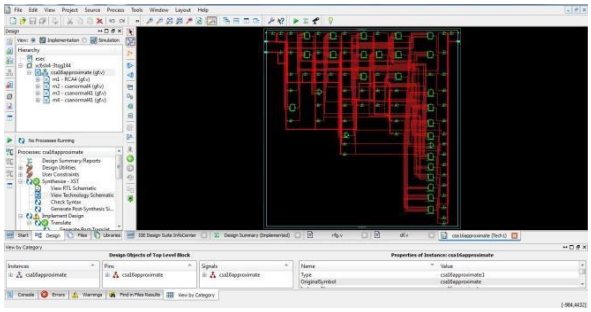

Fig.1.16 Technology Schematic Screenshot

B. Abbreviations:

AFA - Approximate Full Adder
ETA - Error Tolerant Adder
EFA - Exact Full Adder
ILETA - Improved Low power and area efficient Error Tolerant Adder
IFA - Imprecise Full Adder
LETA - Low power and area efficient Error Tolerant Adder
MSB - Most Significant Bit
MFA - Modified Full Adder

IV. CONCLUSION

In this project, the design of the LETA and ILETA is proposed with the modification on the accurate part and utilizing the proposed IFA in the inaccurate part of theETA. The proposed IFA records the minimum gate count with same error distance as the MBAFA. Several well-known approximate error tolerant adders, namely the ET_CSLA, SAET_CSLA, HSETA, and HPETA are reviewed and analyzed in terms of their gate count, structural metrics, error metrics, and image quality metrics. Further, ETAs are differentiated with a new performance metric PEP and is perceived that the ILETA reach a lower PEP value differentiated with existing ETAs. as well, the PSNR value is higher for the proposed ILETA, whichis necessary for image processing application.

Applications:

Digital image processing:

Digital image processing distribute with contrivancesof digital images between a digital computer. It is a subspecialty of signals and systems but focus specifically on images. DIP pivot on developing a computer system that is able to execute processing on an image. The input of that system is a digital image and the system process that image using structured algorithms, and shows an image as an output. The mostcommon example is Adobe Photoshop. It is one of the broadly used applications as processing digital images.

Aplications of digital image processing:

1) Image sharpening and restoration.
2) Medical field.
3) Remote sensing.
4) Transmission and encoding.
5) Machine/Robot vision.
6) Color processing.

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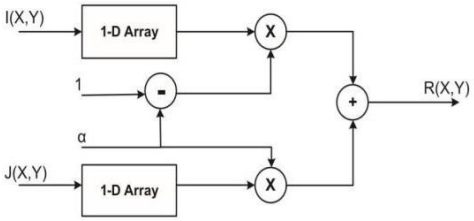
7) Pattern recognition.
8) Video processing.

Image blending application:

The concept of blending images is relativelyasy. We know that in order to copy an image wesimply transfer each source pixel's RGB values into a pixel in a target image. whether we directly restore the pixels of the target, in that case the result is a pasting of the source image into the target.



Example of image blending

Fig.3.1 The source image

Fig.3.2 The target image

Fig.3.3 Poisson blending

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Fig.1.20 Poisson blending with gradient mixing

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