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Design of Power efficient and low area FIR filter using Approximate Circuits

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Abstract: In DSP, the Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter plays a vital role in the design of a complex signal processing system. Most of the IIR filters are used in signal processing applications because of its less computational complexity as compared to the FIR filters. The FIR filter requires only fewer filter coefficients and less amount storage registers. In this research, I propose an FIR filter with Array multiplier and Carry Skip Adder (CSA) to improve hardware utilization and minimize the power of the overall design of an FIR filter. Carry skip Adder is also named as Carry by-pass adder which consists of special circuitry to improve the speed and reducing the carry propagation delay. This circuitry contains two main blocks namely, AND block and multiplexer block which are together defined as block propagate blocks.

Keywords: FIR (Finite Impulse Response), IIR (Infinite Impulse Response), SNR (Signal to Noise Ratio), FPGA (Field Programmable Gate Array), LUT (Look Up Table), CSA (Carry Skip Adder), RCA (Ripple Carry Adder), AM (Array Multiplier), IOB (Input Output Block). GDI (Gate Diffusion Input).

I.INTRODUCTION

With the explosive growth in multimedia applications, the need for low power and high-performance digital signal processing(DSP) devices is higher than ever. One of the most widely used operations performed in Digital Signal Processing is finite impulse response (FIR) filtering. In the field of digital signal processing, digital filters are most commonly used to suppress the harmonic components which rely on less analog circuitry and potentially allow a better Signal to Noise Ratio (SNR). Several digital filters are Characterized based on the strong potential to achieve different design constraints like area, speed, power consumption and delay. FIR filters are well known to have some unique attributes that improve the filtering process but suffer from non-linear phase responses.

At present, multiplication of bits is a common process in any of the algorithms used for processing of systems. The functionality of the algorithm is greatly dependent on functional parameters of multipliers. The parameters include extremely difficult to achieve with an analog implementation. In addition, the characteristics of a digital filter can be changed under software control. Therefore, they are widely used in adaptive filtering applications in communications such as echo cancellation in modems and speech recognition delay, memory and power.

The selection of multiplier plays a key role for efficient working of any algorithm. The selection of multiplier is concerned by observing the time delay and area of the multiplier. The delay and memory of any multiplier can be varied by using different adders.

II.FIR FILTER DESIGN

Finite impulse response filters are widely used in various DSP applications. This paper describes an approach to the implementation of low power –low area digital FIR filter based on field programmable gate arrays (FPGAs).The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips.it has lower costs than an ASIC for moderate volume applications. it also has more flexibility than the alternate approaches. MAC unit has become one of the essential building blocks in digital signal processing applications such as digital filtering, video coding, speech processing, and cellular phone.

$$Y(n) = \sum_{k=0}^{N-1} (h(k)X(N-k)) \quad (1)$$

Normally the filter structure has one delay element, one multiplier and one adder for each number of stages. This complete element is known as a tap. The number of stages depending upon the length of the filter. And this is directly proportional to the tap.The FIR filter represented by Equation.(1) has a general structure as shown in Fig.1.

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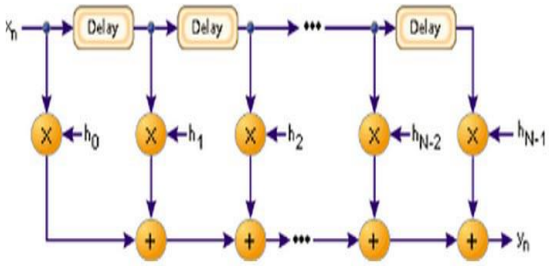

Fig.1 Structure of Digital FIR Filter.

The basic operation in the design of digital FIR filter is the estimation of transfer functions of filter coefficients. It finalise the filter response.Pipelining and parallel processing techniques is used in FIR filter .Pipelining is implemented using delay elements. Although the techniques results increases the overall speed of the system, also it increases the hardware requirement. Multiple inputs are processed for every clock cycle providing multiple outputs ,which would again increases the hardware complexity. The output of FIR filter is the unit convolution sample response by a system along with the signal input. Multiplication is one of the strongest operations that are performed in FIR filter.

The dominating block in Microprocessor and most DSP algorithms is the design of adder and design of multiplier which is for fast and slow execution time that decides the speed of the processor. By constructing an efficient multiplier an FIR filter can perform well.In this research work, an Array Multiplier and Carry Skip Adder is constructed in Verilog language. The simulation is carried out inModelSim software. Simulation results show that the proposed multiplier has less hardware utilization and the adder has low power consumption.

Numerous methodologies have been proposed in designing of FIR filter. In some researches the greater efficiency of the filter achieved by using low power carry increment adder and Vedic multiplier. The design proposed here describes that the FIR filter is unfolded by a factor 3 which concludes in constructing the filter with higher output. By employing all these three techniques such as energy efficient multiplier, low power adder and unfolded technique, the processing speed increases three times than that of the conventional FIR filter. The simulation was done using Xilinx. The achieved results also outperform the FIR Filter design .The high speed FIR filter with higher order length was carried out using the following techniques was also implemented .They are conventional adders and multiplier based FIR filter. It has full custom Distributed Arithmetic method and advanced add and Shift. They synthesized the proposed work in Xilinx Spartan and they concluded that advanced add and shift method of Finite Impulse Response filter achieves better results.

The design of FIR filter using registered adders and hardwired shifts was proposed in research. They revealed that. Because of the extensive use of modified sub expression algorithm in order to reduce the adders the performance result of the proposed work results better results. This filter design is suitable for higher order filter without degrading its performance.

III.CARRY SKIP ADDER.

A carry-skip adder or a carry-bypass adder is an adder implementation that improves on the delay of a Ripple Carry Adder with little effort compared to the other adders. The improvement of the worst-case delay is achieved by using many carry-skip adders to form a block-carry-skip adder. Unlike other fast adders, carry-skip adder (CSA) performance is increased with only some of the Combinations of input bits. That means, speed improvement is only probabilistic.

The layout of a ripple carry adder is simple. It allows for fast design time; however the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous FA(full adder). A 4 bit ripple carry adder formed by cascading four 1-bit full adders. Ripple carry adder is an alternative for which when half adder and full adders do not perform the addition operation when the input bit sequences are large.

The ripple-carry-adder advantages include the following.

- This carry adder has an advantage that we can perform addition process for n-bit sequences to get accurate results.
- The designing of this adder is not a complicated process.

Significantly, in the CSA circuit overall delay produced by the carry propagation is reduced by using the carry skip

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mechanism and helps to improve the overall speed of the addition operation.Using this addition concept, the multiplied values in the IIR filter design get added and produced the desired filter output. Initially, during the first clock cycle, the multiplied values are added with values in the accumulator and get stored in the accumulator itself. For the next clock cycle, the same input data is multiplied with the next filter coefficient which are produced the processing element results. For a multi bit operation every single 1-bit adder has its delay and the carry has to be propagated through the circuit. So the total delay becomes seemingly high.

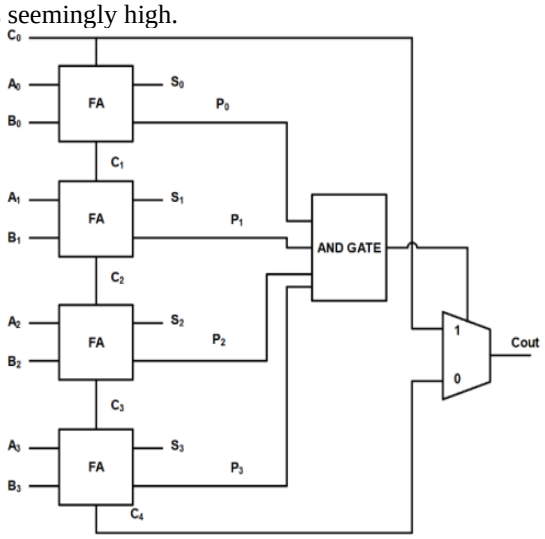

Fig.2 Block diagram of 4-bit Carry Skip Adder.

If Ai is not equal to Bi, then the propagate signal becomes logic 1 and , if Ai is equal to Bi then the propagate signal become logic 0. Then the propagate signal from each of the Full Adder blocks is given to the AND block. AND block performs the basic AND operation and produces logic 1 output if all the Pi is logic 1, otherwise, it generates logic 0 as the output. Further, the AND calculated output is given to Multiplexer block. It acts as a data selector. The multiplexer selects the required value based on the given input .If the input is logic1 multiplexer selects the C0 as the output. Here, the carry is bypassed to the output instead of propagating through all the blocks, which means carry is skipped instead of propagating and directly given to the output. If the multiplexer input is logic 0 then it selects the carry from the last Full Adder which is propagated from the initial FA.

It is fastest adder when compared to Ripple Carry Adder. It contains RCA which is used to increase the speed of carry chain. The implementation of this adder reduces the delay of a RCA. The carry skip adder has a skip logic block that can increase the speed of adder. There are two types of carry skip logic as shown in below fig.4 and fig.5.

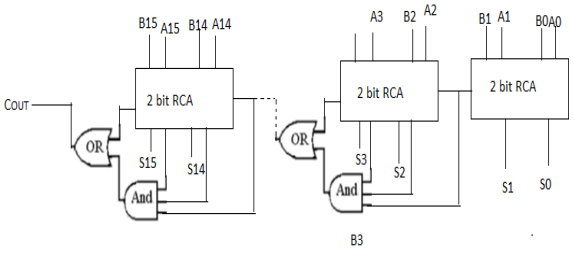

Fig.3 2 bit RCA block in 8 block CSA

Consider the 2-bit operation for a skip logic circuit as shown in below fig.4. This can be replaced by an OR gate.

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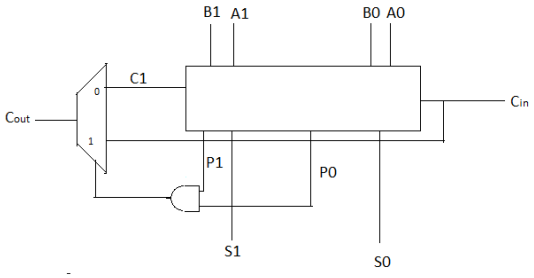

Fig. 4 Skip Logic in 2-bit CSA.

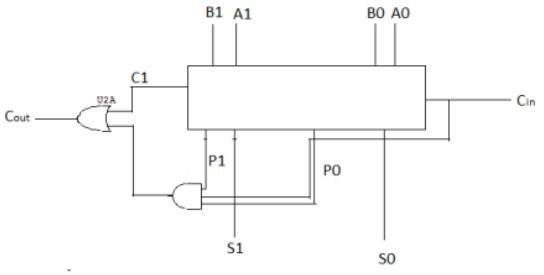

Fig.5 Skip Logic using OR gate.

Advantages of Carry Skip Adder includes:

• In higher bit operations the circuit response is good.

• Skip logic circuit is faster when compare to other circuits.

The delay values of various adders have been listed in Table 1.It shows the comparison of the maximum combinational path delay of the four adders for different number of bits.

Table.1 Comparison of propagation delay of variousAdders.

TYPE OF ADDER	8-BIT	16-BIT	32-BIT
Ripple Carry Adder	2.53	4.47	8.36
Carry Look aheadAdder	2.49	4.95	8.83
Carry Skip Adder	2.45	4.40	11.52
Carry Save Adder	4.80	8.40	15.61

From the delay comparison of adders, it is clear that Carry Skip Adder is the fastest. The delay performance of RCA for 4-bit and 8-bit operands are high compared to Carry Look Ahead Adder and Carry Skip Adder. The skipping mechanism of CSA proves to be advantageous and its delay reduces when compared to other adders. CSA is offering less delay due to improved routing, whereas for 16-bit operands, CSA is advantageous in logic as well as routing.

IV.ARRAY MULTIPLIER.

An array multiplier is a digital combinational circuit used for the multiplication process where it deploys add and shift algorithms. Basically array multiplier forms an array-like structure that includes Full Adder (FA) and Half Adder (HA). The block diagram of the array multiplier is shown in Fig.6.

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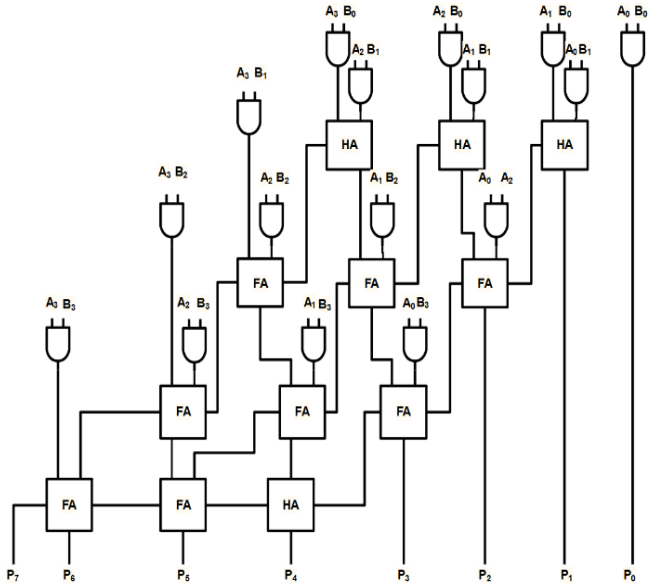

Fig.6 Block diagram of 4×4 Array Multiplier.

In the partial product generation stage, the partial products are generated for the required 4-bit numbers. In this multiplier, the partial products are generated using the AND gates. Fundamentally, each bit of the multiplier B is ANDed with each bit of the multiplicand A, i.e., if any one of the input is logic 0 then the output is logic 0 and it produces logic 1 output only if both the inputs are said to be logic 1. Using this principle, the partial products are generated and it requires (A×B) AND gates.

Once the partial products are reduced, the final addition process is carried out to produce the product terms. The final addition process is carried out with the reduced product terms obtained in step 2. Here, based on the output requirement the final parallel adder is chosen. For 4-bit multiplication 8- bit parallel adder is used to increase the speed of the operation. In this multiplier, all the stages are sequentially executed and the addition process is parallel performed to produce the final product term output.

Array Multiplier requires more area, which consumes the more power. It is one of the major drawbacks of array multiplier. Because number of bits are increases partial product increases, it implies that complexity is more, delay increases, power dissipation also increases. This is main drawback of array multiplier. It consists of array of and gates and adders in iterative structure and it does not require logic registers. This is also known as non additive multiplier, since it does not add an additional operand to the result of multiplication. If the number of bits increases the number of adders and AND gates components also increases, which may result increases the power consumption, occupies more area, take more time. Hence suitable for only less than 16-bit. One of the major drawback is delay of Braun multiplier is dependent on the delay of the full adder cell and also a final adder in the last row.

Table.2 Comparative analysis of 4*4 Array Multiplier

Type of Adder	**Parameter**	**CMOS**	**GDI**
Array Multiplier	Total power dissipation	4.22 mW	3.57mW
	Propagation delay	270ps	98.99ns
	TransistorCount	392	144

By integrating this AM-CSA to design an FIR filter is utilize the lesser hardware resources while minimizing the power of the overall design. This digital FIR filter is applicable for higher order filters and requires a minimum amount of hardware resources, so that the realization of FIR filters have improved for real time systems.

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Due to the less hardware utilization of AM and less latency of the carry skip adder, these are integrated in the FIR filter to achieve less utilization of resources. This integration is used to minimize the memory storage. It is considered as the key factors in the selection of digital FIR filters.

The proposed Array Multiplier and Carry Skip Adder has been implemented using 4GB RAM with 3.30 GHz, and a 500GB hard disk. The proposed algorithm used Modelsim SE-64 10.6d software to simulate the waveform to verify the timing diagram. Verilog language has been used to write the coding for each module.

Due to the less hardware utilization of AM and less latency of the carry skip adder, these modules can be integrated in the FIR filter to achieve less utilization of resources. This integration can be used to minimize the memory storage.It is considered as the key factors in selecting the digital FIR filters. Here the logical elements are reduced by replacing the multipliers and adders which is present in the FIR filter. Here, the multiplier is replaced by the Array multiplier and the adder is replaced by the Carry Skip Adder.

V.SIMULATION RESULTS

The CSA and AM discussed above has been implemented and simulated using ModelSim SE-64 10.6d in Verilog language.The simulation result is shown in fig.7 and fig.8.

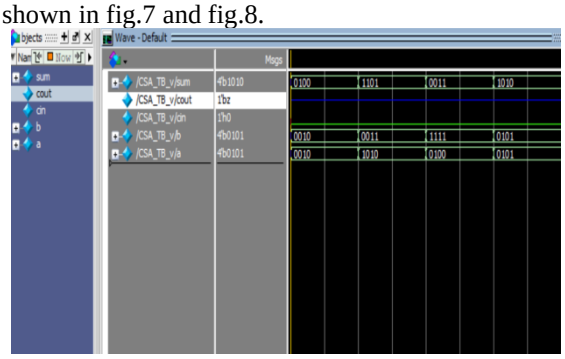

Fig.7 Output waveform of 4-bit CSA

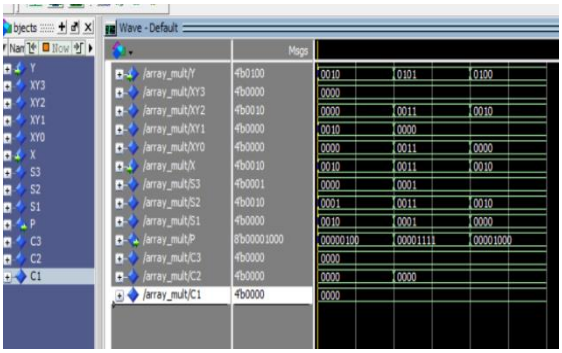

Fig.8 Output waveform of 4-bit AM.

FIR filter has been designed implemented in verilog code .Simulation result is shown in Fig.9

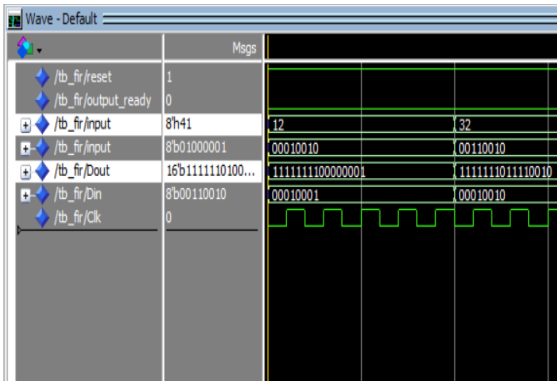

Fig.10 Output waveform of FIR filter

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VI.CONCLUSION

An innovative integration methodology forimproving the filtering process with minimum hardware utilization and improved linearity performance using Carry Skip Adder and ArrayMultiplier has been proposed in this paper. For this studied and evaluated different types adders andmultipliers used in filter design. A 4-bit Array Multiplier and Carry Skip Adder has been implemented and simulated using ModelSim SE-64 10.6d simulator. Also simulated an FIR filter using this multiplier and adde .Verilog language has been used to write the code for FPGA module.The proposed design becomes a promising filter design in the DSP applications with improved filtering options, speed and reduced area, power and delay.

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