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Performance Analysis of Power Gating designs in Low Power VLSI Circuits

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Abstract: The growing market for battery- powered mobile electronic systems (e.g., cellular phones, personal digital assistants, etc.) requires the design of micro-electronic circuits with low power dissipation. As the density and complexity of chips continue to increase, the challenge of dissipating power could limit the functionality of computer systems. Especially the nonometer level. Power dissipation uses approximately 35% of the power of the chip. The purpose of this project is to analyze the performance of one of the most reliable approaches to low power design called "Power Gating". The emphasis is only on nanoscale CMOS devices, as this technology is the most widely adopted in current VLSI systems.

I. INTRODUCTION

The optimal design and implementation of sleep transistors is crucial for a successful power synchronisation design. Particular considerations apply to the conception of sleep transistors. Few of them are sleep transistor door length, width and optimizing body polarization for area, leakage and efficiency. When synchronizing power, standby transistors are used as switches to cut power to parts of a standby design. The header switch is implemented by the PMOS to monitor the supply of Vdd. The PMOS transistor has fewer leaks compared to the NMOS transistor of the same size. The disadvantage of the header switch is that PMOS has lower drive current than NMOS of the same size. As a consequence, a header switch implementation typically consumes more surface than a footer switch implementation. The footer is operated by the NMOS transistor to control the VSS power supply. The advantage of the foot switch is the high drive and hence a smaller area. However, NMOS, PMOS and sleep transistors become more sensitive to floor noise. Figures 1 and 2 give an example of a sleep transistor and a network of distributed sleep transistors.

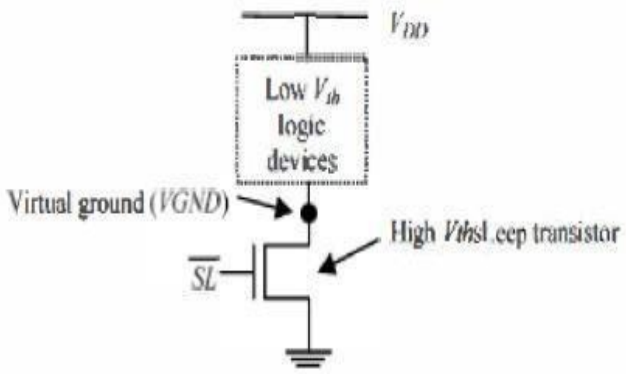

Figure 1: A Power Gating Structure.

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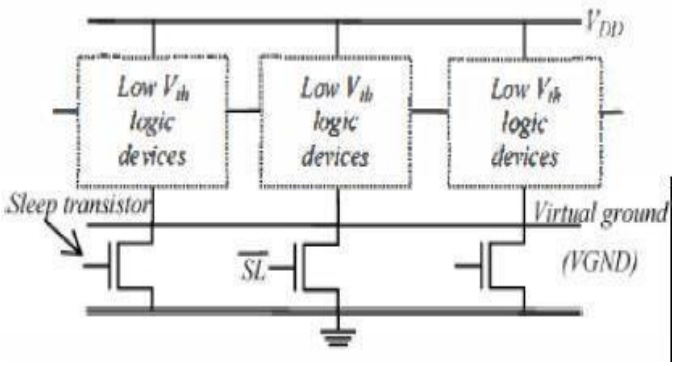

Figure 2: A DSTN Strucutre

When implementing sleeper transistors in CMOS circuits, performance is better when they are interconnected to form a network. There is much such architecture whose most notable structure is the distributed sleep transistor network (DSTN). a network of sleep gateways distributed within a cluster are connected to the sleep transistor through virtual grounding threads. The. where the sleep transistor is connected to logical gates is referred to as tapping point. By adding more threads to form a mesh containing all the virtual earthing threads, we get the DSTN structure. Because of leak- reduction techniques, the power-release technique has become one of the most effective methods. nanoscale, sleep transistor programming plays a vital role in reducing circuit leakage power. Here a new scheduling method for the sleep transistors has been designed and I have attempted to compare the performance of various power gating designs at 65nm scale by implementing the design on conventional 4-bit BCD adder.

II. CONVENTIONAL CMOS 4- BIT BCD ADDER

BCD is a binary-encoded decimal. This is another method used to represent decimals in the digital circuitry. Because all digital circuits must display the results digitally, this circuit is unavoidable in any digital circuit. In BCD, many types of codes are used for conversion; but the 8 - 4 - 2 - lis the most common code.

8 - 4 - 2 - 1 code indicates the weight of each bit in the following order:

23 - 22 - 21 - 2°.

For example, consider the decimal number: 9342. This value can be converted into binary shape using 8-4-2-1 BCD as follows:

9342 = 1001 0011 0100 0010
9 3 4 2

To implement a 4-bit BCD adder, two 4-bits are required. Full adders, one to add two 4bit BCD numbers and the other. Full adder to add the complement of 2 results greater than 9. at the result if carry is generated. Also we need 2 AND gates and a OR gate to generate the portage signal.

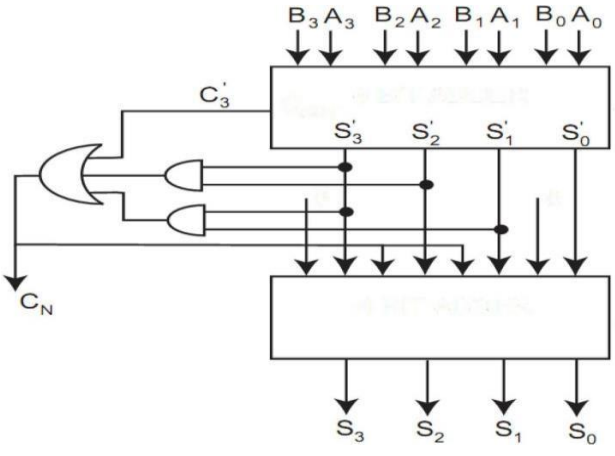

Figure 3: A 4 bit BCD adder.

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The scheme of a 4-bit BCD CMOS addendum designed using. HCSD 3.1 is shown in Figure 4.

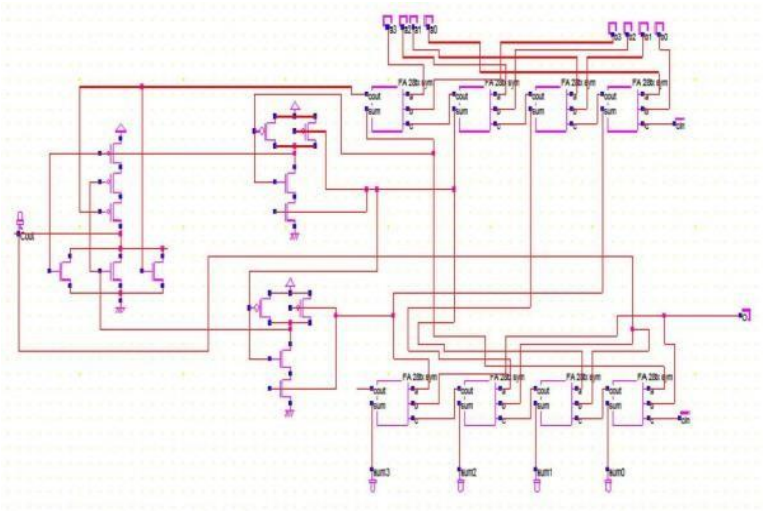

Figure 4: Schematic of 4 bit BCD adder

III. POWER GATED 4-BIT BCD ADDER DESIGN

A. 4-BIT BCD Adder Power Gated With DSTN

In a network of distributed sleep transistors, the doors of a group are linked to the sleep transistor by virtual earth wires. The location where the sleep transistor is connected to the logical doors is called the tapping point. By adding more leads to form a mesh containing all the virtual grounding leads, we get the DSTN structure. When designing the DSTN for the BCD adder, two sleep transistors are placed for each complete circuitry. One for the total circuit and one for the portage circuit. The sleep transistor within each complete adder forms one cluster. The sleep transistors present in each beam are connected across a single line that is called "Virtual Ground". The virtual earth line is energized through an external sleep signal. The diagram of the BCD adder designed with the DSTN power synchronisation structure is shown in the figure

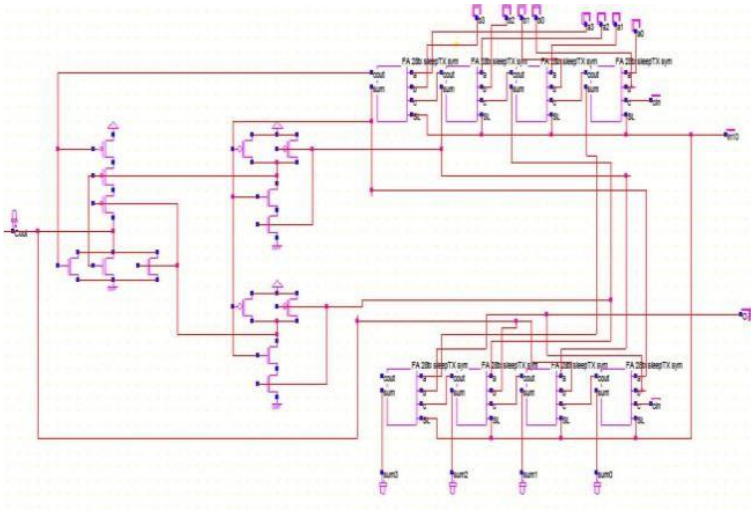

Figure 5: Bit BCD adder power gated with DSTN.

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B. 4-BIT BCD Adder With Clock Gated Power Gating

In the synchronous power synchronization structure, an internal clock signal is used to excite standby transistors in the BCD circuit. The clock frequency depends in part on the mean delay that occurs in the circuit. The clock speed is predetermined as a function of the propagation speed of the intermediate results between the logical clusters in the circuit. The diagram of the BCD addendum with synchronized power synchronisation is given in Figure 6. These circuits are designed to a 65nm scale. The sleep transistors used are designed for a higher WIL ratio than those used in the BCD adder

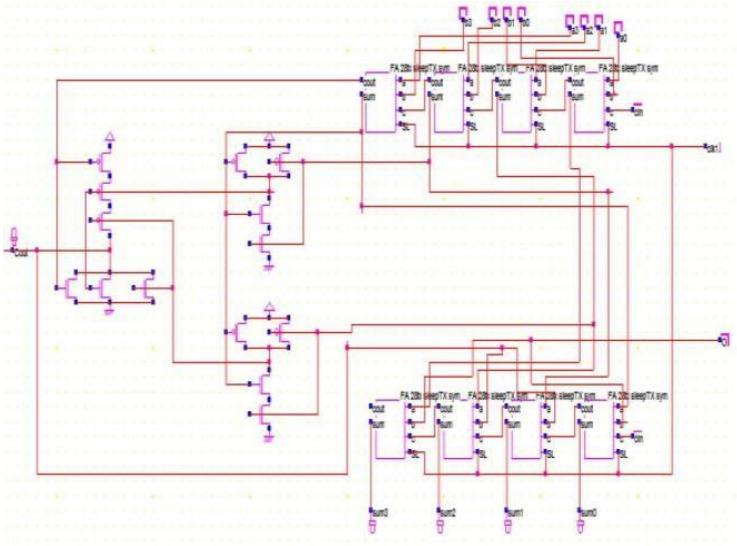

Figure 6: 4-bit bcd adder with clock gated power gating

IV. SIMULATION RESULTS

In this section I've described the simulation results. generated by using DSCH3.l. First, let's take it. output for the scheme designed using DSCH 3.l. Then we convert the scheme into layout using the network list and.Develop the design of the development. The layout for us. obtain different circuit characteristics such as V-I. characteristics. Diagram 7 shows the exit from.

BCD traditional adder and 8 displays the output of the. Proposed Power Synchronized BCD Adders.

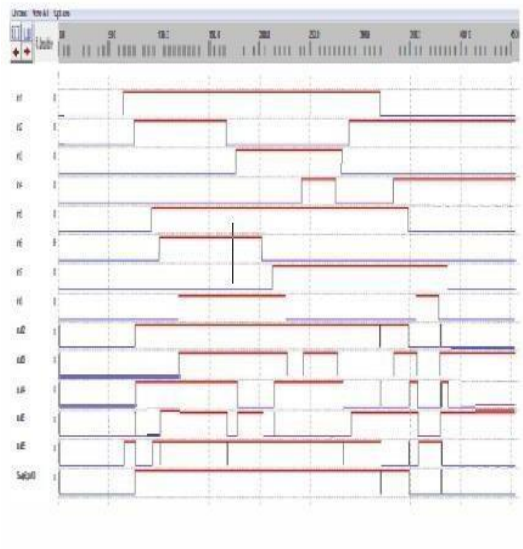

Figure 7: Output of conventionl CMOS 4- bit BCD adder.

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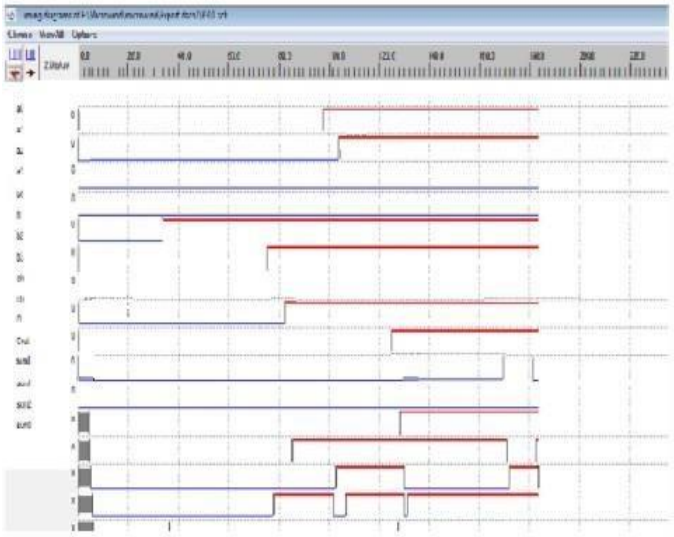

Figure 8: Output of power gated 4-bit BCD adder.

V. VI CHARACTERISTICS

The V-I features of the circuits designed above. Are produced using the Microwind layout tool. It appears that. the frequency of the voltage surge is reduced to a maximum. The range when we use power synchronization structures. The VI feature of a 4-bit BCD CMOS adder is shown in the figure 9. The Figures 10 and 11 show the VI characteristics of the circuitry implemented with DSTN and Clock Gated. Structures respectively.

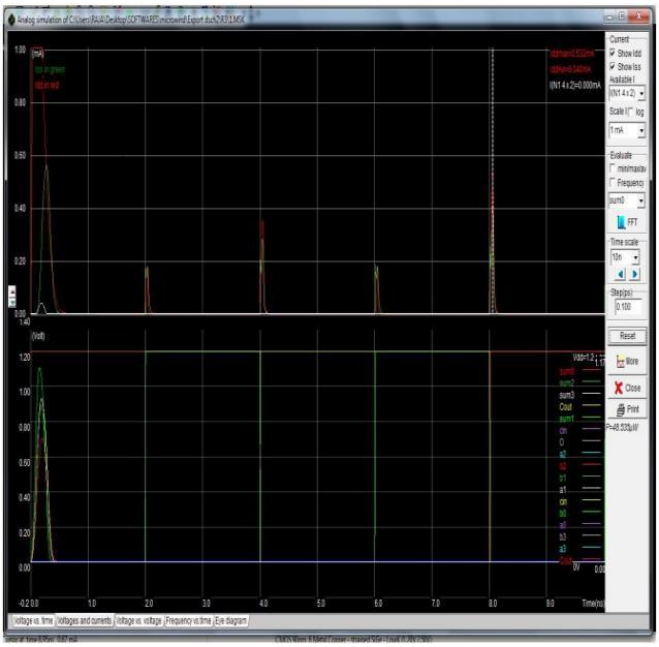

Figure 9: Chaeactertistics of conventional 4-bit BCD adder

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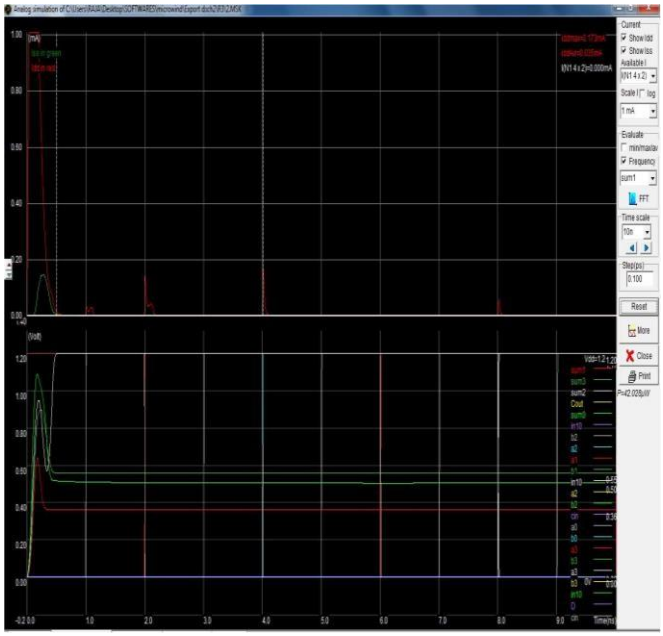

Figure 10: VI characteristics of 4-bit BCD adder power gated With DSTN.

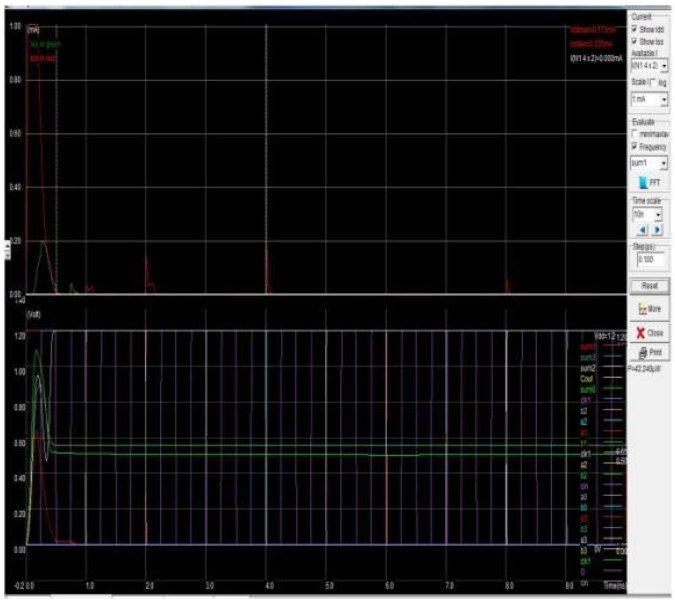

Figure 11: VI characteristics of 4-bit BCD adder with clock gated Power gating.

In the graphs above, the voltage is shown below and the current values are shown at the top of the graph.

VI. PERFORMANCE ANALYSIS

A. Power Analysis

Based on the values of the drain current and voltage in the circuit, the power consumed by each circuit is computed and listed in Table 1. The power consumption of the synchronized circuit is below that of the normal circuit. In addition, it is found that the timed synchronized power synchronization design works better than the DSTN design. The power consumed (in mW) per circuit.

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S. No	Time (ns)	Power Consumed(in µW)		
		Conventional BCD adder	*BCD adder (DSTN)*	*BCD adder (Clk gated)*
1	0.1	0.514	0.5292	0.529
2	0.2	0.6625	0.55592	0.5559
3	0.3	0.1624	0.0986	0.0864
4	0.4	0.00312	0.0311	0.01071
5	0.5	0.0371	0.00441	0.000234
6	6	0.00265	0.000856	0.000051

Table l: Power consumed conventional multiple adder power gating.

A graphic is drawn with the above values. They provide a comparison of the performance of the power gated circuits atscale. The average consumption of each circuit is also indicated. The design performance of the synchronized clock is considered optimal and it functions better than DSTN.

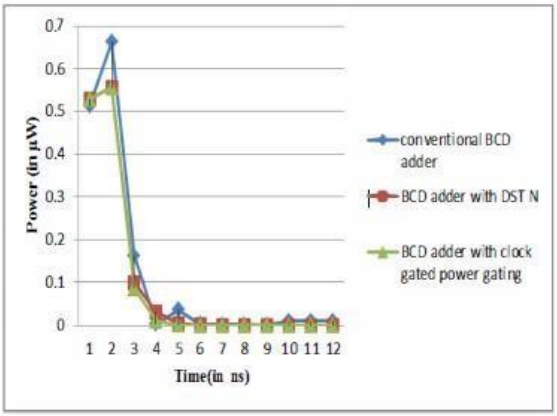

Figure 12: Power Consumed by conventional 4- bit BCD Adder, BCD adder with DSTN & Clock gated 4- Bit BCD adder.

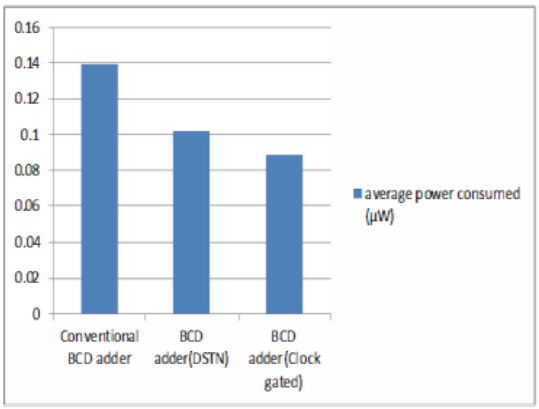

Figure 13: Average power consumption.

B. Delay Analysis

The Delay Analysis is performed to calculate the delay occurring on the circuits designed above. This allows us to determine the time range for sleep transistor excitation. The results from the late analysis are presented below.at different times is calculated.

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S No	Circuit	Delay (in ps)	Power Delay Product(μJ)
1	Conventional BCD adder	82.50	11.846
2	BCD adder(DSTN)	77.15	7.846
3	BCD adder(Clock gated)	72.36	6.138

Table 2: Comparison of Delay and Power delay product of conventional BCD adder, BCD Adder with Clock gated power gating

VII. CONCLUSION

The sleep transistor is designed at the 65 nm scale and implemented in power synchronisation designs. The power sync concepts discussed in this project are DSTN sync and Clock. The sleep transistors in each cluster is connected by means of daisy chain implementation which provides enough time for the results to propagate from one cluster to the other, thus synchronizing the circuit operation with triggering of sleep transistors.

The clock synchronization method is introduced into the power synchronization design, which provides additional control on the excitation process of sleep transistors. Finally, the performances of the DSTN and Clock Gating are compared in terms of circuit energy consumption and overvoltage current. According to the results, the power synchronization design is more efficient than DSTN circuits designed at the 65 nm scale.

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