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DESIGN AND ANALYSIS OF WALLACE TREE MULTIPLIER USING APPROXIMATE FULL ADDER AND KOGGE STONE ADDER

V.Thamizharasan[1], P. Pavithra[2]

Assistant professor, Department of ECE, Erode Sengunthar Engineering college, Perunthurai, Erode[1]

M.E - Applied Electronics, Erode Sengunthar Engineering College, Perunthurai, Erode[2]

Abstract: To achieve a very fast digital devices with reduced power usage is an important for the VLSI circuit designers and manufacturers. For the most part of the digital circuit design carried out using the multiplier, where it is used more power consuming component in the electronic circuit design. The multiplication operation has been carried out by the process of shift and add method. Due to the improvement among various adders, which the way for the increase in execution rate of the multipliers. Parallel multiplication algorithms are used in the combinational circuits. And don't contain feedback structures. The circuit is developed by VHDL and functions were validated based on the simulations obtained utilizing Xilinx. In this project, the enhancement in WTM using the KSA and the Modified Approximate Full Adder concepts is done.

I. INTRODUCTION

Arithmetic and logic unit are the most important unit in any electronic devices. In the recent creation, for an arithmetic and logic unit needs to have an effective algorithmic operation such as Multiplications and addition. Multipliers are a supreme unit in the digital world. It will take the important role in the applications of digital signal processing and image processing. If we design a multiplier the multiplier should be effective and efficient in terms of multiplier performance. The multiplier needs high speed or low power or to be a time effective. To decrease computation time we want to reduce the delay. Area and delay are the two major restriction in the digital designs. This overall project must be made for an efficient multiplier.

Multipliers are one the most important component in the many systems. In high speed digital signal processing (DSP) and image processing multiplier plays a very important role. In image processing fast Fourier transform (FFT) is one of the most important transform in the multiplication . A Fast Fourier transform requires large number of multiplication and addition operation. The execution of these algorithms requires MAC and Arithmetic Logic Unit (ALU). Multipliers and adders are the key aspects of these arithmetic units . In the advance technology, many developers have tried to implement increase the efficient multiplier. They focus on designing low power consumption, high speed and reduced delay. Multiplication plays an important role in the signal processing algorithms.

Multipliers are occupies the large area, long latency and utilize the high power. In VLSI system design low power multiplier plays an important role . There are three major steps in the multiplication process partial product (PPG) generation, partial product grouping & reduction, and final addition. A system's performance is considered by the performance of the multiplier because the multiplier is the slowest element in the system. And the multiplication are generally most area consuming. As a result, a whole project of multipliers with different area- speed constraints has been designed with fully parallel. To increase the speed we use Wallace tree multiplier . The Wallace tree multiplier is a one of the high speed multiplier. The addition of the partial product bits in parallel using a tree of carry-save adders became generally called as the "Wallace Tree"

II. WALLACE TREE MULTIPLICATION

2.1 WALLACE TREE MULTIPLIER

WTM is considered as one of the effective fast multipliers. Wallace multiplier considered of three stages namely:

1. PPG
2. PPR
3.Addition at last stage.

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And in the Partial Product Reduction it consists a 15-4 compressor which is include modified full adders and 5-3 compressor and KSA (Kogge stone Adder). In the last stage addition where the delay shows a important role, to reduce delay parameter KSA has been used. KSA is one type of the fast-parallel adders used in computation for the reduction in delay from the expect output.

2.2 MULTIPLIER BASED ON WALLACE TREE

Multiplier has become the most significant portion of the digital circuits which carries the majority of operation at system level. It is a circuit utilized in digital electronics, kind of a computer, to multiply two binary numbers. Binary adders are used construct a multiplier. An effective multiplier ought to have the subsequent features:

1) Accuracy: An efficient multiplier have got to produce proper results.
2) Speed: Multiplier must achieve operations at tremendous speed.
3) Area: A multiplier must cover a lesser amount of slices and LUTs.
4) Power: Multiplier ought to use minimum power.

A WTM is an effective hardware which makes use of electronic circuit that products numbers. In this design, a Wallace tree multiplier since it has the advantages of superior processing speed and minimal power utilization. There are three stages for a multiplication process usually occurs are:

1) Generation of Intermediate partial products
2) Reduction of them
3) Addition at the end.

2.3 16x16 WTM UTILIZING 15-4 COMPRESSOR

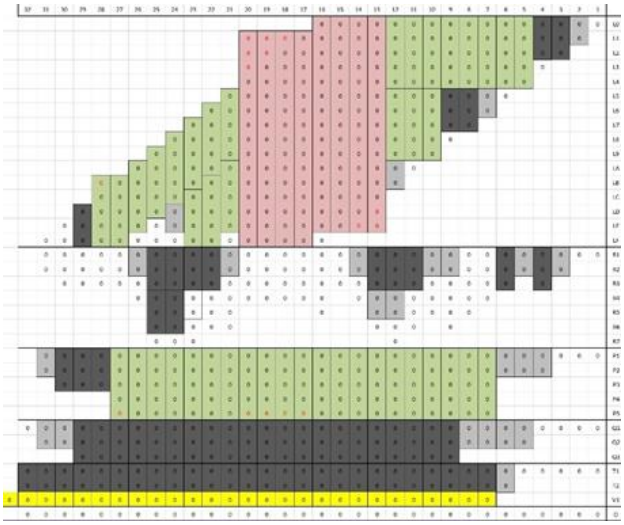

Fig. 2.1 Configuration of 16X16 Multiplier utilizing 15-4 Compressor

Fig.3.1 describes the Configuration or Structure of 16-bit WTM using 15-4 compressor and modified approximate full adder. In this model, every dot denotes a partial product. Between the column numbers 13 to column number 20, a 15-4 compressor is employed and there 13 partial products and two zero are included in the 13th column in order to have 15 inputs for the compressor to perform. By the same way, a zero is added. Column number 13th to 20th needs to be performed using approximate compressor. Various half adder are involved in the second stage of the multiplier, modified approximate full adders and 5:3 compressors. For every individual bit, it is brought down to successive stages of column without any chance of additional actions. Till only two rows stay, the method of reduction is persisted.

2.4 VARIOUS STAGES IN WALLACE TREE MULTIPLIER

Numbers are binary integers, It is “long hand” multiplication Products (each in blue square) are the result of simple AND gate. All products are done simultaneously. Requires N square AND gates. To add up the columns, add up three rows at a time. The result for each three row is a set of two rows. Every two row results are considered as the sum and carryout

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of the two set of the rows . Odd rows are left alone. repeat the process. There are two set of three rows result is two set of two rows. Gray boxes express the summation bits have been moved down to the carry out . Repeat the process This time, there is only one set of three rows, plus an extra row to carry down. Consider the result is three rows, two from the set of three addition the one from the carried down. All adders are done in parallel. Repeat the process one last time. Remaining three rows become two rows. In this example, stage 2 had 4 step and four full adder delays. The five LSBs have already calculated. Final Addition, Final result is calculated by adding the final two rows. An efficiant high speed Wallace tree multiplier architecture has the advantage of reduced latency which causes 44.4% higher speed and 11% reduced power consumption than the conventional Wallace multiplier.

Wallace tree multiplier use the full adders and half adders to reduce the partial product of the two rows, and then a finally the adder is used to add the last final two rows of partial products.

III. 15-4 COMPRESSOR

Compactors or compressor are merely used as an adding circuit. This compressor has fifteen inputs (C0 - C14) and it delivers four outputs (B0 – B3). The compressor has 5 modified approximate full adders at the initial phase, 2 5-3 compressors in the secondary phase and the last phase has a KSA. Sum and Carry is generated out of the given inputs. One of the two 5-3 compressors obtains the sum bits of all the modified approximate full adders . Likewise, the other compressor obtains the carry bits of all the modified approximate full adders. A compressor adder delivers lowered delay on standard adders applying all the half adders with modified approximate full adders . Yields of intermediate compressors provided as input for the KSA. With the use of KSA at last stage the output is obtained. Compressors are used in the reduction of quantity of gates also the amount delay when compared to the other adders . The Approximate compressor of 15-4 involves three segments. 1st segment consists of the modified approximate 3 input full adders, where as 2nd segment consists of two 5-3 compressors and 3rd segment the 4-bit KSA.

The design of 15:4 compressor has five full adders at first stage, two 5:3 compressors in second stage and parallel adder at final stage. Design of 5:3 compressor is implemented in 15:4 compressor which will result increased speed and reduced power consumption. The outputs will be verified by using the outputs of full adders in the 15:4 compressor, 5:3 compressors and the 4 bit parallel adder.

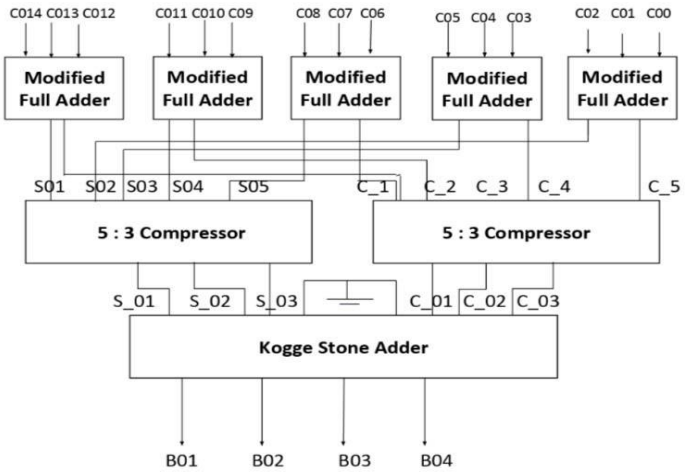

Fig. 3.1 15-4 Compressor using Modified Approximate Full Adder

3.1 MODIFIED APPROXIMATE FULL ADDER

Modified approximate full adders are used in the initial stages of the entire process. There are five number of modified approximate full adders in the multiplier design. This is used the regular full adders to reduce the counts of the gates in the approximation concept. The modified approximate full adder uses only one OR gate, one EX-OR gate and one AND gate in total to obtain the desired function of a full adder thereby reducing the number of gate counts and other parameters like power and area. These modified approximate full adders after its functioning it gives five equivalent sum outputs and five equivalent carry outputs.

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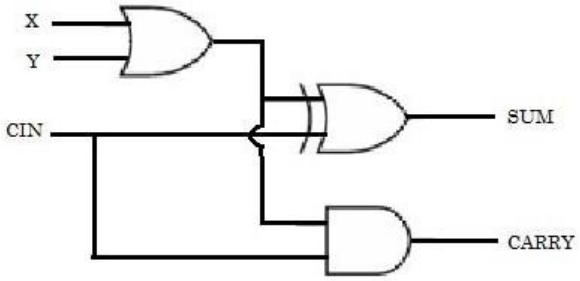

Fig. 3.2 Logical structure of 3 input Approximate Full Adder

3.2 5:3 COMPRESSOR CIRCUIT

A 5:3 compressor comprises with a combinational logic circuit having 5 inputs and 3 outputs. It accepts a5 bit input string as input, and produces its sum as output. The conventional architecture of a 5:3 compressor is based on the extended design of a conventional 4:2 compressor.

15-4 compressor or compactor is made up of two 5-3 compressors in order to obtain 3 respective compressed outputs . The 5-3 compressor applies 5 initial inputs such as S01, S02, S03, S04, S05 and produces three outputs namely S_01, S_02 and S_03. In the same way, another 5-3 compressor is used to obtain the results from carry inputs namely C_1, C_2, C_3, C_4 and C_5. Yield at compressor is being determined by the number of 1's in the place of the input and further implemented by the property of counter.

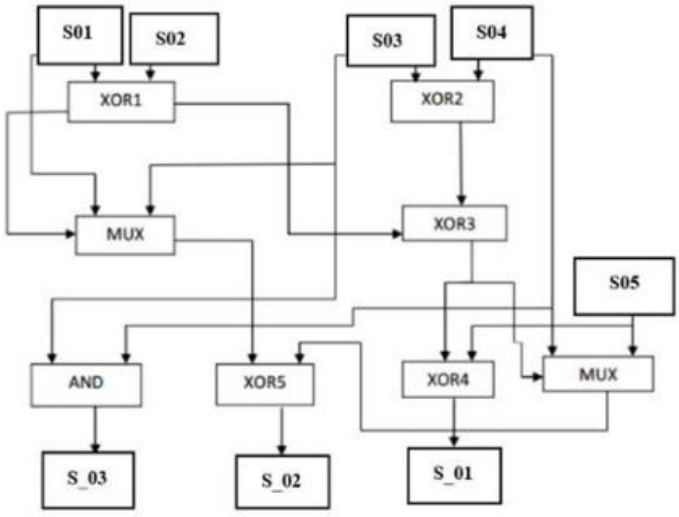

Fig. 3.3 Block Diagram of 5-3 Compressor

3.3 KOGGE STONE ADDER

The KSA is one of the well known parallel prefix adder. KSA is found to be the fastest interms of addition in design perspective . The KSA acquires extra area when compared to Brent–Kung adder, but KSA has lesser fan-outs at each phase, which rises execution. In this design, a 4-bit KSA is used. These type of Adders are mostly categorized in 3 types.

A. Pre- processing stage
B. Carry Generation section
C. Final processing or Post processing.

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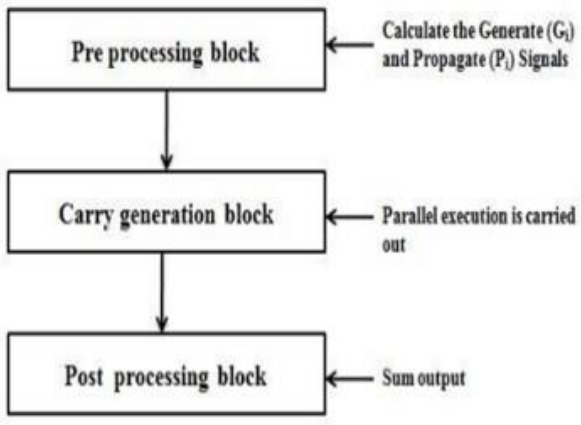

Fig. 3.4 Functions of Basic KSA

3.3.1 Pre processing

This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

pi = Ai xor Bi (1)

gi = Ai and Bi (2)

3.3.2 Carry look ahead network

The block differentiates Kogge Stone Adder from the other adders and its mainly used in high performance.

The steps are involves computation of carries in the each corresponding bits . This method use the group propagate and generate in the intermediate signals which are given by the logic method given below:

Pi:j = Pi:k+1 and Pk:j (3)

Gi:j = Gi:k+1 or (Pi:k+1 and Gk:j) (4)

3.3.3 Post processing

Post processing is the final step and is common to all adders of this family (carry look ahead). It includes the computation of sum of the every bits. Sum of the bits are computed by the logic given below :

Si = pi xor Ci-1 (5)

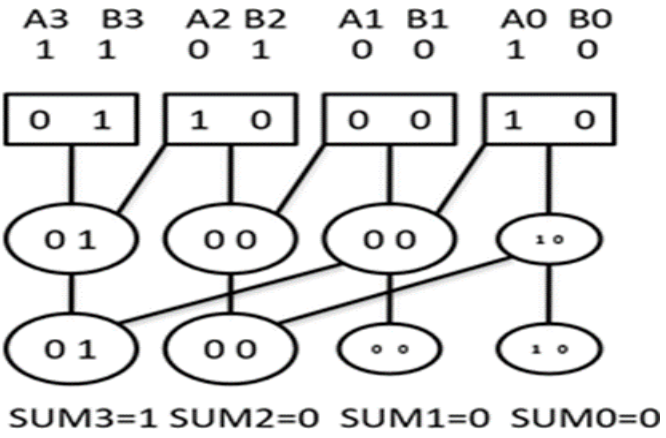

Fig. 3.5 Block Representation of KSA

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IV. RESULT AND DISCUSSION

4.1 SOFTWARE OUTPUT

The model of 16×16 bit WTM used the above compressor is developed with VHDL, using the software Xilinx ISE 14.7. Simulation outputs shows the structural pattern of WTM as shown in Fig. 4.1 in this analyse Area and Power parameters are observed, and the outputs are plotted.

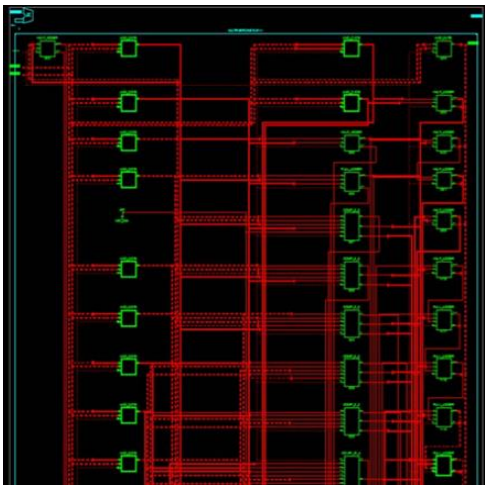

Fig. 4.1 Register Transfer Level View of KSA

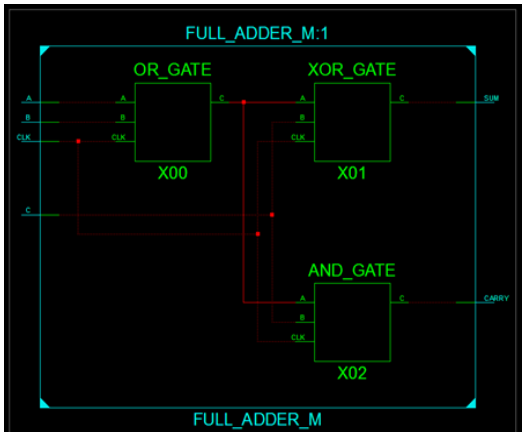

Fig. 4.2 Structural Design of 16x16 Bit WTM

4.2 TABULATION OUTPUT

Table I and II explains the power parameters and area consumption of a 16-bit WTM. It gives the clear results than more types of adder at a distance from that it provides fewer area.

TABLE 4.1 Power Analysis of 16x16 Bit WTM

On Chip	Power(W)
Clocks	0.016
Logic	0.002
Signals	0.002
IOs	0.003
Leakage	0.014
Total	0.037

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TABLE 4.2 Device Utilization of 16x16 Bit WTM

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of slice registers	1332	4800	27%
Number used as flip flops	18		
Number used as latches	1314		
Number used as latch-thrus	0		
Number used as AND/OR logics	0		
Number of slice LUTs	1158	2400	48%
Number used as logic	1148	2400	47%

The Approximate 16x16 multiplier which consists of 15-4 compressor has been comparatively analysed among existing adders at the last stage as an alternative of KSA. The distinguishing results in reference to the number of LUTs occupied with its power are calculated and listed in Table 4.2.

TABLE 4.3 Design And Analysis of Different Multipliers

S.NO	Categories of Multiplier	LUTs Used	Power (mW)
1	16×16 - bit multiplier with the use of accurate15-4 compressor	5066	56
2	16×16 - bit WTM utilizing 15-4 compressor with KSA	1570	42
3	16×16 - bit multiplier using modified approximate full adder (proposed)	1332	37

The Approximate 16x16 multiplier which consists of 15-4 compressor has been comparatively analysed among existing adders at the last stage as an alternative of KSA. The distinguishing results in reference to the number of LUTs occupied with its power are calculated and listed in Table 4.2.

In this table we can analyse the different type of the multiplier using in the Wallace tree design 16x16 multiplier with the use of the 5-4 compressor this gives the power value in the 56mw and the same 16x16 multiplier use the 15-3 compressor with the use of the kogge stone adder it gives the 42mw . Then the third combination same 16x16 multiplier using modified approximate full adder it gives the results on 37mw.These are values are calculated by using the look up Table

V. CONCLUSION

The 16x16 – bit WTM is designed using the KSA andmodified approximate Full adder and synthesized using the software Xilinx ISE 14.7. The profound multiplier architectureusing KSA is distinguished based on the analysis of performance with the multiplier architecture composed of modified approximate full adder. With the forthcomingtechnologies in future, the profound Multiplier may be enhanced and can be employed at various places such as image processing, video conferencing and DSP.

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