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Harmonic Compensation in Distribution System Using Four Pole Based Three-Phase Four-Wire Shunt Active Filter

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Abstract: Shunt Active power filters have been proved as useful elements to correct distorted currents caused by non-linear loads in power distribution systems. This paper deals with a Novel Adaptive Hysteresis Band Current Controller, a new control scheme for an Shunt Active Power Filter (APF) to reduce harmonics and to compensate the reactive power of three-phase rectifier. The switching dynamics of a voltage source inverter (VSI) Four pole based three-phase, four-wire shunt APF system with adaptive hysteresis band current control has been studied and verified by simulation. The simulation results of Active Power Filter (APF) control technique, carried out in MATLAB environment, are presented in this paper and are quite satisfactory to reduce harmonics and reactive power components from utility current.

Index terms: Active Power Filter (APF), d-q-0 reference frame, and adaptive hysteresis band current controller.

I. INTRODUCTION

Three-phase four-wire (3P4W) electric power supply systems are considered as one of the most vulnerable systems for multiple power quality problems. The 3P4W system can be viewed as a combination of three-phase three-wire and single-phase two wire systems. The 3P4W system possess neutral current problem in addition to load current harmonics, reactive power and unbalance[1-3]. The undesirable harmonics, reactive power and unbalanced currents may affect the performance of the electric power system by introducing harmonics and unbalance in the supply voltages. The unbalanced currents result in the presence of negative and zero sequence current components. These sequence currents may cause excessive heating in electric machines[4-7], undesirable operation of electronic equipment, neutral conductor heating, etc. However, the development of active power filters (APFs) has made it possible to compensate these power quality problems at a certain level. A variety of APF configurations are developed and successfully deployed to compensate different power quality problems in single-phase and three-phase systems [7-9]. This paper begins with the discussion on the 3P4W shunt APF system configuration under consideration. Next, the algorithm used is described to control the shunt APF[10]. Later on, an extensive simulation study is carried out both for steady state and dynamic conditions.

II. THREE-PHASE FOUR-WIRE SHUNT APF SYSTEM CONFIGURATION

To compensate load current related power quality problems associated with 3P4W system, several shunt APF configurations/topologies are used. The most popular among them is four pole or four- leg topology (4L). This configuration is realized using two-level voltage source inverter topology. [4-5]

The configuration for 3P4W shunt APF is given in Fig. 1. The utilization of additional pole/leg in typical three-phase three-wire system has given it a name of four-pole or four-leg (4L) topology. The fourth leg is solely added to compensate the load neutral current. A direct, and thus better, control over neutral current is assured due to the additional leg. In 4L topology, single DC bus capacitor and hence only one DC voltage sensor is enough. Additionally, the sensing of load neutral current is not required to generate the reference source side neutral current which necessarily should be zero. On the economical aspect, the cost involved due to addition of two extra switches and their corresponding control circuitries can be a disadvantage of 4L topology.

The minimum required DC bus voltage ($V_{dc|min}$) for 4L topology can be determined by the following mathematical relationship [1].

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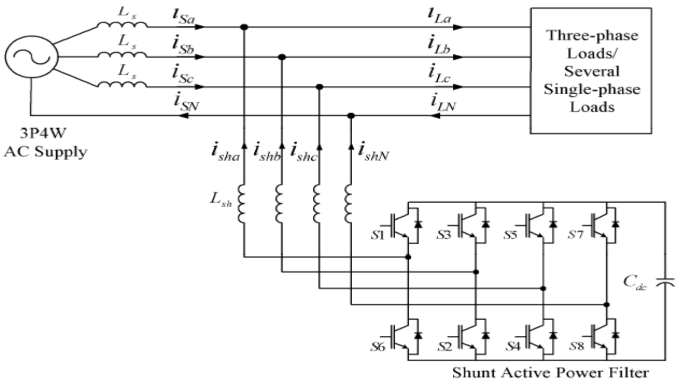


Fig.1 Four-leg(4L) based 3P4W shunt active power filter topology.

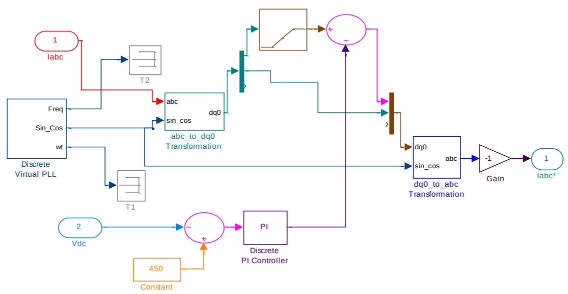
$V_{dc/min} = \sqrt{3} * \sqrt{2} * V_{S,\,rms} = 2.45 * V_{S,\,rms}$ (1)

Typically, a multiplying factor of 1.25 to 1.75 times the minimum required DC bus voltage is common

A Hysteresis rule based carrier less PWM current control technique [6] is used to realize desired currents in the three phases of the APF. The main objective of the APF is to compensate harmonics, reactive power, neutral current and unbalancing of non-linear loads locally such that ac mains supplies only unity power-factor sinusoidal balanced three-phase currents.

III. SYNCHRONOUS D-Q-0 REFERENCE FRAME BASED COMPENSATION

Synchronous d-q-0 reference frame based compensation algorithm is shown in Fig. 2. Here the three phase load currents are transformed to the synchronous reference frame (a-b-c to d-q-0 transformation). A high pass filter is used to extract the DC component representing the fundamental frequency of the currents. The coordinate transformation from three-phase load currents (i_{La}, i_{Lb}, i_{Lc}) to the synchronous reference frame based load currents (i_{Ld}, i_{Lq}, i_{Lo}) is obtained as follows:



$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{Lo} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ -\sin(\omega t) & -\sin(\omega t - 2\pi/3) & -\sin(\omega t + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (2)$$

Fig. 2 Synchronous d-q-0 reference frame based algorithm.

The d-axis current (i_{Ld}) is filtered out and applied to inverse transformation to remove DC component and to determine harmonic contents. The DC side voltage of APF should be controlled and kept at a constant value to maintain the normal operation of the inverter. Because there is energy loss due to conduction and switching power losses associated with the diodes and IGBTs of the inverter in APF, which tend to reduce the value of voltage across the dc capacitor V_{DC}. A feedback voltage control circuit needs to be incorporated into the inverter for this reason. An error signal is generated based on the difference between the reference value (V_{ref}) and the feedback value (V_{DC}). This error function first passes through a PI regulator and the output of the PI regulator is subtracted from the d-axis value of the harmonic current components. Reference filter currents (i^*_{abc}) are determined negatives of the outputs of the inverse transformation matrix (d-q-0 to a-b-c).

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IV. THE NOVEL ADAPTIVE HYSTERESIS CURRENT CONTROLLER

The APF comprises of three single phase VSI bridges isolated with unity turns ratio transformers [6] and connected to a common dc bus capacitor. The current controllers of the three-phases are designed to operate independently. Each current controller determines the switching signals to its VSI Bridge. The switching logic for 'phase-a' is formulated as:

If $i_{ca} < (i^*_{ca}$ - HB) upper switch is OFF and lower switch is ON in the left leg of 'phase-a' and SAL=0;

If $i_{ca} > (i^*_{ca}$ + HB) upper switch is ON and lower switch is OFF in the left leg of 'phase-a' and SAL=1.

The right leg devices of 'phase-a' bridge are switched in a complementary manner to left leg devices, i.e. SAL is the complement of SAR. In the same fashion, the switching of 'phase-b and c' devices is derived using HB the width of hysteresis band. The switching frequency of the hysteresis band current control method described above depends on how fast the current changes from the upper limit of the hysteresis band to the lower limit of the hysteresis band, or vice versa.

The hysteresis-band current control method is popularly used because of its simplicity of implementation, among the various PWM techniques. Besides fast-response current loop and inherent-peak current limiting capability, the technique does not need any information about system parameters

The Fig. 3 shows the PWM current and voltage waves for phase-a. When the actual line current of the active power filter tries to leave the hysteresis band, the suitable power transistor is switched to ON or OFF state to force the current to return to a value within the hysteresis band. Then the switching pattern will be trying to maintain the current inside the hysteresis band. The currents i_a tends to cross the lower hysteresis band at point 1, where upper side IGBT of leg "a" is switched on. The linearly rising current (i_a^+) then touches the upper hand at point 2**,** where the lower side IGBT of leg "a" is switched on.

The following equations can be written in the respective switching intervals t_1 and t_2 from Fig. 3.

$$\frac{di_a^+}{dt} = \frac{1}{L}(0.5V_{DC} - V_s) \quad (3)$$

$$\frac{di_a^-}{dt} = -\frac{1}{L}(0.5V_{DC} + V_s) \quad (4)$$

From the geometry of Fig. 3, we can write,

$$\frac{di_a^+}{dt}t_1 - \frac{di_{ca}^*}{dt}t_1 = 2HB \quad (5)$$

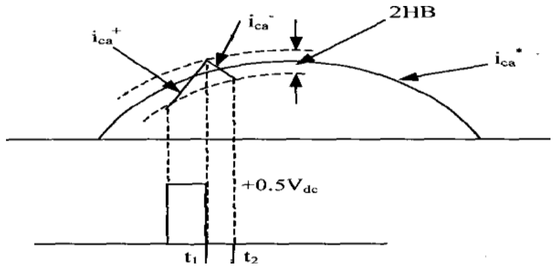

Fig. 3 Current and voltage waves with hysteresis band current control.

$$\frac{di_a^-}{dt}t_2 - \frac{di_{ca}^*}{dt}t_2 = -2HB \quad (6)$$

$$t_1 + t_2 = T_c = \frac{1}{f_c} \quad (7)$$

Where t_1 and t_2 are the respective switching intervals and f_c is the switching frequency. From the above equations we can get hysteresis band (HB) as [7],

$$HB = \left\{ \frac{0.125V_{DC}}{f_c L}\left[1 - \frac{4L^2}{V_{DC}^2}\left(\frac{v_s}{L} + m\right)^2\right]\right\} \quad (8)$$

Where f_c is modulation frequency, $m = di^*_{ca}/dt$ is the slope of command current wave.

V. SIMULATION RESULTS

The harmonic current and reactive power compensation by APF is implemented in a three-phase power system in which the utility power supply voltage of 127 V and current source three-phase diode-bridge rectifier with resistive load as the

Fig. 6: FFT Analysis without active filter

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harmonic current compensation object. The design specifications and the circuit parameters used in the simulation are indicated in Table I.

Table I. Design Specifications and Circuit Parameters

Switching frequency	12kHz
Fundamental frequency	60Hz
AC supply voltage	127 V
Inverter DC voltage (V_{dc})	450 V
Rectifier load resistance	5 ohm
Rectifier side inductance	1 mH
Inverter side inductance	1 mH
C_{DC} Capacitor	1500 µF

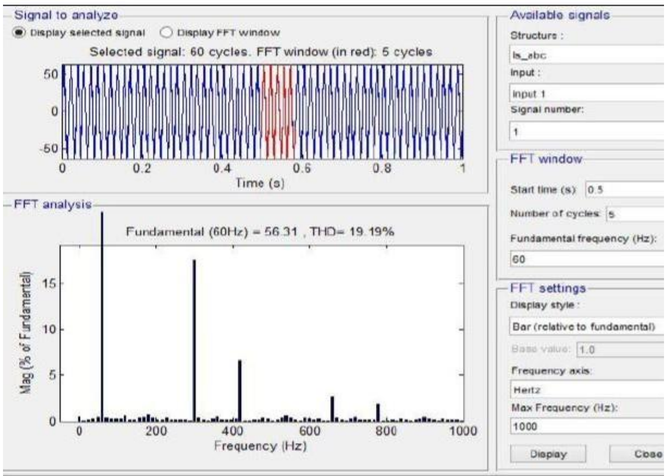
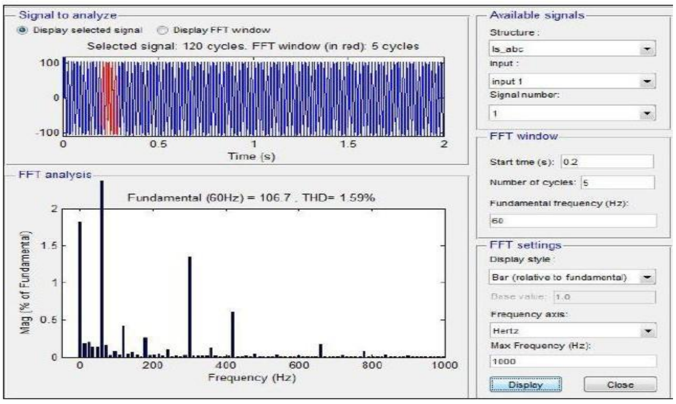


Fig. 7:FFT Analysis of 4LEG TOPLOGY

Table II. COMPARISION

Topology type	THD		
	Phase-a	Phase-b	Phase-c
No Compensation	19.19%	19.34%	18.54%
Four-Leg Topology	1.59%	1.57%	1.58%



The utility power source current after the harmonic compensation is illustrated in Fig. 7. The THD (Total Harmonic Distortion) is also computed in load current as well as in supply current. The THD is 19.19% before harmonic compensation in load current and 1.59% in supply current after harmonic current compensation that is within the limit of the harmonic standard of IEEE 519.

CONCLUSIONS

The 4Leg APF topology analyzed in this paper for the compensation of harmonic current components in non-linear load was effective for harmonic isolation and keeping the utility supply line current sinusoidal. The validity of this technique in order to compensate current harmonics was proved on the basis of simulation results. The APF is found effective to meet IEEE 519 standard recommendations on harmonics levels. The 4L topology is a promising candidate for the low to medium power applications.

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BIOGRAPHIES

Jagadish Kumar SINGARAPU was born in India, 1980. He received the B.E. degree from OSMANIA UNIVERSITY Hyderabad, India in 2003, the M.Tech.degree from JNTUH College of Engineering, Hyderabad, India in 2008, and is currently Assistant professor in the Electrical Engineering Department, JNTU JAGITIYAL and pursuing Ph.D. degree at the JNTU, Hyderabad, India. His area of interest includes power electronics, Power system protection and Power Quality.

Narsaiah Srinivas GONDLALA was born in India, 1973.He received the B.Tech. degree from JNTU College of Engineering, Hyderabad, India in 1995,the M.E. degree from Osmania University, Hyderabad, India. in 2001, and the Ph.D. degree in Electrical Engineering from JNTU, Hyderabad, India in 2009.He has teaching and research experiences of about 25years, published/presented more than 20 papers at National &International levels. Chaired technical sessions at National & International Conferences. Currently, he is a Professor in the Electrical Engineering Department, JNTU Hyderabad. His research interest includes power system, power quality and distribution system reliability evaluation.