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Different Phase Locked Loop: A Review

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Abstract: Rapid penetration of renewable energy sources connected to the grid and distribution systems with power electronic circuits have changed the expected grid requirements to guarantee an appropriate performance under grid faults. This paper presents the analysis of SRF PLL for distorted grid conditions. An exact detection of phase and fundamental frequency of grid current is essential for the control algorithm of grid connected power converter circuit. A control model of the SRF PLL is developed and is made on tuning the system under distorted grid conditions like harmonics and dc offsets. The SRF PLL can be completely implemented in software with pre-filters. The pre-filters are band pass and high pass filters these can be used to reduce harmonics present in the input and high pass filter alone can reduce the dc offset present in the input. The effects of high pass and band pass filters on dc offsets are analyzed. The superior performance of proposed pre-filter-based SRF PLL phase detection system is studied and the obtained results are compared with SRF PLL-based phase detection to confirm the feasibility of the study under different grid environment such as high-harmonic injection. All analytical results are verified using MATLAB software.

Keywords—Grid-connected operation, phase-locked loop (PLL), Band pass filter, Low pass filter, seamless transfer, three-phase inverter, PI regulator, voltage sag detection.

I. INTRODUCTION

Phase locked loop is abbreviated as PLL. Brain of phase locked loop is voltage controlled oscillator. In technical fields, such as frequency control, frequency synthesizing, FM (frequency modulation) demodulation, data recovery, signal synchronization, there used PLL. Jitter attenuator for reduce noise within jitter is the versatile application of the phase locked loop that is for communication system, networking, variation of phase carried on a clock signal. Phase locked loop circuit is necessary for increase of circuit speed. This is known to provide a clock recovery circuit using a phase locked loop for example, in a digital transmission system, a clock signal which is used for timing purposes in processing the data signal. The data signal is a serial binary signal having binary 0s and 1s represented respectively by the absence and presence of a positive voltage and the clock signal is produced at the bit rate of the data signal. The present innovation relates to a phase-locked loop, and more particularly, to frequency stabilization of an oscillation output signal generated by a phase locked loop. The present invention further relates to a current drive type charge pump circuit and a voltage controlled oscillator of the phase-locked loop.

II. RELATED WORKS

In recent development era of new involvement of emerging technologies vastly introduce in the field of VLSI. Our study is based on PLL which is started in early in 1932 which reach to its peak with a great upsurge where as consumption of power and circuit area is reduced. The phase-locked loop (PLL) is a prime component globally used in various integrated circuit IC including clock recovery and wireless communication system frequency synthesizers and communication system. Currently, system-on-chip (SOC) and Microelectronics designs are used for delay-locked loops and for matching the clock [1]. By appropriate choosing the Phase frequency detector framework and adjusting the charge pump current and the loop filter design values gives a better lock time can be achieved [2]. Mahmoud Abdellaoui et.al presented the design of the Inverse Sine Phase Detector (ISPD) with more effective and simplicity, robustness, in this ISPD PLL Demodulator designed without using any of the filters [3]. Modeling and design of a multi-standard fractional PLL in CMOS/SOI technology is used in [4]. To suppress them coupled supply noise A step-down voltage regulator is utilized is described in [5]. By limiting the sweep rate of VCO for a phase-lock loop applied sweep voltage which promptly declined the closed-loop frequency error to a tip where phase lock occurs quickly [6]. A low-power high compelling ability voltage control oscillator used in PLL is introduced in [7]. To control the loop dynamic characteristics, the capacitance in the loop filter is on-chip calibrated so that the loops are accurately controlled despite the process variation [8]. In this article demonstrate the chaotic behavior of a nonlinear amplifier (NLA) - based delayed phase-lockedloop (PLL) including a first order phase detector for a certain range of system parameters [9]. A multiplexer based lengthvarying ring oscillator and the effects of using it as a voltage controlled oscillator (VCO) in a phase locked loop (PLL) based system is proposed in [10]. A research of true random number generator based on PLL using FPGA in [11].

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PLL has been applied in, angle modulation, carrier regeneration and demodulation, frequency synthesis, data/clock recovery etc [12-14]. The main incorporation of data and clock recovery are jitter transfer, tolerance, generation, acquisition time and capture range, among which jitter characteristics are the major and most important clock data recovery specifications is illustrated in [15].a new charge pump circuit is introduced by using 0.18 μm CMOS technology, which helps in reducing the mismatch of current which lies in between two branches of the cascade current mirror topology, By using this proposed circuit, the mismatching between the two input UP/DN current of the Charge pump can be achieved with less than 0.065% from post-layout simulation and spur is also reduced with applying low power consumption and low noise technique which results in better output [16].

III.WORKING PRINCIPLE OF CONVENTIONAL PLL TECHNIQUES

The basic structure of Synchronous Reference Frame PLL(SRF-PLL) is shown in Fig. 1. In this angular frequency detection circuit at first, by the use of Park's transformation the three-phase voltage vector is transformed from the abc-natural rotating reference frame to the dq- synchronous reference frame as shown in equation(1).

$$v_{sa} = V_m \cos(\theta)\,,\; v_{sb} = V_m \cos\left(\theta - \frac{2\pi}{3}\right)\,,\; v_{sc} = V_m \cos\left(\theta + \frac{2\pi}{3}\right)$$

In alpha-beta reference frame:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}$$

$$v_\alpha = V_m \cos(\theta)\,,\; v_\beta = V_m \sin(\theta)$$

In dq - reference frame

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} \cos(\theta^*) & \sin(\theta^*) \\ -\sin(\theta^*) & \cos(\theta^*) \end{bmatrix} \cdot \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{1}$$

$$v_{sd} = V_m \cos(\theta - \theta^*)\,,\; v_{sq} = V_m \sin(\theta - \theta^*)$$

If $\theta^* = \theta\,,\; v_{sd} = V_m\,,\; v_{sq} = 0\,,\; \theta - \theta^* = \Delta\theta$

θ^* is the output response, shown in figure 1. At steady state control action is taken such a way $\Delta\theta$ should be zero.

$$v_{sd} = V_m \cos\Delta\theta\,,\; v_{sq} = V_m \sin\Delta\theta$$

A feedback loop is used to regulate the q component to zero by controlling the angular velocity of the dq synchronous reference frame. The voltage vector amplitude is given by the d component and the output of feedback loop gives the angular velocity of the grid as shown in Fig.1. When a balanced fault occurs, the $dq-$PLL is operating well and can track the phase angle. However, when an unbalanced fault occurs, then the $dq-$PLL fails to track accurately the phase angle because V_d does not perfectly match with the positive sequence voltage V^p due to the oscillation which appears because of the existence of the negative sequence voltage V^n under unbalanced disturbances [17].

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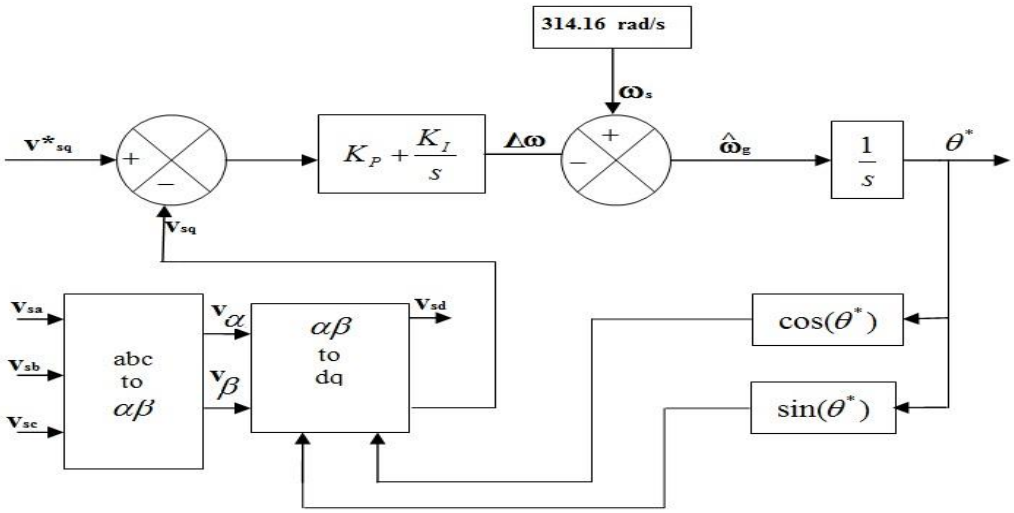

Fig.1.General structure of the SRF-PLL

IV.PERFORMANCE OF PLL TECHNIQUE IN UNBALANCED GRID VOLTAGE

The input phase voltage space vector of the grid supply voltage can be written as

$$\vec{v}_i = \frac{2}{3}\left(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}} \right) \qquad (2)$$

In the case of a balanced and sinusoidal supply voltage, $\vec{v}_i$ makes a circular trajectory because the magnitude of $\vec{v}_i$ and angular velocity are constant. When the grid voltages are unbalanced then it consists of a positive sequence component vector and a negative sequence component vector as in equation (3)

$$\vec{v}_i = \vec{v}_p + \vec{v}_n$$

$$\vec{v}_i = V_p e^{j\omega_i t} + V_n e^{-j\omega_i t - \theta_n} \qquad (3)$$

where, ω_i is the angular frequency; $\vec{v}_p$ is the positive sequence component whose peak value is V_p and the initial phase angle is assumed zero; $\vec{v}_n$ is the negative sequence component whose peak value is V_n and θ_n is the initial phase angle of the unbalanced grid voltage.Space vectors $\vec{v}_p$ rotates in anti-clockwise direction with angular velocity ω_i and $\vec{v}_n^*$ rotates in clockwise direction with angular velocity ω_i as shown in Fig.2..Due to the presence of negative sequence component vector in the grid voltages, $\vec{v}_i$ makes an elliptical trajectory because the magnitude of $\vec{v}_i$ and angular velocity is not constant with time.

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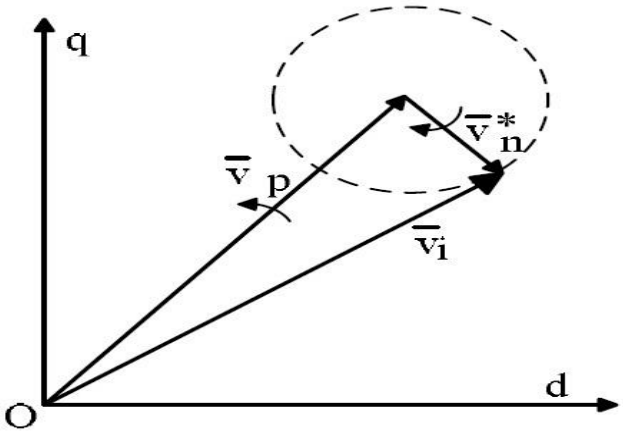

Fig. 2. Space vector representation of the unbalanced grid phase voltage

A. Different PLL Techniques

In normal grid condition ,SRF-PLL behaves with quite high bandwidth fast and accurate performance. In harmonics distortion and imbalance condition,it fails in accuracy. In last decades many researchers investigated in improving the conventional PLL as follows,

B. Double Synchronous Reference Frame (DSRF) PLL

The unbalanced voltage vector, consisting of positive and negative sequence components is expressed on a "double synchronous reference frame"(DSRF). An improved three phase PLL technique [18] based on using, positive and negative synchronous speed. The handling of this technique permits in decoupling the effect of negative sequence component by the SRF rotating with positive angular speed, that makes possible grid synchronization in unbalanced conditions.

C. Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL)

In this PLL technique two rotating reference frames: one for the positive sequence component (dq^p) rotating in the anticlockwise direction whose initial phase angle is θ' and another one for the negative sequence component (dq^n) rotating in the clockwise direction whose initial phase angle is $-\theta'$ are used for the detection of the angular frequency accurately in the case of the unbalanced grid voltages. Both reference frames are rotating with an angular velocity of ω_i .When the unbalanced grid voltages are transformed from abc reference frame to $\alpha\beta$ reference frame then it also consists two sub-vectors positive sequence vector $\vec{v}^{\,p}_{(\alpha\beta)}$ and negative sequence vector $\vec{v}^{\,n}_{(\alpha\beta)}$ as expressed in equation (4)

$$\vec{v}_{in}(\alpha\beta) = \begin{bmatrix} \vec{v}_\alpha \\ \vec{v}_\beta \end{bmatrix} = \vec{v}^{\,p}_{(\alpha\beta)} + \vec{v}^{\,n}_{(\alpha\beta)} \tag{4}$$

$$\vec{v}_{in(\alpha\beta)} = V_p \begin{bmatrix} \cos(\omega_i t + \phi_p) \\ \sin(\omega_i t + \phi_p) \end{bmatrix} + V_n \begin{bmatrix} \cos(-\omega_i t + \phi_n) \\ \sin(-\omega_i t + \phi_n) \end{bmatrix} \tag{5}$$

V_p is the peak value and ϕ_p is the initial phase angle of positive sequence of the input voltages; V_n is the peak value and ϕ_n is the initial phase angle of negative sequence of the input voltage and θ' is the phase angle which is the output of PLL. Then, if PLL is detecting the phase angle θ' accurately then it could be assumed that θ' is approximately equal to $\omega_i t$. The voltage vectors $\vec{v}^{\,p}_{(dq)}$ and $\vec{v}^{\,n}_{(dq)}$ after the transformation from $\alpha\beta$ stationary reference frame to the dq^p and dq^n rotating reference frames can be expressed as follows:

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$$\vec{v}_{(dq)}^{\,p} = \begin{bmatrix} \vec{v}_d^{\,p} \\ \vec{v}_q^{\,p} \end{bmatrix} = \left[T_{dq}^{\,p}\right]\vec{v}_{in(\alpha\beta)}$$

$$\vec{v}_{(dq)} = \begin{bmatrix} \vec{v}_d^{\,p} \\ \vec{v}_q^{\,p} \end{bmatrix} = V_p \begin{bmatrix} \cos(\phi_p) \\ \sin(\phi_p) \end{bmatrix} + V_n \cos(\phi_n) \begin{bmatrix} \cos(2\omega_i t) \\ -\sin(2\omega_i t) \end{bmatrix} + V_n \sin(\phi_n) \begin{bmatrix} \sin(2\omega_i t) \\ \cos(2\omega_i t) \end{bmatrix} + V_n \sin(\phi_n) \begin{bmatrix} \sin(2\omega_i t) \\ \cos(2\omega_i t) \end{bmatrix} \quad (6)$$

$$\vec{v}_{(dq)}^{\,n} = \begin{bmatrix} \vec{v}_d^{\,n} \\ \vec{v}_q^{\,n} \end{bmatrix} = \left[T_{dq}^{\,n}\right]v_{in(\alpha\beta)}$$

$$\vec{v}_{(dq)}^{\,n} = \begin{bmatrix} \vec{v}_d^{\,n} \\ v_q^{\,n} \end{bmatrix} = V_n \begin{bmatrix} \cos(\phi_n) \\ \sin(\phi_n) \end{bmatrix} + V_p \cos(\phi_p) \begin{bmatrix} \cos(2\omega_i t) \\ \sin(2\omega_i t) \end{bmatrix} + V_p \sin(\phi_p) \begin{bmatrix} -\sin(2\omega_i t) \\ \cos(2\omega_i t) \end{bmatrix} \quad (7)$$

Where,

$$\left[T_{dq}^{\,p}\right] = \left[T_{dq}^{\,n}\right]^T = \begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix}$$

As can be seen from (6) and (7), the magnitude of the low harmonic components in the dq^p axis depends on the average value of the signal in the dq^n axis, and the magnitude of the low harmonic components in the dq^n axis depends on the mean value of the signal in the dq^p axis.

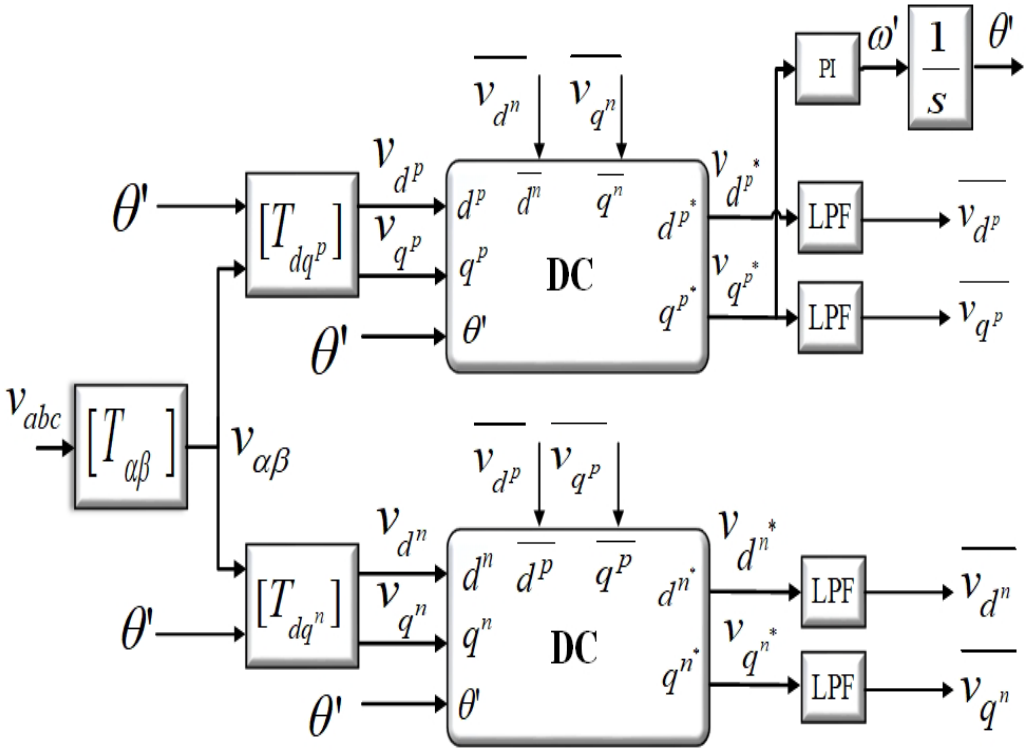

Fig. 3. Block diagram of the DDSRF-PLL

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For the elimination of low order harmonics from the dq^p and dq^n axis a decoupling network is used for the elimination of the oscillations from both reference frames.

The equations of the decoupling network is

$$\vec{v}_d^{\,p^*} = v_d^p - \cos(2\omega_i t)\vec{v}_d^{\,n} - \sin(2\omega_i t)\vec{v}_q^{\,n} \quad (8)$$

$$\vec{v}_q^{\,p^*} = v_q^p - \cos(2\omega_i t)\vec{v}_q^{\,n} + \sin(2\omega_i t)\vec{v}_d^{\,n} \quad (9)$$

$$\vec{v}_d^{\,n^*} = v_d^n - \cos(2\omega_i t)\vec{v}_d^{\,p} + \sin(2\omega_i t)\vec{v}_q^{\,p} \quad (10)$$

$$\vec{v}_q^{\,n^*} = v_q^n - \cos(2\omega_i t)\vec{v}_q^{\,p} - \sin(2\omega_i t)\vec{v}_d^{\,p} \quad (11)$$

Fig.3 shows the basic scheme of the DDSRF-PLL technique. After the decoupling network the signal $v_q^{p^*}$ can be used as the input to the $dq-PLL$ for the detection of the fundamental angular frequency without any error.

D. Voltage Reforming Synchronous Reference Frame PLL (V RSRF -PLL)

The basic structure of the Voltage Reforming Synchronous Reference Frame PLL (VRSRF-PLL) technique [16] as shown in Fig.4. It consists of two blocks, first one is the voltage reforming block and the second one is the conventional $dq-PLL$ block. Input signals of the voltage reforming block are v_a, v_b and v_c ;which are the grid voltages with magnitude unbalance and v_a^*, v_b^* and v_c^* are the output of the voltage reforming block which are balanced signals with same magnitude after signal reforming.

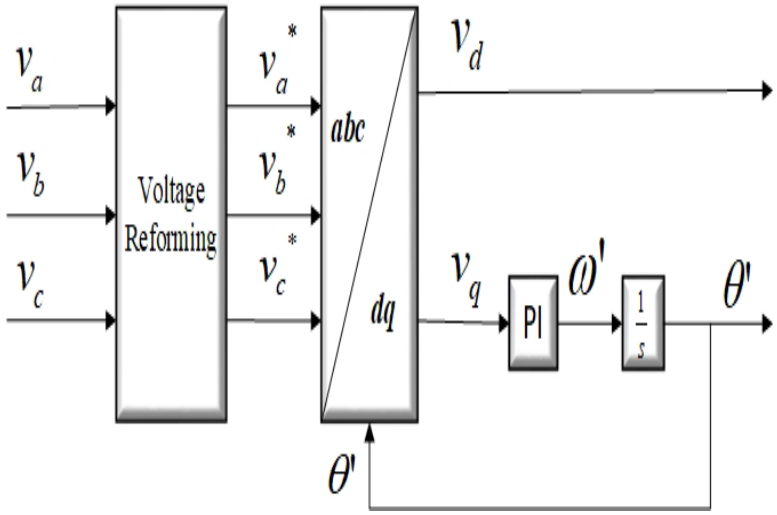

Fig. 4. Block diagram of the vrsrf – PLL

The grid voltages with magnitude unbalance can be expressed as equation (12), v_a, v_b and v_c

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_a \cos(\theta_a) \\ V_b \cos(\theta_b) \\ V_c \cos(\theta_c) \end{bmatrix} \quad (12)$$

where V_a, V_b, V_c are the amplitudes and $\theta_a, \theta_b, \theta_c$ are the phase angles of the grid voltages v_a, v_b and v_c respectively. Two coefficients k_2 and k_3, are defined which satisfy the relation in equation (13).

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By the use of k_2 and k_3, a new voltage sequence $(v_a, k_2 v_b, k_3 v_c)$ could be derived in equation(14). Hence, by the calculation of k_2 and k_3 a new reformed balanced set of voltages could be created without disturbing the grid phase angle information.

$$V_a = k_2 \times V_b = k_3 \times V_c \tag{13}$$

$$\begin{bmatrix} v_a \\ k_2 v_b \\ k_3 v_c \end{bmatrix} = \begin{bmatrix} V_a \cos(\theta_a) \\ k_2 V_b \cos(\theta_b) \\ k_3 V_c \cos(\theta_{c)} \end{bmatrix} = \begin{bmatrix} V_a \cos(\theta_a) \\ V_b \cos(\theta_{b)} \\ V_c \cos(\theta_c) \end{bmatrix} \tag{14}$$

$$v_a + k_2 v_b + k_3 v_c = 0 \tag{15}$$

For the calculation of k_2 and k_3, any one of the phase voltage is taken as the reference signal, here v_a is taken as the reference signal. At first the value of k_3 is calculated by identifying the zero-crossing instants of phase voltage v_b. At the zero crossing instant of phase voltage v_b, equation(15) becomes (16) at this instant. Then by using the instantaneous values of v_a and v_c the value of the coefficient k_3 could be exactly calculated in equation (17)

$$v_a \mid v_{b=0} + k_3 \times v_c \mid v_{b=0} = 0 \tag{16}$$

$$k_3 = -\frac{v_a \mid v_{b=0}}{v_c \mid v_{b=0}} \tag{17}$$

The reformed phase voltage v_c^* can be calculated as

$$v_c^* = \left(-\frac{v_a \mid v_{b=0}}{v_c \mid v_{b=0}} \right) v_c = k_3 v_c \cos(\theta_c) = V_a \cos(\theta_c) \tag{18}$$

Now two phases become equal in magnitude and the phase v_b reformed signal v_b^* can be generated by the use of equation (15).

$$v_b^* = -v_a - v_c^* \tag{19}$$

Now all the reformed phase voltages have the same magnitude which is the same as that of the magnitude of the reference signal. Hence, in this case, the conventional dq gives accurate results because the input signals to the $dq - PLL$ are balanced one. Each PLL has some merit and demerit so, you have to select the PLL according to the grid voltages. The comparison of different PLL given in Table I.

TABLE I: COMPARISION PLL TECHNIQUE

Qualities	SRF-PLL	DSRF-PLL	DDSRF-PLL	VRSRF-PLL
Positive sequence detection	NO	Yes	Yes	Yes
Balanced	Yes	Yes	Yes	Yes
Magnitude and phase unbalanced	No	Yes	Yes	Yes
Settling time	2.5ms	1.5ms	20ms	1.5ms
Architecture simplicity	Yes	No	No	No
Transient spike	Very high	Very Low	Very Low	Very Low

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V.CONCLUSION

In this paper analysis and performance of conventional and proposed synchronization technique is presented. For grid side converter control technique, the proposed DSRF, DDSRF and VRSRF technique tracks the signal unbalanced voltage and frequency conditions. The main important point of the technique is presented in this paper showed that the stationary reference frame PLL accurately detects the fundamental angular frequency in the case of balanced grid voltages, a voltage reforming synchronous reference frame PLL is a suitable solution for the detection of the fundamental angular frequency in the case of magnitude unbalanced grid voltages and a decoupled double synchronous reference frame PLL is a suitable solution to the detection of the fundamental frequency in the case of magnitude and phase unbalanced grid voltages.

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