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Highly Efficient Hybrid Model Carry Select Adder with Power-Area-Delay Trade

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Abstract: In this study, we offer a high speed design, a design with the smallest size compared to prior CSLAs, and two hybrid designs for Square root (SQRT) Carry Select Adder (CSLA). The first proposed architecture uses a new fast and merged add-one and multiplexing circuit to optimise the Binary to Excess-1 Converter (BEC)-based CSLA.
This architecture, in addition to having a significantly lower area, delay, and energy consumption than the BEC CSLA, takes up about the same space as the best extant CSLA, the IR redundant Carry Generation and Selection scheme (IRCGS CSLA), while delivering a greater speed. The area-optimized architecture of IRCGS CSLA, which uses a new logic optimization while preserving speed, is the second suggested CSLA as the lowest-area design. To reduce the number of gates and produce a more compact architecture, this system employs multiplexer-based logic. Furthermore, experimental results reveal that Hybrid CSLAs are more favourable since they combine the advantages of both architectures. It can be coupled with a variety of parallel prefix adders to increase performance even further. Furthermore, the hybrid CSLAs surpass the best current design in all three area, delay, and energy metrics.

Keywords: Carry select adder, Parallel prefix adder, Ripple carry adder, Hybrid CSLA

I. INTRODUCTION

In today's consumer electronics and portable gadgets, high-speed computations with minimal costs and power consumption are increasingly desired. Fast compute algorithms, in general, increase power consumption and area overhead in portable devices [1]. In fact, Very Large-Scale Integration (VLSI) circuit designers face a problem in creating high-speed digital circuits with a small chip size and low energy consumption [2]. One of the most important processes in computing and digital processing systems is addition. Normally, sophisticated processing systems include many arithmetic units and, as a result, multiple adders.
As a result, the system's performance is significantly improved by the efficient design of adders in terms of delay, area, and energy. The first category contains approaches that use the outputs of the first RCA to replace the second RCA in each CSLA group (the RCA with the input carry Cin equal to one) with a simpler logic (the RCA with the input carry Cin equal to zero). The approaches that evaluate prior CSLAs based on their logic operations and apply some logic optimizations to remove duplicate operations fall into the second category for reducing area and power consumption. Additional designs, such as [25–27], that improved on prior designs by including and mixing other adder structures into the CSLA exist in addition to the listed CSLAs. The area-delay product of hybrid CSLAs is reduced by 10-48 percent, while the energy delay product is reduced by 8-65 percent. It can be used in conjunction with a variety of parallel prefix adders to improve on existing hybrid systems. Here, a highly efficient hybrid architecture with power area delay trade is proposed.

II. BASIC CARRY SELECT ADDER

To reduce both size and power consumption, the BEC CSLA offered as the best design of the first category employs a gate-level add-one circuit (BEC unit) instead of the second RCA (the RCA with the input carry Cin = 1) of the standard CSLA. To prepare all essential inputs for the selection part of the CSLA, including 2-to-1 multiplexers, the BEC unit adds one to the output sum of the RCA with the input carry Cin = 0. An m-bit single-stage BEC CSLA's architecture is shown in fig 1. This CSLA can be organised as a multi-stage CSLA, just like other CSLAs.

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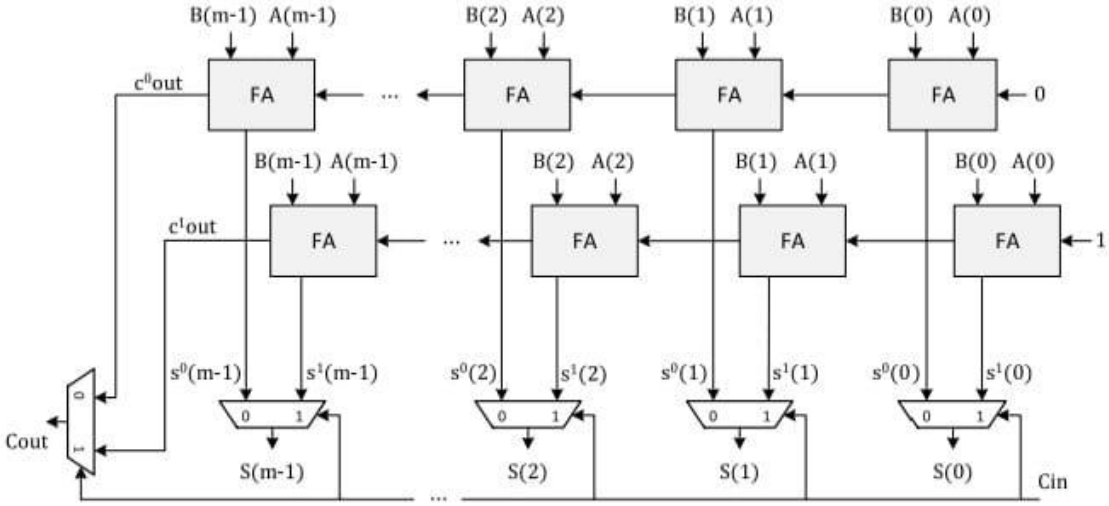

Fig 1. BEC CSLA

III. CSLA WITH FAST ADD-ONE AND MULTIPLEXING CIRCUIT

The FAM CSLA differs from the standard CSLA. Because there is no multiplexer in this architecture, it is more compact and simpler than plain CSLA. By creating RCA in each group utilising FA structures, more speed may be attained. There are four different types of Gate level FAs that are examined.

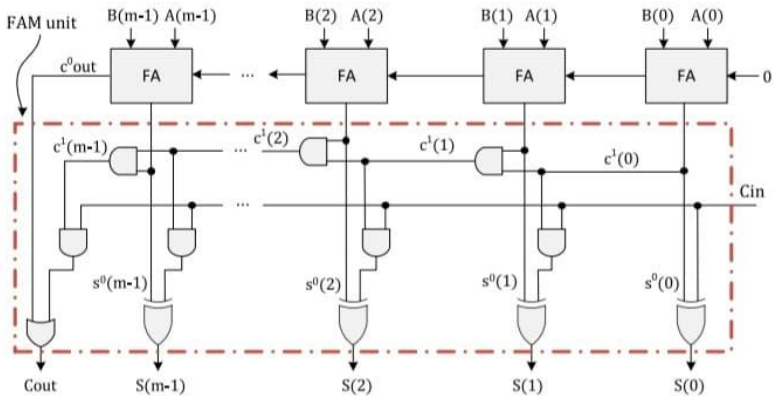

Fig 2. FAM CSLA

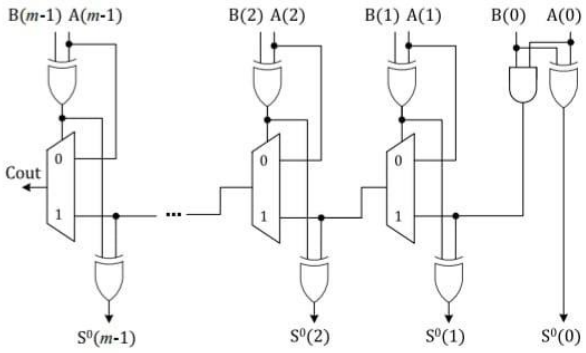

Fig 3. RCA with MUX based

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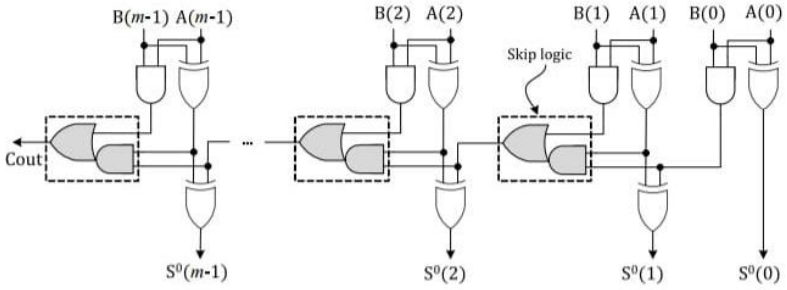

Fig 4. RCA with skip logic based carry generation

IV. LOW COST CSLA

In comparison to CGS and IRCGS CSLAs, low cost CGS (LCCGS CSLA) achieves a smaller area. The latency is the same, but the power usage is lower. The LCCGS CSLA block diagram has four steps. The Propagate Signal Generation is the first phase. Two parallel units exist in the second phase. The CS unit is the third step. Full Sum Generation is the fourth phase. Furthermore, its power consumption is lower than CGS CSLA and nearly equal to IRCGS CSLA.

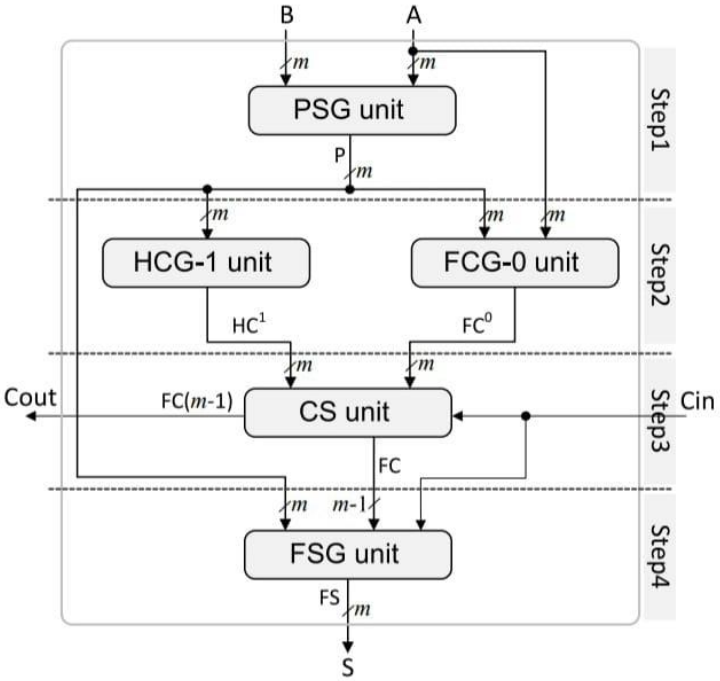

Fig 5. Block diagram of LCCGS CSLA

V.HYBRID CSLAs

A superior square root based CSLA is obtained by combining FAM CSLA and LCCGS CSLA. Hybrid1 and Hybrid2 16-bit SQRT CSLAs are addressed. The initial organisation, known as Hybrid1 CSLA, consists of a rapid RCA in the first stage, the FAM CSLA in the second and final phases, and the LCCGS CSLA in the intermediate stages. The Hybrid2 CSLA organisation consists of a quick RCA in the first stage, the FAM CSLA in the second and third stages, and the LCCGS CSLA in the remaining stages.

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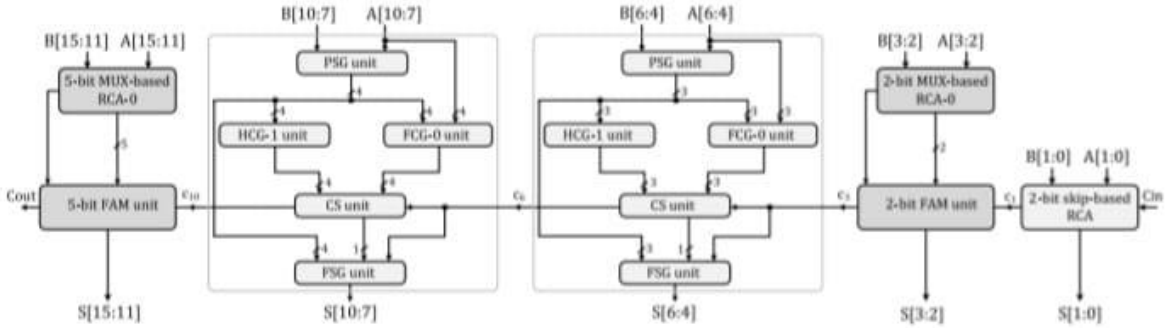

Fig 6. Hybrid-1 CSLA

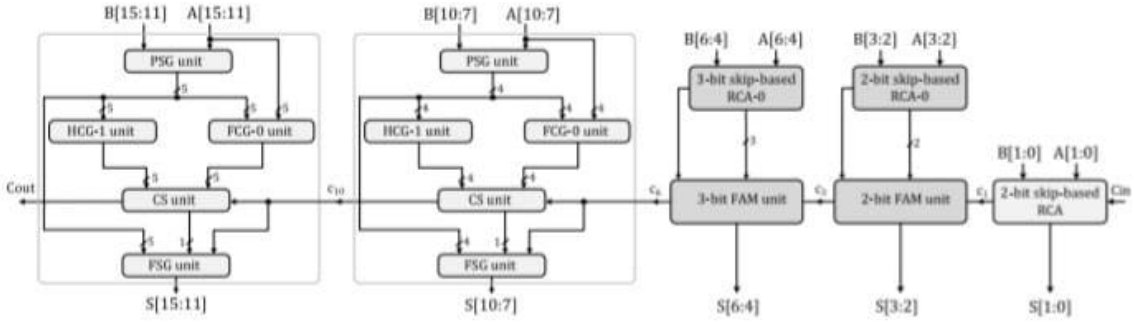

Fig 7. Hybrid-2 CSLA

In comparison to earlier designs, the two CSLA architectures have competitive qualities. For a wide range of 8-bit to 128-bit adder sizes, the Hybrid1 and Hybrid2 CSLAs, as well as LCCGS, outperform preceding designs.

VI. 4 BIT BRENT KUNG PARALLEL PREFIX ADDER

Hybrid CSLAs are more helpful since they combine the best features of both architectures. It can be used in conjunctio n with a variety of parallel prefix adders to improve on existing hybrid systems.
Here,a highly efficient hybrid architecture with power area delay trade is proposed. Many parallel prefix adders have be en constructed, such as the Kogge stone adder, the Ladnerfischer adder, and the Brent Kung adder. A 4 bit Brent Kung Parallel Prefix adder can be used to replace the CSG units in hybrid 1 and hybrid 2 structures, and then a comparison is made for a better outcome. The Brent Kung Parallel Prefix adder has a low fan out and critical path, as well as being a better delay adder.

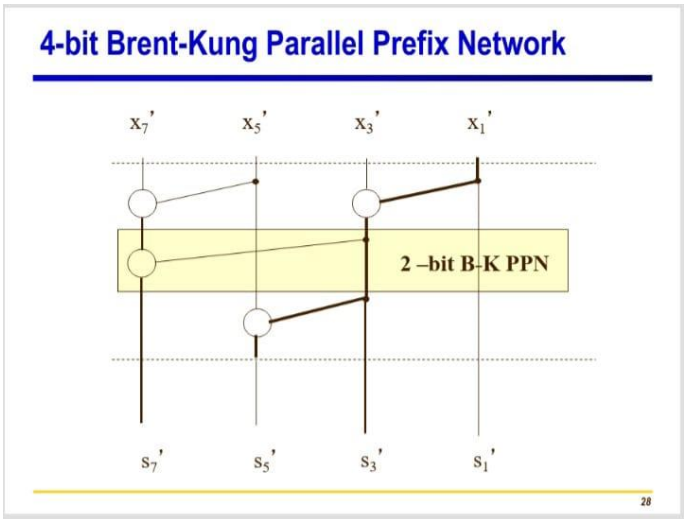

Fig 8. 4 bit Brent Kung parallel prefix adder structure

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VII. STIMULATION RESULTS

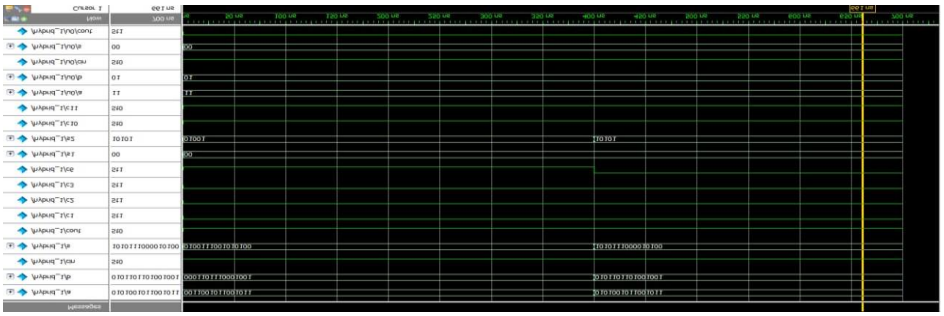

Fig 1. 16 bit SQRT CSLAs based hybrid 1

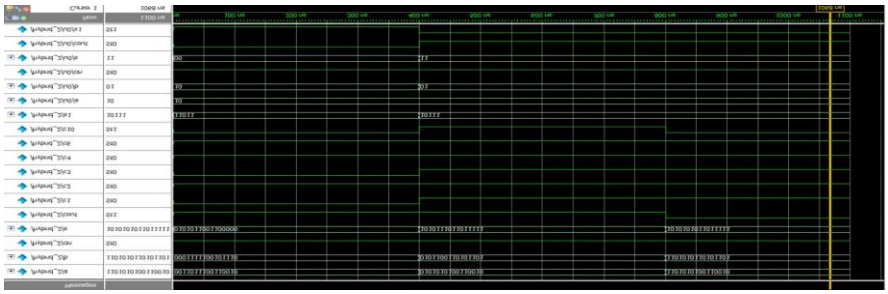

Fig 2. Hybrid 2

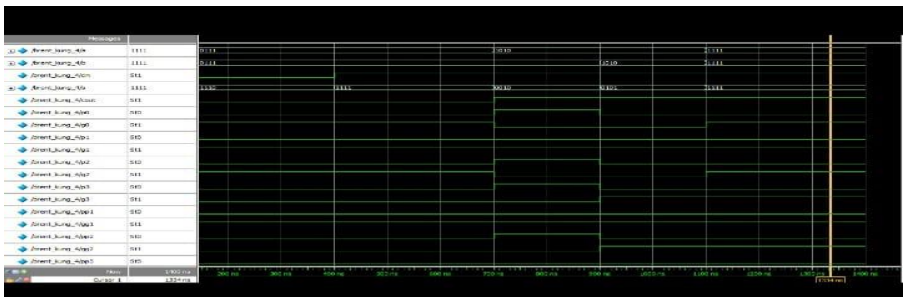

Fig 3. 4 bit Brent Kung parallel prefix adder

VIII. CONCLUSION

Hybrid CSLAs are more helpful since they combine the best features of both architectures. It can be used in conjunctio n with a variety of parallel prefix adders to improve on existing hybrid systems. Here, a highly efficient hybrid architect ure with power area delay trade is proposed. The proposed hybrid design achieves reduced power consumption, area, a nd delay

IX. ACKNOWLEDGMENT

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