IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 5, May 2022

DOI: 10.17148/IJIREEICE.2022.10536

Design and implementation of 32-bit MAC unit using reversible logic gate

Niveditha T[1], Shahaziya Parvez M[2]

Student, Department of electronics and communication engineering, IES college of engineering, Thrissur-Kerala, India[1]

Assistant Professor, Department of electronics and communication engineering, IES college of engineering, Thrissur-Kerala, India[2]

Abstract: The multiplication and accumulation processes are carried out by the MAC unit. Multiplier, adder, and accumulator are the basic MAC unit. - It has two stages of operations: one is to discover the product of two numbers, and the other is to get the sum of two numbers. Adding the goods to the other numbers and retailers is another option. It is stored in the accumulator. Utilization of power, delay, and LUT are the most essential factors in determining the performance of a set of processors Introducing Reversible logic gates are logic gates that can be used in both directions. In comparison to conventional logic, they dissipate less power. Vedic Multiplier is one of the most effective multipliers for lowering the cost. Postpone and enhance performance Moreover, various. To add the partial outputs, reversible adders are used. The proposed work compares the performance of several Reversible logic architectures are employed in MAC units.

Keywords: Reversible Logic, Urdhava Triyagbhayam, Ripple carry adder, Carry save adder , Carry look ahead adder

I.INTRODUCTION

The most essential word in the electronic field is low power design. To achieve great performance and low power dissipation, reversible logic gates are used. This logic has been proven, the primary feature for obtaining inputs from theoutputs that are related the following are the characteristics of reversible logic gates, In the circuit, fanout should be zero.34% of the time, feedback is not permitted.

Quantum capital is required at a minimum of 34 percent.34 The outputs and inputs are the same. In MAC, both addition and multiplication are performed. The multiplier is a crucial component in the development of any system. It's a MAC unit. The Vedic Multiplier is employed in this case. Procedure of multiplication In Vedic literature, there are sixteen sutras.[1] Mathematics. It is a cost-effective method of producing. Intermediate partial products, which has the benefit of parallel product.

The MAC unit will take up a lot of space and use a lot of electricity. have an impact on the electronic system's performance and quickness. As a result, In this research, we present a 32-bit MAC based on resible logic gate. Combined with a multiplier and RCA (ripple carry adder) Using a Vedic multiplier and RCA, create a MAC.

In addition, the document includes another MAC unit that employs a Vedic multiplier and carries Adder should be saved. Modalism is used to model all of the MAC units. XILINX ISE DESIGN is used for software and synthesis. SUITE. All MAC implementations were compared to one another. Factors for the area as well as the delay

II.REVERSIBLE LOGIC GATES

The CNOT gate, Toffoli Gate, Fredkin Gate, Peres Gate, and TKS gate are the basic and important reversible logic gates that are widely used everywhere and in this study. Bennet demonstrated in 1973 that reversible logic gates withstand information loss and use less power to compute the basic and important reversible logic gates. Are discussed farther down.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 7.047 ⁜ Vol. 10, Issue 5, May 2022
DOI: 10.17148/IJIREEICE.2022.10536

2.1 Feyman gate

The 2*2 Feynman gate is also called as controlled not (CNOT)

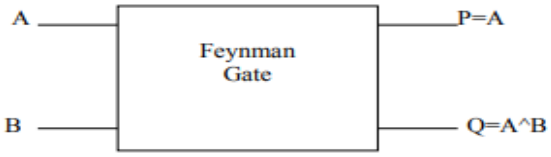

Fig 1. Feyman gate

2.2 Fredkin gate

Peres Gate is a 3*3 reversible logic gate that is commonly used as a half adder by setting the input variable C to zero and receiving sum and carry outputs from Q and R.

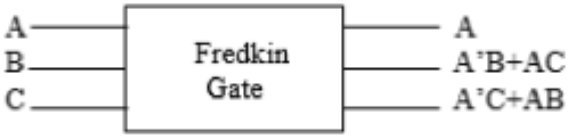

Fig 2. Fredkin gate

2.3 Peres gate

Peres Gate is a 3*3 reversible logic gate that is commonly used as a half adder by setting the input variable C to zero and receiving sum and carry outputs from Q and R

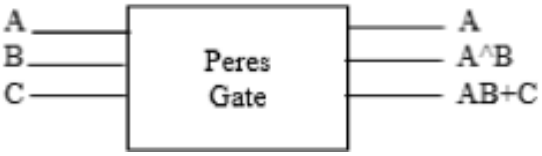

Fig 3. Peres gate

2.4 Toffoli gate

The Toffoli gate is a universal reversible logic gate in logic circuits, which means that it can be used to build any classical reversible circuit. It's also known as the "controlled-controlled-not" gate because of how it operates.

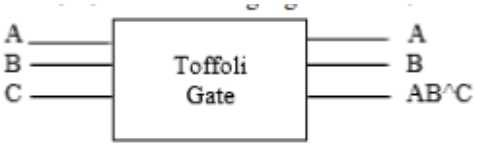

Fig 4. Toffoli gate

2.5 HNG gate

HNG gate works the function of full adder. it's a 4*4 reversible logic gate. it has quantum cost of 6.

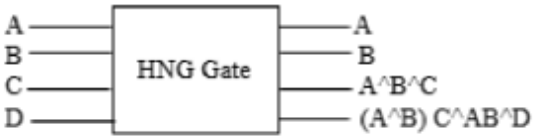

Fig 5. HNG gate

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 7.047 ⁜ Vol. 10, Issue 5, May 2022
DOI: 10.17148/IJIREEICE.2022.10536

2.6 TSG gate

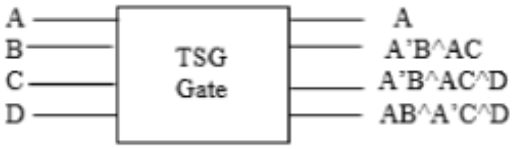

Fig 6. TSG gate

III.REVERSIBLE VEDIC MULTIPLIER

In this paper Vedic Multiplier is used as a multiplier of 32*32 bit of binary numbers. The algorithm is used here for the multiplication purpose which is Urdhva Tiryagbhyam. 2X2, 4X4, 8X8 and 16X16 bit multipliers are used to implement 32X32 bit multiplication

3.1 2X2 Reversible Vedic Multiplier

2X2 Reversible Vedic Multiplier consist of Peres gate and CNOT gate. The half adders function carried out by Peres gate. The output of 2X2 Vedic multiplier is given below. 3 inputs and 3 outputs are represented in figure

Q0=A0B0
Q1=A1B0
Q2=A0B1
Q3=A1B1

The product can find out 3 steps. The first step find is multiplication of A0A1 and B0B1 product step. step 2 cross multiplication is done by A1B0+A0B1.The final step is A1B1 product step

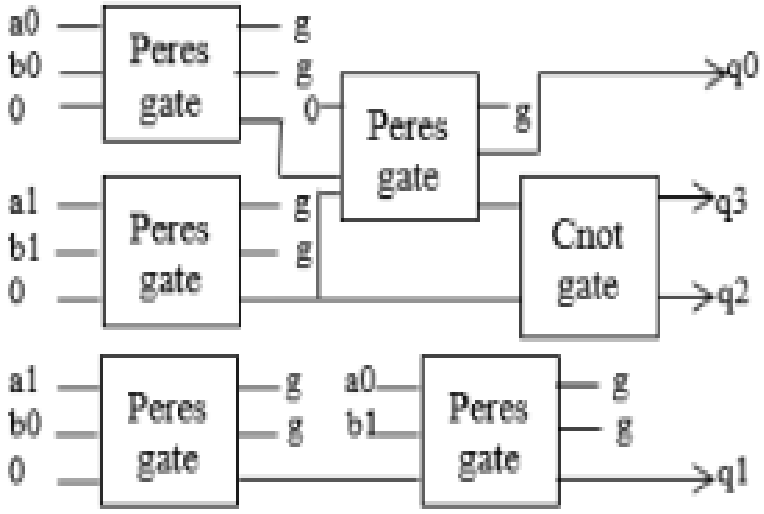

Fig 7. 2X2 Reversible Vedic Multiplier

3.2 4X4 Reversible Vedic Multiplier

The 4X4 bit Reversible Vedic Multiplier is designed by four 2X2 Vedic Multipliers, 2 Peres gates and has a Reversible OR gate to implement the design. Input is given to the four 2X2 multiplier. output is taken from Peres gate

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 5, May 2022

DOI: 10.17148/IJIREEICE.2022.10536

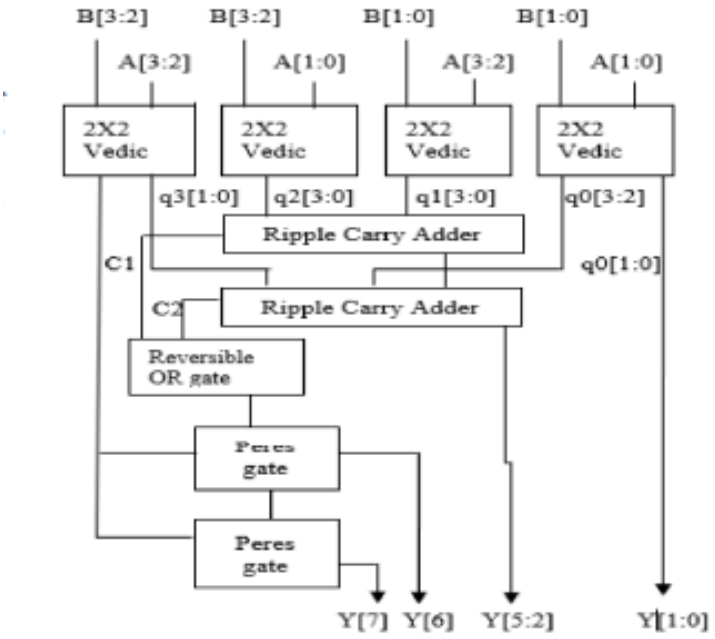

Fig 8. 4X4 Reversible Vedic Multiplier

IV.MAC UNIT WITH DIFFERENT ADDERS

To perform addition operation different type of adders are using in MAC unit, Ripple Carry Adder, Carry Save Adder and Carry Lookahead Adder are implemented using the reversible logic gate. MAC unit comprises of Multiplier, Adder and Accumulator blocks. In this paper, Vedic Multiplier performs multiplication and addition operation performed by Carry Save Adder, Ripple Carry Adder, Carry Lookahead Adder

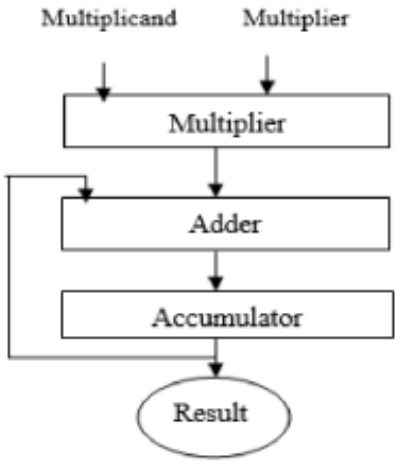

Fig 10. MAC unit

1. Reversible Carry look ahead adder

In Carry Look ahead adder, carry generated and propagated separately. The Peres gate is replaced as reversible gate to implement the carry look ahead adder ,it requires number of Peres gate to for n bit binary number . The figure shows 4 bit carry look ahead adder. . Reversible logic is playing a significant role in quantum computing as quantum operations are unitary in nature. Quantum computer performs computation at an atomic level

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 5, May 2022

DOI: 10.17148/IJIREEICE.2022.10536

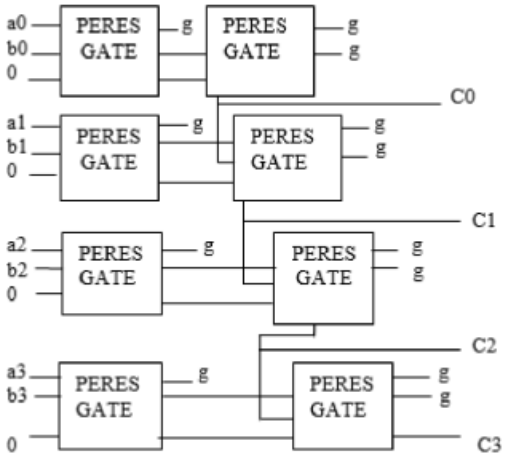

Fig 10. Reversible 4 bit carry look ahead adder

2. Reversible Ripple carry adder

The ripple carry adder perform the functions adding two-bit binary numbers it require a full adder. its also called n-bit parallel adder. For reversible operation it requires n number of HNG gate for n bit binary number. carry output is rippled to adjacent gate as one of the bit.

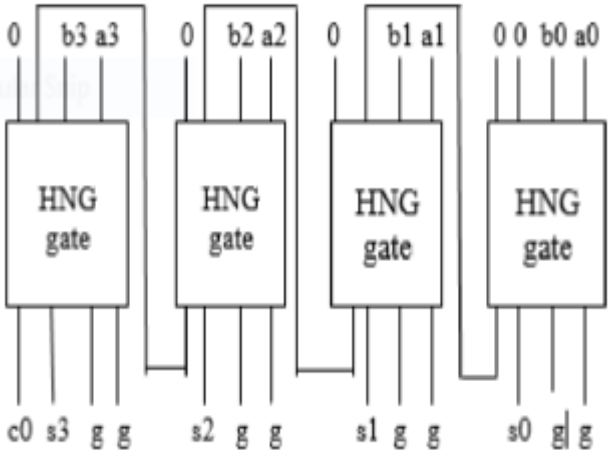

Fig 11. Reversible ripple carry adder

3. Reversible Carry save adder

Reversible carry save adder using Peres gate and NHG gate . The carry save adder consist full adders and half adders. it hasf(n-1) full adder and (n+1) half adders for representing it using Peres gate and HNG gate. Carry save adder used to add three or more number of bits

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 5, May 2022

DOI: 10.17148/IJIREEICE.2022.10536

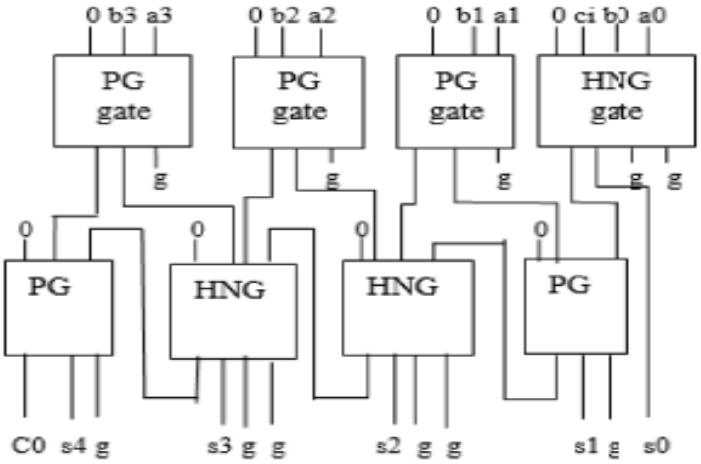

Fig 12. Reversible carry save adder

V.SIMULATION RESULTS

Reversible logic gates are used to implement MAC unit in the proposed work to design the 32-bit Mac unit. 32-bit binary multiplication used here is obtained from 2X2 multiplication, 4X4 multiplication, 8X8 multiplication and 16X16 multiplication. The corresponding simulation result are shown in figure. Synthesis done by Xilinx ISE 14.3 and implemented using Xilinx

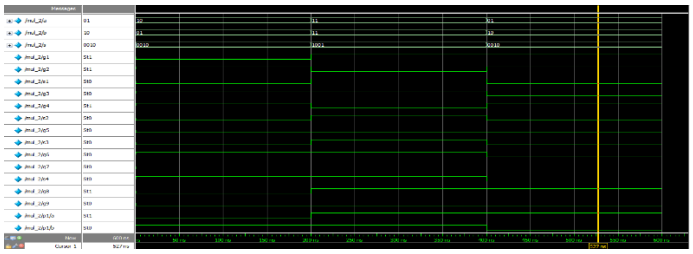

Fig. 1 2X2 bit multiplication using reversible gate

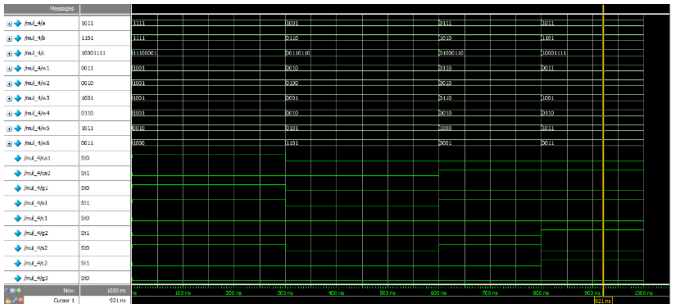

Fig. 2 4X4 bit multiplication using reversible gate

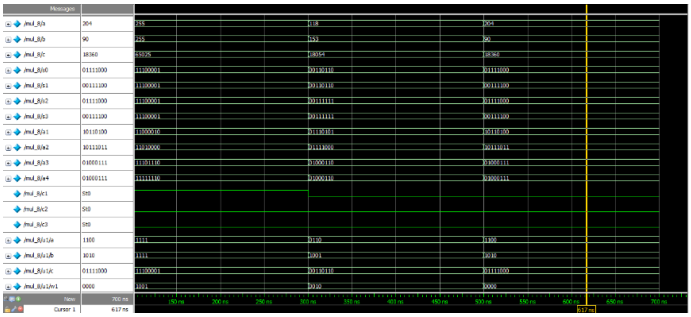

Fig. 3 8X8 bit multiplication using reversible gate

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 5, May 2022

DOI: 10.17148/IJIREEICE.2022.10536

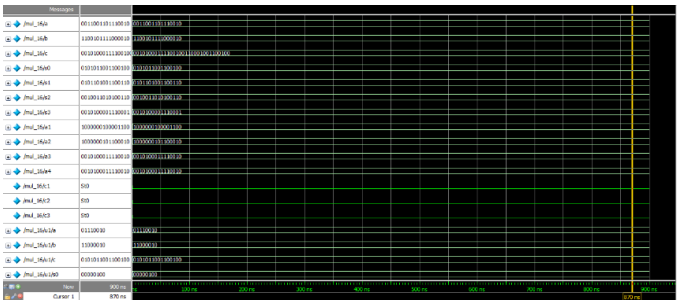

Fig. 4 16X16 bit multiplication using reversible gate

VI.CONCLUTION

In this paper, reversible logic gates were specifically wont to implement the MAC unit. Multiplication operation done Vedic multiplier using reversible logic gates. Addition operation through with ripple carry adder and carry save adder and carry look ahead adder. designed 32-bit MAC unit with reversible logic gate. High performance and low power MAC unit is designed

VII.ACKNOWLEDGEMENT

The authors are thankful to 'CLAROZON TECHNOLOGIES' and also to Ms. Shahaziya Parvez M, for her valuable suggestions and technical staff members of CLAROZON TECHNOLOGIES' are acknowledged for their suggestions.

VIII.REFERENCES

[1]. FPGA Implementation of 32 Bit Complex Floating Point Multiplier Using Vedic Real Multipliers with Minimum Path Delay 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering KK.Deergha Rao Dept. of ECE, VasavPP.V. Muralikrishna Ch. Gangadhar 2018

[2]. Exploring the Use of Parallel Prefix Adder Topologies into Approximate Adder Circuits Morgana Macedo- Federal University of Rio Grande do Sul (UFRGS), Porto Alegre, Brazil 2017

[3]. FPGA-Based Parallel Prefix Speculative Adder for Fast Computation Application 2020 Sixth International Conference on Parallel, Distributed and Grid Computing (PDGC) Garima Thakur Harsh Sohal Shruti Jain

[4]. FPGA Implementation of Complex Multiplier Using Minimum Delay Vedic Real Multiplier Architecture 2016 IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering (UPCON) Indian Institute of Technology (Banaras Hindu University) Varanasi, India, Dec 9-11, 2016

[5]. FPGA Implementation of Complex Multiplier Using Minimum Delay Vedic Real Multiplier Architecture 2016 IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering (UPCON) Indian Institute of Technology (Banaras Hindu University) Varanasi, India, Dec 9-11, 2016

[6]. Exploring the Use of Parallel Prefix Adder Topologies into Approximate Adder Circuits 978-1-5386-1911-7/17/$31.00 ©2017 IEEE Morgana Macedo†, Leonardo Soares∗, Bianca Silveira†, Claudio M. Diniz ´ †, Eduardo A. C. da Costa

[7]. FPGA Implementation of 32 Bit Complex Floating Point Multiplier Using Vedic Real Multipliers with Minimum Path Delay 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON) KKK.Deergha Rao PP.V. Muralikrishna Ch. Gangadhar

[8]. FPGA-Based Parallel Prefix Speculative Adder for Fast Computation Application 2020 Sixth International Conference on Parallel, Distributed and Grid Computing (PDGC) Garima Thakur Harsh Sohal Shruti Jain