IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 4, April 2022

DOI: 10.17148/IJIREEICE.2022.10418

Review And Implementation Of 4:2 Compressor Based Multiplier Using Verilog

C.M.Rohini[1], Dr.B.Sargunam[2], Dr.R.Chitra[3] , E.Elakkiya[4]

M.E VLSI Design, School of Engineering, Avinashilingam Institute for Home Science and Higher Education for Women,Coimbatore[1,2,3]

Assistant Professor, Department of ECE, School of Engineering, Avinashilingam Institute for Home Science and Higher Education for Women,Coimbatore[4]

Abstract: The scientific literature, which suggests numerous circuits built with approximate 4-2 compressors, has a lot of interest in approximation multipliers. The designer who desires to employ an approximation 4-2 compressor faces the difficulty of selecting the suitable topology due to the enormous variety of available alternatives. This paper compares approximate 4-2 compressors already proposed in the literature in this work. We also introduce a fresh approximate compressor, bringing the total number of approximate 4-2 compressors studied to twelve. The circuits under investigation are used to create 8x8 and 16x16 multipliers in 28nm CMOS technology.

Keywords: Multiplier, 4:2 Compressor, Half adder, full Adder.

1. INTRODUCTION

Machine learning, multimodal digital signal processing, data mining, and data recognition are only a few of the major applications that are error resistant. Approximate computing is an excellent technique to make efficiency gains in terms of power, speed, and area for these types of applications. The backbone of most multimedia applications is Digital Signal Processing (DSP) blocks. The image and video processing algorithms are implemented in the majority of these DSP blocks, with the final output being either an image or a video for human consumption. Because of the limitations of human eyesight, the algorithms' outputs are numerically approximate rather than exact. This loosening of numerical precision is beneficial. some latitude in carrying out imperfect or approximate tasks computation. The freedom can be used to come up with new ideas. at several phases of design, come up with low-power designs logic, architecture, and algorithm are examples of abstractions. Inexact computing methodologies rely on the fact that many applications can accept some loss of precision, and hence the solution can tolerate some uncertainty. Inexact computer applications, on the other hand, are typically implemented utilizing digital binary logic circuits, which provide a high level of predictability and precision. A methodology with a reduced degree of precision and growing uncertainty in operation can nonetheless be used with a framework based on a precise and specialized implementation. For addition, full-adder cells have been thoroughly investigated for approximate computing. Multiplication is a widely used operation in computer arithmetic. When creating bio-inspired systems, for example, the inexact computation paradigm relies on relaxing fully accurate and perfectly predictable basic elements such as a full adder. This allows nature inspired computation to reroute the current design process of digital circuits and systems, resulting in a reduction in complexity and expense, as well as a possible boost in performance and power efficiency.

2. MULTIPLIER

The two essential functions of partial product creation and summations are merged in the n array multiplier. N2+N-1 cells (where N2 has an AND gate for partial product generation, a full adder for summing, and N-1 cells contain a full adder) are coupled to form a multiplier for unsigned N N multiplication. This array creates N lower product bits directly and forms the top N bits of the product using a carry-propagate adder, in this instance a ripple carry adder. The array multiplier's two basic functionalities, partial product creation and summation, are integrated. N2+N-1 cells are coupled to form a multiplier for unsigned N x N multiplication, where N2 has an AND gate for partial product creation, a full adder for summing, and N-1 cells contain a full adder. The array creates N lower product bits directly and forms the top N bits of the product using a carry-propagate adder, in this case a ripple carry adder. By substituting half adders for full adders, the complexity can be reduced to N2 AND gates, N half adders, and N(N-2) full adders. (2N-2) c is the worst-case delay, where c is the adder delay. In order to create a multi-array array, The partial products are computed by analyzing two multiplicand bits at a time. In comparison to the simple array multiplier, this approach gives no performance or area gain save for the ability to use two's complement operands. However, a higher radix modified Booth method can be used to produce better latency.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 4, April 2022

DOI: 10.17148/IJIREEICE.2022.10418

Baugh et al. proposed another approach for generating an array multiplier that handles two's complement operands, as shown in fig. 1. The maximum column height is increased by two with this strategy. This could result in a second round of partial product reduction, resulting in longer overall delays.

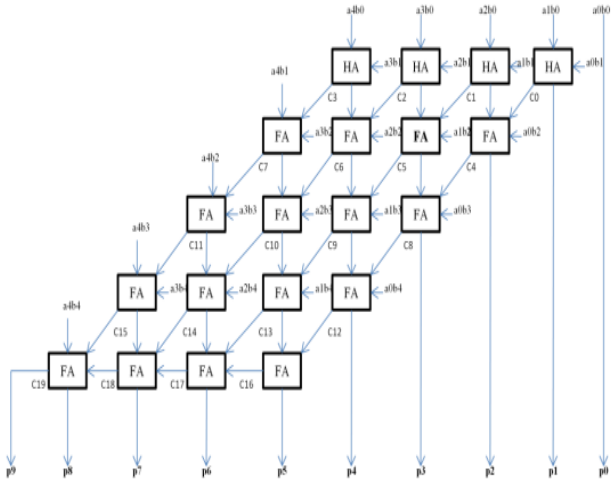

Fig1: Multiplier using half and full adders

Compressor is a modern digital circuit that is utilised for high speed with few gates and necessitates the use of design techniques. This compressor becomes a necessary tool for quick multiplication using a fast CPU and a small area. A compressor is a device that is commonly seen in multipliers and is used to decrease the operands while adding partial product terms. M equally weighted input bits are fed into a conventional M-N compressor, which outputs an N-bit binary integer.

3. 4:2 COMPRESSOR

A compressor is a device that is commonly seen in multipliers and is used to decrease the operands while adding partial product terms. M equally weighted input bits are fed into a conventional M-N compressor, which outputs an N-bit binary integer. The 3-2 compressor, also known as a complete adder, is the most basic and extensively used compressor. It contains three inputs that must be added together and produces two outputs. Similarly, two cascaded 3-2 compressor circuits can be combined to form a 4-2 compressor. As shown in fig. 2.

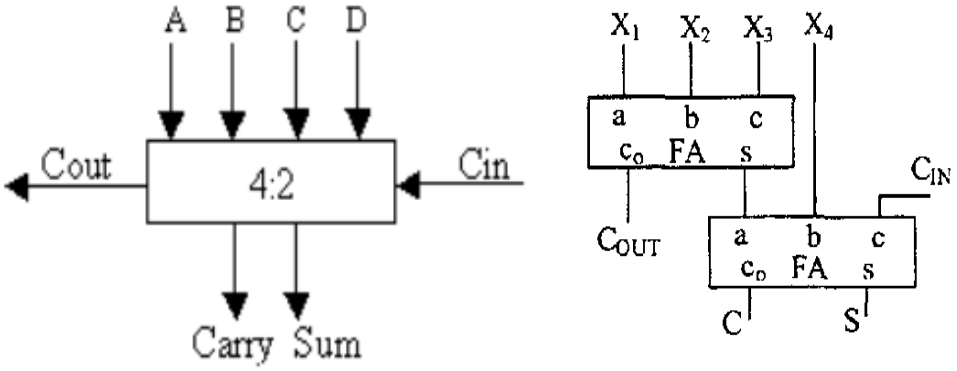

Fig -2: 4:2 compressor

4:2 compressors can add four bits and one carry, resulting in a three-bit output. The 4-2 compressor has four inputs (X1, X2, X3, and X4), two outputs (Sum and Carry), and a Carry-in (Cin) and Carry-out (Cout) (Cout). Cin is the output of the lower significant compressor before it. In the next significant stage, the Cout is the output to the compressor. The traditional implementation of a 4-2 compressor consists of two serially coupled full adders. The ability to add numbers with minimum carry propagation is one of the key speed enhancement strategies utilized in current digital circuits. The essential principle is that in a 3:2 compressor, three numbers can be reduced to two by completing the addition while keeping the carry and total distinct. This means that all of the columns can be added simultaneously without relying on the previous column's result, resulting in a two-output "adder" with a time delay independent of the size of its inputs. To get the right result, recombine the sum and carry in a conventional addition. This method may appear more complicated and unnecessary at first, but the beauty of it is that it can be used to bead any amount or number of additions together. A carry propagating

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 4, April 2022

DOI: 10.17148/IJIREEICE.2022.10418

addition is only required for the final recombination of the final carry and total. Full adder is another name for a 3:2 compressor. Three one-bit binary values, a total, and a carry are added. in most cases, the full adder is part of a cascade of adders. The full adder circuit gets its carry input from the cascade circuit's carry output. The full adder's carry output is sent into another full adder. The 4:2 compressors' features. The outputs are the sum of the five inputs, making it a true 5-bit adder. Both carries have the same weight. Cout's value is solely determined by A, B, C, and D to avoid carry propagation. It is unaffected by Cin. The Cout signal is fed into the Cin of the next column's 4:2. The most popular way to implement a 4-2 compressor is to use two full-adder (FA) cells to add binary values. The 4:2 compressor is made up of two complete adders that are coupled in serial. Instead of using another adder, we employ a compressor adder with little carry propagation. Compressor is a modern digital circuit that is utilised for high speed with few gates and necessitates the use of design techniques. This compressor becomes a necessary tool for quick multiplication using a fast CPU and a small area. A compressor is a device that is commonly seen in multipliers and is used to decrease the operands while adding partial product terms. M equally weighted input bits are fed into a conventional M-N compressor, which outputs an N-bit binary integer. The 3-2 compressor, also known as a complete adder, is the most basic and extensively used compressor. It contains three inputs that must be added together and produces two outputs. Similarly, two Cascaded 3-2 compressor circuits can be combined to form a 4-2 compressor.

4. PROPOSED MULTIPLIER

For NxN multipliers, Dadda developed a calculation with predetermined grouping of network (stage) statures to reduce the number of diminishment stages. It's made by starting over at the two-column stage. Every middle of the road stage is limited in height to a floor estimate of 1.5 times the preceding stage's height. Stage i's stature is equal to (3/2) * stage i+1's height. In AI and DSP applications, multiplication is certainly a performance deciding operation. These applications involve high-speed parallel operations with acceptable levels of accuracy, which necessitate high-speed multiplier designs. The use of approximation in multipliers allows for quicker computations with less hardware complexity, delay, and power consumption, while maintaining acceptable accuracy.

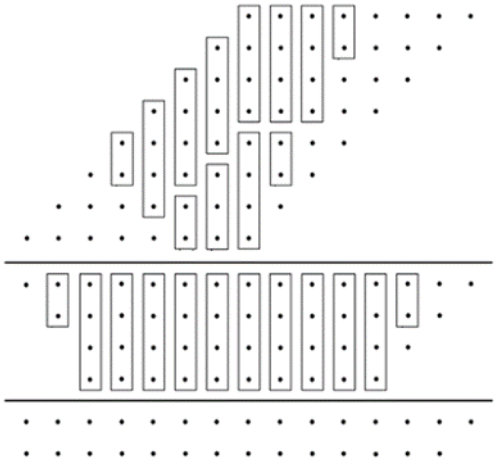

Fig -3: Multiplier using 4:2 compressor

Due to the propagation delay in adder networks, partial product summation is the speed limiting process in multiplication. Compressors are used to shorten the propagation delay. At each level, compressors compute the sum and carry at the same time. In the next stage, the resultant carry is combined with a higher significant sum bit.

Design 1

The gate level structure of the design 1 Fig.4 shows delay is the same as for the exact compressor. However the propagation delay through the gates of this design is lower than the one for the exact compressor. Therefore, the delay in the proposed design is lower than in the exact design and moreover, the total number of gates in the proposed design is significantly less than exact compressor.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
Impact Factor 7.047 ⁜ Vol. 10, Issue 4, April 2022
DOI: 10.17148/IJIREEICE.2022.10418

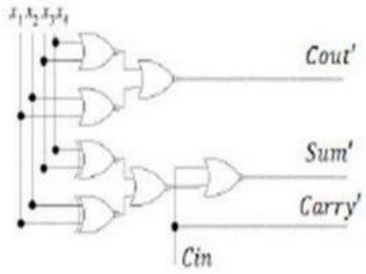

Fig -4: Gate level implementation of design 1

Design 2

The design 2 of an approximate compressor further increase the performance as well as reduces the error rate. Fig5. shows the gate level implementation of design 2 compressor. The delay of this approximate design is less than the design 1 also further reduction in the number of gates is accomplished.

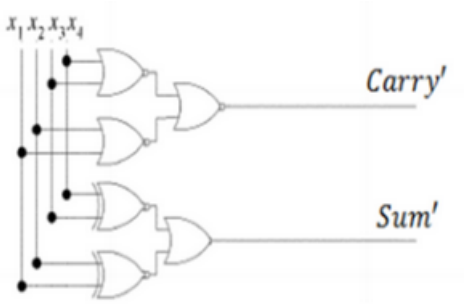

Fig -5: Gate level implementation of design 2

5. RESULT AND ANALYSIS

4-2 compressor is better than other compressor because of its reduced transistor count and power dissipation.

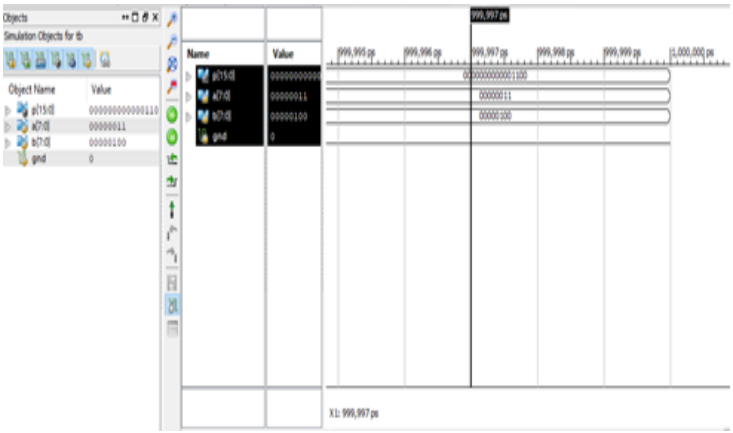

Fig -6: Simulation Output

COMPRESSOR	POWER DISSIPATION (µW)	TRANSISTOR COUNT
Exact design	0.016140	82
Design1	0.010332	44
Design 2	0.010096	42

Fig -7: Analysis of compressor

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

Impact Factor 7.047 ⁜ Vol. 10, Issue 4, April 2022

DOI: 10.17148/IJIREEICE.2022.10418

MULTIPLIER	POWER DISSIPATION (mW)	DELAY
Exact design	9.6566	1.25ns
Design1	5.8186	1.42ns
Design 2	5.5080	84.3ps

Fig -8: Analysis of multiplier

6. CONCLUSIONS

For quick execution, a unique transistors 8x8 multiplier has been demonstrated, which employs 4-2, which are designed with full adders of rapid and low power, as well as a multiplexer. When implementing the dadda algorithm for multiplication, we found that the technique is superior than the 4-2 compressor and the no compressor technique. When compared to Multiplier, the power utilized by a 4-2 compressor based multiplier is lower. For low-power and sophisticated electrical circuits, this compressor approach may be preferred. The 8x8 multiplier demonstrates excellent speed execution as compared to the core Dadda multiplier, both with and without Compressor methods, as well as power usage.

REFERENCES

[1]S. Ghosh, D. Mohapatra, G. Karakonstantis and K. Roy, "Voltage Scalable High-Speed Robust Hybrid Arithmetic Units Using Adaptive Clocking", in IEEE Trans. on Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 9, pp. 1301-1309, Sept. 2010.M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

[2]D. Baran, M. Aktan and V. G. Oklobdzija, "Multiplier structures for low power applications in deep-CMOS," 2011 IEEE Int. Symp. of Circuits and Syst. (ISCAS), Rio de Janeiro, 2011, pp. 1061-1064.K. Elissa, "Title of paper if known," unpublished.

[3]S. Mittal, "A survey of techniques for approximate computing", ACM Comput. Surveys (CSUR), vol. 48, no. 4, p. 62, May 2016.

[4]H. Jiang, C. Liu, L. Liu, F. Lombardi, J. Han, "A review classification and comparative evaluation of approximate arithmetic circuits", ACM J. on Emerg. Tech. in Comput. Syst. (JETC), vol. 13, no. 4, pp. 60, 2017.

[5]J. Liang, J. Han and F. Lombardi, "New Metrics for the Reliability of Approximate and Probabilistic Adders," IEEE Trans. on Comput., vol. 62, no. 9, pp. 1760-1771, Sept. 2013.

[6]R. Zendegani, M. Kamal, M. Bahadori, A. Afzali-Kusha and M. Pedram, "RoBA Multiplier: A Rounding-Based Approximate Multiplier for High- Speed yet Energy-Efficient Digital Signal Processing," in IEEE Trans. On Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 2, pp. 393-401, Feb. 2017.

[7]S. Hashemi, R. Bahar and S Reda, "DRUM: A dynamic range unbiased multiplier for approximate applications,"" Proceedings of the IEEE/ACM Int. Conf. on Comput.-aided design, Austin, Texas, USA, pp. 418-425, 2015.

[8]S. Narayanamoorthy, H. A. Moghaddam, Z. Liu, T. Park and N. S. Kim, "Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications," IEEE Trans. on Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 6, pp. 1180-1184, June 2015.

[9]G. Zervakis, S. Xydis, K. Tsoumanis, D. Soudris and K. Pekmestzi, "Hybrid approximate multiplier architectures for improved power-accuracy trade-offs," 2015 IEEE/ACM Int. Symp. on Low Power Electron. And Design (ISLPED), Rome, 2015, pp. 79-84.

[10]B. Shao and P. Li, "Array-Based Approximate Arithmetic Computing: A General Model and Applications to Multiplier and Squarer Design," IEEE Trans. on Circuits and Syst. I: Reg. Papers, vol. 62, no. 4, pp. 1081-1090, April 2015.

[11]C. Chang, J. Gu and M. Zhang, "Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits," IEEE Trans. on Circuits and Syst. I: Reg. Papers, vol. 51, no. 10, pp. 1985-1997, Oct. 2004.