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A 12-bit High speed Analog to Digital Converter

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Abstract: High resolution analog to digital converters have been based on self–calibrated successive approximation technique. But successive approximation technique ADCs are unsuitable for high speed conversions. Flash converters are popular for high speed applications up to 8-bit resolutions, conversion resolution higher than 8- bits, flash architecture require large number of comparators, hence this architecture is not suitable for high resolution ADCs. In this case, however, this paper demonstrates that, effective combination of successive approximation and parallel quantization techniques have to be used for optimizing the number of comparator requirements while maintaining conversion speed. Such optimization is achieved through a systematic design process. A simple Analog-to-Digital conversion technique, which provides superior conversion speed to that of successive approximation converter, is presented. In this approach, the increased conversion speed is achieved by effective combination of parallel quantization and successive approximation techniques. An 12-bit flash quantizer uses 2^{12}-1 comparators, where as proposed architecture uses only 256 comparators. A successive approximation converter requires 12 comparisons for 12-bit quantization, while proposed technique converts an analog signal into 12-bit equivalent digital code in 12 comparisons. The technique uses less number of comparators while maintaining the speed. Therefore this architecture is best suitable when high speed combined with high resolution is required. Result of 12-bit prototype is presented.

Keyword: Analog to digital converter, digital to analog converter, flash ADC, Microprocessor, Successive approximation.

1. INTRODUCTION

High-Resolution CMOS analog to digital converters (ADC's) with conversion rates in the video range are paramount in modern multimedia communication systems, where increasingly complex processing of analog signals is performed digitally [1]. Typically high-resolution ADC's have been based either on self-calibrated successive approximation [2]-[4] or over sampling architectures [5], but both of these architectures are unsuitable to reach the envisaged speed of conversion compatible with video processing requirements. For video-range ADC's, several designs based on two-step flash and pipelined architectures have been proposed in both CMOS [6] and BiCMOS [7] technologies. Two step flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [8]-[9]. However, beyond such resolution, the area and power dissipation of two-step flash ADC's nearly double for each additional bit of resolution [10].

The conventional pipelined architecture has been widely employed to meet the required performance in this arena[11].Among a variety of pipelined ADC's, the multibit-per stage architecture is more suitable for high resolution. However the multibit-per stage architecture has a relatively low signal processing speed due to reduced feedback factor in the amplifiers.

In this paper a novel analog-to-digital converter architecture is proposed. This architecture is best suitable when high speed combined with high resolution is required. It is based on effective combination of the flash quantization and successive approximation technique. The parallelism of the flash architecture has drawbacks for high resolution applications; the number of comparators grows exponentially with N, where N is stated resolution. In addition, the separation of adjacent reference voltages grows smaller exponentially [12]. Proposed architecture overcomes these two drawbacks. Also, in comparison with fully parallel architectures, proposed technique requires fewer comparators while maintaining the advantage of high speed. It provides superior conversion speed with just twenty nine comparators for 8-bit resolution. This ADC completes conversion in three comparisons, where as conventional successive approximation converter takes eight comparisons for quantization. This makes the quantization feasible with much higher speed then conventional successive approximation technique.

In section II, The and III Flash and SAR ADCs are described. IV, the proposed architecture is discussed and its circuit implementation is described. Prototype ADC results are presented in section V to show the validity of the proposed architecture. Finally, the conclusions are given in section VI.

2. FLASH ADC

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters

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consume considerable power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that typically cannot be addressed any other way. Typical examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.

2.1 Architectural Details

Flash ADCs are made by cascading high-speed comparators. Fig. 1 shows a typical flash ADC block diagram. For an N-bit converter, the circuit employs 2^N -1 comparators. A resistive-divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0. Thus, if the analog input is between VX4 and VX5, comparators X1 through X4 produce 1s and the remaining comparators produce 0s. The point where the code changes from ones to zeros is the point at which the input signal becomes smaller than the respective comparator reference-voltage levels. If the analog input is between VX4 and VX5, comparators X1 through X4 produce 1s and the remaining comparators produce 0s. This architecture is known as thermometer code encoding. This name is used because the design is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code.

The comparators are typically a cascade of wideband low gain stages. They are low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. The comparators are designed for low-voltage offset, so that the input offset of each comparator is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code that is not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a 1 or a 0.

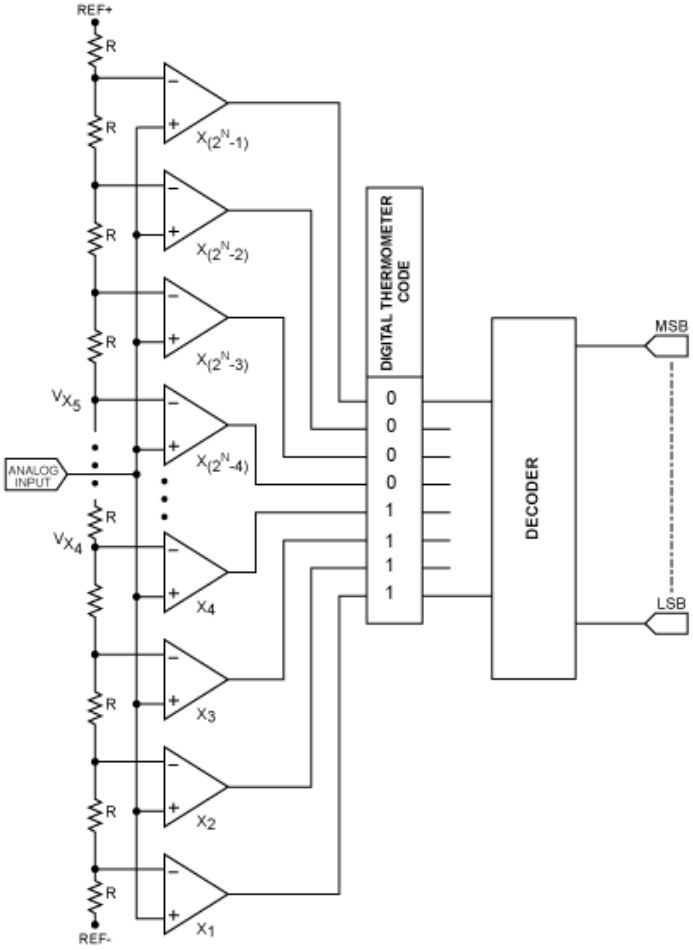

Fig 1. Flash ADC architecture.

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3. SAR ADC

Successive approximation ADCs are widely used for high resolution, medium speed 5MS/s, low-power, low-cost applications such as automotive, factory automation, and pen digitizer applications [13-17]. Successive approximation ADCs with improved performance, lower cost, and higher reliability can make a significant impact in industry.

3.1 Configuration of Successive Approximation ADC

A conventional successive approximation ADC consists of a track-hold circuit, a comparator, a DAC, successive approximation logic and time-base circuits Fig. 2 shows a typical block diagram of successive approximation ADC. The track-hold circuit, and ensuring linearity of DAC input output characteristics, is the most critical parts of the design. Usually a ring counter is used in the time-base circuitry to provide accurate timing signals.

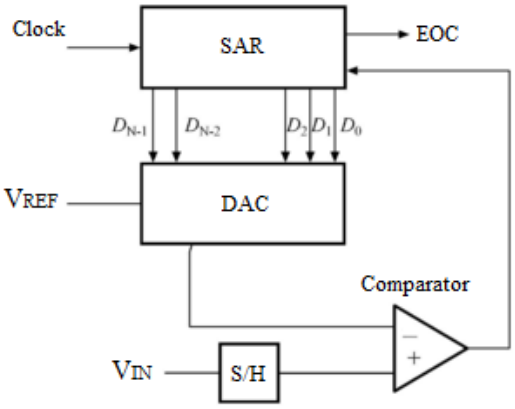

Fig 2. Block diagram of SAR ADC

3.2 Operation Of Successive Approximation ADC

The successive approximation ADC operates according to a binary search algorithm as follows: The track-hold circuit samples and holds the voltage of the analog input Vin (full-scale input is Vref).The comparator compares the voltages of Vin (held by the track-hold circuit) and Vref /2 (where Vref /2 is generated by the DAC).In case Vin >Vref/2: The comparator outputs logic ”1”.The comparator then compares the voltage Vin with (3/4)Vref (where (3/4)Vref is generated by the DAC).If Vin > (3/4)Vref, then (7/8)Vref is used for the next comparison. Else if Vin < (3/4)Vref, then (5/8)Vref is used. This binary search continues in this manner. In case Vin<Vref /2: The comparator outputs logic”0”.The comparator then compares the voltages Vin with (1/4)Vref (where (1/4)Vref is generated by the DAC).If Vin > (1/4)Vref, then (3/8)Vref is used for the next comparison. Else if Vin < (1/4)Vref, then (1/8)Vref is used. The successive approximation ADC performs N comparisons, then outputs a digital value corresponding to the N-bit binary comparison result.

4. PROPOSED ADC ARCHITECTURE

The block diagram of the proposed 12-bit ADC is illustrated in Figure-3. It is based on a conventional successive approximation technique. The ADC consists of an input sample and hold amplifier (SHA), 8-bit flash ADC, 12-bit DAC, 8-bit µP 8085 and some extra supporting circuit blocks. 8-bit flash ADC partitions input range into 256-quantization cells. From the 8-bit code µP8085 decides within which cell the input sample lies. This gives 8 MSB bits 00000000 to 11111111 according to the cell value. Remaining 4 bits are obtained by successive approximation technique.

The Analog to digital converter is designed and developed using µP8085. The 8-bit code generated by 8-bit flash ADC is fed to Port A of 8255. Depending on the code value, a binary count is loaded in Register A. The successive approximation technique is used to get a final 12-bit digital code for the analog input signal.

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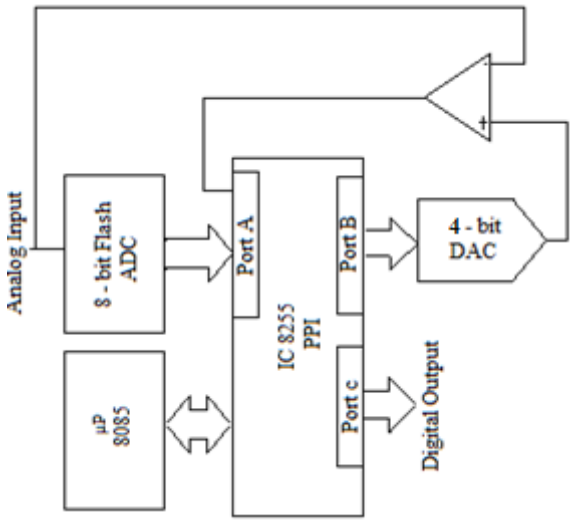

Fig 3. Block diagram of 12-bit ADC

4.1 Circuit Implementation

The block diagram of the 12-bit ADC is as shown in Fig. 3. The Microprocessor port A is used as input port, which gets the 8-bit code from 8-bit flash ADC, corresponding center value 12-bit binary code of a particular cell is loaded into the accumulator. Port B is used as output port, connected to 12-bit DAC to obtain analog signal equivalent to digital count in register A, which is compared with an analog input voltage VIN. Equivalent 12-bit digital code for analog input signal is obtained by successive approximation technique. The conversion algorithm is similar to the binary search algorithm. First, the reference voltage of a particular cell, Vref (DAC) provided by DAC is set to VN / 2 to obtain the MSB, where VN is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with VN/4 or 3/4*VN depending on the result of the MSB. If the MSB is "1", then Vref (DAC) = ¾*VN, otherwise Vref (DAC) =VN/4. This sequence will continue until the LSB is obtained. To get a 12-bit digital output, 12 comparisons are needed. Finally 12-bit digital code is available at Port C software for implementing successive approximation converter in Microprocessor is written in assembler code and converted to hex code by assembler software. Hex codes are transferred to Microprocessor by programmer.

5. MEASURED RESULT

An experimental prototype of 12-bit ADC using proposed technique was designed and developed using µP8085. The working functionality of the ADC has been checked by applying a ramp input going from 0 to 3.5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 2^{12} for 12-bit at the output, indicating that the ADC's working is functionally correct. Both the differential and integral nonlinearities (DNL and INL) were measured over 2^{12} output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 2^{12}- 1 steps .The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.49LSB and a maximum INL of 0.51LSB as shown in the Figs. 4(a) and 4(b).

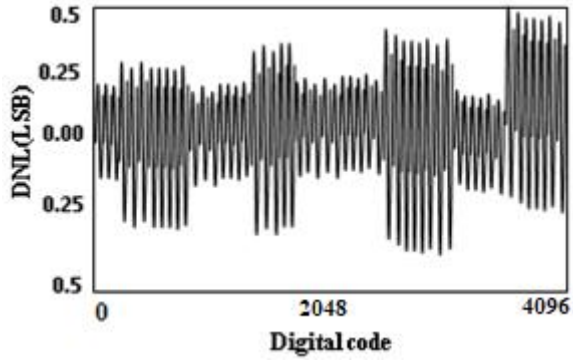

Fig 4(A). DNL Versus output code

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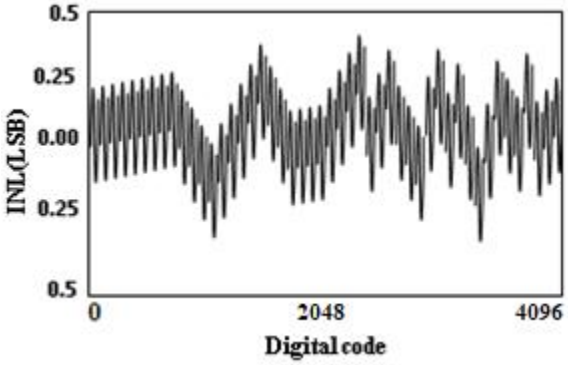

Fig 4(b): INL Versus output Code

CONCLUSION

We have presented a simple and effective technique for enhancing speed of 12-bit SAR ADC. This technique would be effective in a large number of high speed controls and signal processing applications such as hard disk- drive read Chanel and wireless receivers. Although, these applications are most often implemented with flash convertors but these ADC's demands larger power. And also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10-bits. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10-bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high speed applications, with less power dissipation even beyond 12-bit resolution. Implementation of successive approximation algorithm using Microprocessor has reduced the hardware requirement and cost. Proposed technique uses only 256 comparators for 12-bit resolution.

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