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A 9-bit Successive Approximation Analog to Digital Converter Using µp 8085

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Abstract: An Hybrid technique to the circuit implementation of 9-bit analog-to-digital (ADC) converter is proposed, This method demonstrates a simple technique to increase speed of successive approximation ADC's that require as few as 4 comparisons for 9 bit conversion. This technique doubles the conversion speed of conventional successive approximation technique. The approach divides input range into 32-quantization cells, separated by 31 boundary points. A 5-bit binary code 00000 to 11111 is assigned to each cell. A normal successive approximation converter requires 9 comparisons for 9-bit quantization, while proposed technique reduces number of comparison requirements to 4 comparisons. An experimental prototype of 9-bit ADC using proposed technique was implemented using µp 8085. Use of Microprocessor has greatly reduced the hardware requirement and cost. This technique is best suitable when high speed combined with high resolution is required. The ADC Results of 10-bit prototype is presented. The results show that the ADC exhibits a maximum DNL of 0.47LSB and a maximum INL of 0.5LSB.

Keyword: Analog to digital converter, digital to analog converter, flash ADC, Microprocessor, Successive approximation.

1. INTRODUCTION

Analog-to-digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses 2^N-1 comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions. All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially and consequently this architecture requires very large IC's. It has high power dissipation. The conventional pipelined architecture has been widely employed to meet the required performance in this arena due to properly managed trade-offs between speed, power consumption and die area [2]. Among a variety of pipelined ADCs, the multi bit-per-stage architecture is more suitable for high resolution, as the single bit- per stage structure requires more stages, high power consumption and larger chip area. However the multi bit-per-stage architecture has a relatively low signal processing speed due to reduced feedback factor in the closed – loop configuration of the amplifiers. In switched capacitor type multiplying digital-to-analog converters (MDACS) used in conventional pipelined ADCs, the mismatch between capacitors limits the differential nonlinearly (DNL) of ADCs. This is because each DNL step is defined by the random process variation of each unit capacitor value. A common centroid geometry layout technique can improve this capacitor matching for DNL, but it cannot have an effect on random mismatch. Naturally, increasing the capacitor size can directly improve the capacitor matching accuracy, but at the added cost of increased load capacitance. This means the amplifiers would dissipate more power or the ADC sampling speed would have to be reduced. Two step Flash converters are popular for conversion resolutions in the 8-10 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [3]. However, beyond such resolution, the area and power dissipation of two-step flash ADC's nearly double for each additional bit of resolution [4]. There are many different architectures like pipelined convertor, successive approximation convertor, Sigma-Delta convertor, folding ADC's [5], reported recently for high speed applications. But these architectures have significant amount of complexity.

High-Resolution CMOS analog to digital converters (ADC's) with conversion rates in the video range are paramount in modern multimedia communication systems, where increasingly complex processing of analog signals is performed digitally [6]. Typically high-resolution ADC's have been based either on self-calibrated successive approximation [7]-[9] or over sampling architectures [10], but both of these architectures are unsuitable to reach the envisaged speed of conversion compatible with video processing requirements. For video-range ADC's, several designs based on two-step flash and pipelined architectures have been proposed in both CMOS [11] and BiCMOS [12] technologies. Two step flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power

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dissipation and small silicon area for implementation [13]-[14]. However, beyond such resolution, the area and power dissipation of two-step flash ADC's nearly double for each additional bit of resolution [15].

The conventional pipelined architecture has been widely employed to meet the required performance in this arena[16].Among a variety of pipelined ADC's, the multibit-per stage architecture is more suitable for high resolution. However the multibit-per stage architecture has a relatively low signal processing speed due to reduced feedback factor in the amplifiers.

In this paper a simple hybrid technique for the circuit implementation of 10-bit analog-to-digital (ADC) converter is proposed, This method demonstrates a simple technique to increase speed of successive approximation ADC's that require as few as 4 comparisons for 9 bit conversion.

2. FLASH ADC

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters consume considerable power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that typically cannot be addressed any other way. Typical examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.

3. SAR ADC

SAR ADCs are widely used for high resolution 10-12 bit, medium speed 5MS/s, low-power, low-cost applications such as automotive, factory automation, and pen digitizer applications [17]. SAR ADCs with improved performance, lower cost, and higher reliability can make a significant impact in industry. A conventional successive approximation ADC consists of a track-hold circuit, a comparator, a DAC, successive approximation logic and time-base circuits. The track-hold circuit, and ensuring linearity of DAC input output characteristics, is the most critical parts of the design. Usually a ring counter is used in the time-base circuitry to provide accurate timing signals. The successive approximation ADC operates according to a binary search algorithm as follows: The track-hold circuit samples and holds the voltage of the analog input Vin (full-scale input is Vref).The comparator compares the voltages of Vin (held by the track-hold circuit) and Vref /2 (where Vref /2 is generated by the DAC). In case Vin >Vref/2:The comparator outputs logic "1".The comparator then compares the voltage Vin with (3/4)Vref (where (3/4)Vref is generated by the DAC).If Vin > (3/4)Vref, then (7/8)Vref is used for the next comparison. Else if Vin < (3/4)Vref, then (5/8)Vref is used. This binary search continues in this manner. In case Vin<Vref/2: The comparator outputs logic "0". The comparator then compares the voltages Vin with (1/4)Vref (where (1/4)Vref is generated by the DAC). If Vin > (1/4)Vref, then (3/8)Vref is used for the next comparison. Else if Vin < (1/4)Vref, then (1/8)Vref is used. The successive approximation ADC performs N comparisons, then outputs a digital value corresponding to the N-bit binary comparison result.

4. PROPOSED ADC ARCHITECTURE

Flash ADC's are promising for high Speed applications. However, these ADC's are unsuitable for high resolution applications. The number of comparators grows exponentially with resolution, and consequently this architecture requires very large IC's and it has high power dissipation. The ADC based on our technique enjoys the benefit of employing only 32 comparators instead of 511 comparators normally required in conventional 9-bit flash architecture while maintaining the advantage of high speed. The block diagram of the 9-bit ADC using proposed technique is illustrated in Figure 1. The ADC consists of an input sample and hold amplifier (SHA), 5-bit flash ADC, 10-bit DAC, 8-bit µp 8085, 8:16 bit MUX/DEMUX switch and some extra supporting circuit blocks. 5-bit flash ADC, partitions input range into 32-quantization cells, separated by 31 boundary points. A 5-bit binary code 00000 to 11111 is assigned to each cell. The µp 8085 decides within which cell the input sample lies and assigns a 9-bit binary center code 000000000 to 111111111 according to the cell value. The exact 9-bit digital code for analog sample is obtained by successive approximation technique.

The block diagram of the 9-bit ADC is as shown in Figure 1. The µp port C is used as input port, which gets the 5-bit code from 5-bit flash ADC, corresponding center value 9-bit binary code of a particular cell is loaded into the accumulator. Port A is used as output port, connected to 9-bit DAC through 8:16 bit switch to obtain analog signal equivalent to digital count in register A, which is compared with an analog input voltage Vs. Equivalent 9-bit digital code for analog input signal is obtained by successive approximation technique.

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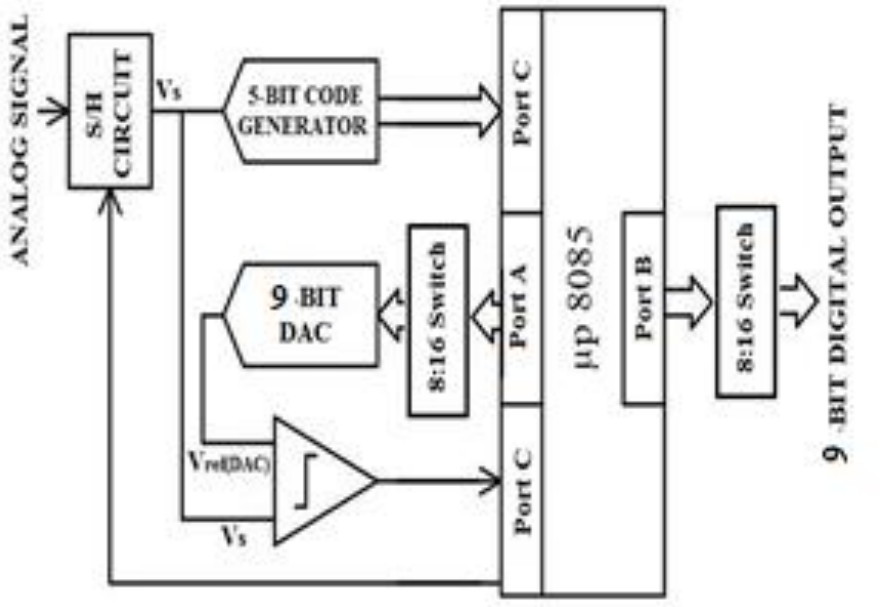

Fig 1. Block diagram of 9-bit ADC

5. MEASURED RESULT

An experimental prototype of 9-bit ADC using proposed technique was designed and developed using µP 8085. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 512 for 9 bits at the output, indicating that the ADCs working is functionally correct. Both the DNL and INL were measured over 2^9 output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 512 steps. The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.47 LSB and a maximum INL of 0.5 LSB as shown in the Fig. 2(a) and 2(b).

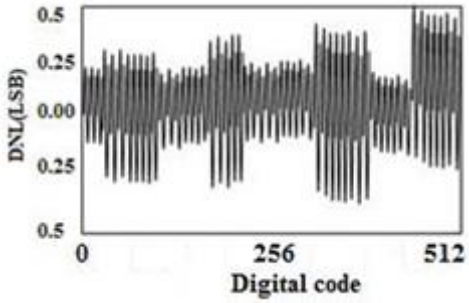

Fig 2(a). Differential Non Linearity.

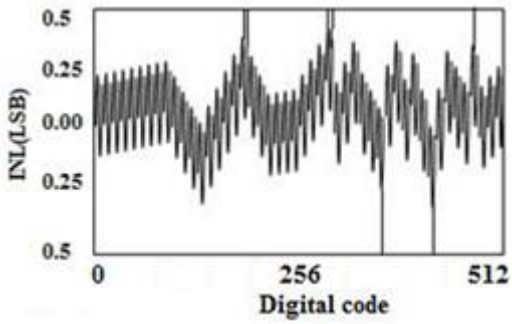

Fig 2(b). Integral Non Linearity.

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CONCLUSION

We have designed and developed a high performance SAR ADC architecture that achieves both high speed and high reliability ideal for automotive, high speed controls and signal processing applications such as hard-disk-drive read channel wireless receivers and digital audio applications etc. ADC results of 9-bit prototype are presented. Implementation of SAR algorithm in µP 8085 has reduced the hardware requirement and cost. We further plan to implement this architecture and algorithm efficiently on an IC.

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