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DESIGN AND ANALYSIS OF MEMRISTOR BASED 7T SRAM USING LEAKAGEREDUCTION TECHNIQUES

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Abstract: In today's world demand of low power devices is increasing and the reason behind this is scaling of CMOS technology. Due to the scaling, size of the chip decreases and number of transistor in system on chip (SOC) increases and this phenomenon also apply on memories that are used in SOC. Memories are the power hungry devices in any digital system but today no digital system can be completed without memories. However, the transistor miniaturization also introduces many new challenges in very large-scale integrated (VLSI) circuit design. So in future the need of low power memories is increasing and to design low power memories leakage power is attentive parameter to design low power devices because it plays a major role in increasing the total power consumption of the devices.
In this project, Dual Sleep technique is used recently it is very famous in academia and industry. It is a power reducing technique that helps in reducing leakage power in the SRAM by turning of the inactive circuit domains. Designing and calculation of parameters of simple SRAM, Memristor based SRAM and Dual Sleep based Memristor SRAM has been done with CMOS Design tool and that will do at 45 nm technology.

keywords: Low power, Speed, SRAM, Non Volitle Memory, CMOS, Memristor, MTCMOS, Dual Sleep.

I.INTRODUCTION:

Since the invention of the first Integrated Circuit (IC), silicon technology scaling down continues to meet the increasing demands for higher functionality and better performance at a lower cost. The advances in VLSI integration technology have made it possible to put a complete System on a Chip (SoC) which facilitates the development of portable systems. The growing demand for VLSI circuits the leakage current on the oxide thickness is becoming a major challenge in deep-sub-micron CMOS technology. In deep submicron technologies, leakage power becomes a key for a low power design due to its ever increasing proportion in chip's total power consumption. Motivated by emerging battery-operated application on one hand and shrinking technology of deep sub micron on the other hand, leakage power dissipation is playing a significant role in the total power dissipation as threshold voltage becomes low. Due to the trade-off between power, area and performance, various efforts have been done. So the low power devices are the first choice of VLSI designers and these low power devices fulfill the goal of the systems. The value of power that can be dissipated from the power supply mathematically is represented as-

Where is average power, T is time, I is current

$$P_{av} = \left[\left(\frac{1}{T}\right)\int_0^T Idt\right] \times V$$

and V is voltage. In future demand of battery operated portable systems in electronic field increases such as mobile phones, laptops, notebook computers, Personal Digital Assistants (PDAs), military equipments and other handheld devices in electronic field Low power system and these systems to store their data use memories.

The computer memory system has both volatile and non volatile memory. The Volatile memories such as SRAM and DRAM used as a main memory and non volatile memory like flash memory. But in recent days new non volatile technologies are invented that promise the rapid changes in the landscape of memory systems. In DRAM each memory cell holds one bit of information and is made up of two parts: a transistor and a capacitor. Transistor acts as a switch.

The capacitor can be either charged or discharged. These two states are 0 and 1. It stores each bit of data in a separate capacitor within IC. It has to be dynamically refreshed all of the time. In SRAM flip-flop holds each bit of memory. Flip-flop for a memory cell takes 4 or 6 transistors along with some wiring but never has to be refreshed. SRAM and DRAM holds data in different ways. SRAM can read and write data faster than DRAM. SRAM consumes less power than DRAM. The main reason to use SRAM is its speed advantage over the main memory that uses DRAM. Now a day the aggressive

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scaling of the transistor size drastically affects SRAM devices, which are widely used in many digital chips such as cache and so on. In SRAM cell does not need refreshing technique and it is volatile in nature that means when power is plugged in, data is stored and as the power is plugged out data will get lost other qualities of SRAM is it use number of transistors to store a single bit in system on chip (SOC) and it reduces the delay between the processor and memories. These advantages of SRAM are used to design portable systems that is why low power SRAM is very demand full in handheld devices.

Memristor was invented by Leon O. Chua in 1971 and according to Chua Memristor is a fourth non-linear passive two terminal electrical component with variable resistance also called as memristance that give relation between flux (Φm) and charge (q) in which the magnetic flux (Φm) between the terminals is a function of the amount of electric charge q that has passed through the device and it is denoted by M and its unit is Ω and mathematically represented as-

$$M(q) = \frac{d\varphi m}{dq}$$

Where M is the Memristor, Φm is the magnetic flux and q is the charge. First Memristor was manufactured in HP labs by the R. Stanley Williamsin 2008. Memristor is a new type of device that can be used to design memristive system, devices and memories. Resistance of memristor depends on the magnitude and polarity of the voltage applied to it. It has nonlinear relationship between voltages and current which is similar to memory devices. Using the Memristor technique in simple SRAM reduces the total power and leakage power.

In this paper also apply MTCMOS technique on Memristor based SRAM it is a power switch and an effective circuit-level technique. It is a variation of CMOS chip technology which has transistors with multiple threshold voltages (Vth) in order to optimize delay or power. It uses sleep transistors which improves the speed of the devices and decrease the power remarkable. It is a power reducing technique that helps in reducing leakage power in the SRAM during standby mode and attains high speed in active mode. Therefore in this paper designed MTCMOS based Memristor SRAM. Memristor and MTCMOS have been used to designed low power SRAM.

II.LITERATURE REVIEW

Thangamani.V [2] presented by the approach to design memristor based nonvolatile 6-T static random access memory (SRAM) and analysis the circuit performance with conventional 6-T SRAM cell in order to prove the parameter optimizations. Then we address the memristor-based resistive random access memory (MRRAM) which is similar to that of static random access memory (SRAM) cell and we compare the nonvolatile characteristics of MRRAM with SRAM cell.

Uma Nirmal, Geetanjali Sharma, Yogesh Sharma [3] presented by the main objective is to provide new low power solution for Very Large Scale Integration (VLSI) designers. MTCMOS is an effective circuit-level technique that provides a high performance and low-power design by utilizing both low and high-threshold voltage transistors. MTCMOS technique has been proposed in this paper and the proposed technique has small power dissipation as compared to CMOS technique. Simulations based on BSIM 3V3 180nm CMOS technology. It shows 4 bit adders of the proposed technique have low power dissipation as compared CMOS technique.

Mika Kutila, Ari Paasio and Teijo Lehtonen [6] presented by the 8T SRAM and 6T SRAM memory cells are compared in order to establish guidelines for choosing SRAM cell constructions for NTC systems. 8T SRAM is traditionally concerned as a more reliable memory cell, but we have managed to design 6T SRAM which executes read operation with an acceptaple reliability; read being the most vulnerable operation of conventional 6T SRAM cell. Also, our 6T SRAM cell has 31% smaller area and smaller power consumption.

Amit Grover [8] presented by the motivation of reduction of the dynamic power in SRAM memory and focuses on the analysis in terms of power dissipation, delay and area of the 7- transistor SRAM memory cell at 90 nm technologies by using the Tanner tool. The article targets towards short circuit power dissipation as well as switching power dissipation. The circuit is characterized by using the 90 nm technology which is having a supply voltage of 1.0 volts and threshold voltage is 0.3 volts.

III.IMPLEMENTATION 6T SRAM

The static RAM is a very important class of memory. It consists of two cross-coupled inverters, which form a positive feedback with two possible states. Fig.1. shows the conventional SRAM cell. Word line is used for enabling the access transistors N1 and N4 for write operation. BL and ~BL lines are used to store the data and its compliment. Both the bit lines (BL and ~BL) are used to transfer the data during the read and write operations in a differential manner. To have

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better noise margin, the data signal and its inverse is provided to BL and ~BL respectively. For write operation one BL is High and the other bit line remain in low condition. It uses six transistors in Fig 1. to store and access one bit. The four transistors in the centre form two cross-coupled inverters. It has 2 pull up PMOS and 2 NMOS pull down transistors as two cross coupled inverters and two 2 NMOS access transistors to access the SRAM cell during Read and Write operations.

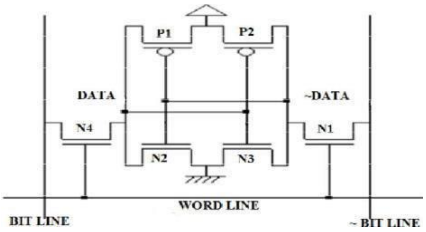
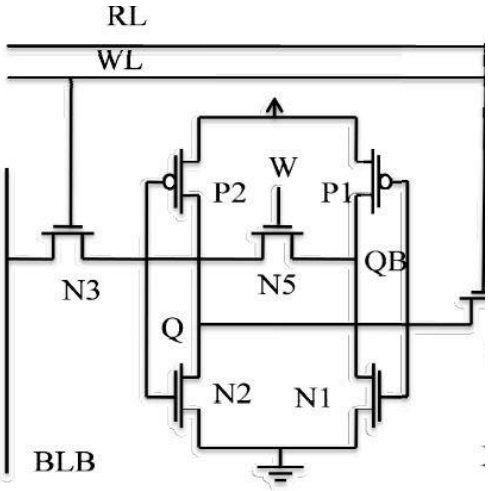


Fig1.6T SRAM

7T SRAM:

7T SRAM has been designed and parameters like total power and leakage power has been calculated. SRAM (Static Random Access Memory) is a type of memory that provide a link with CPU and designing of SRAM is very critical because it takes large part of power and area therefore to achieve low power SRAM we have designed Memristor based SRAM. Memristor is a forth missing non-linear resistor which acts as memory and it improves the power and speed



Memristor based SRAM

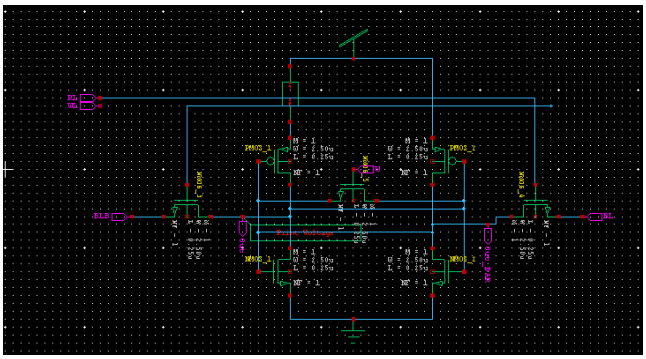


Fig. 2 Memristor based SRAM

Memristor works as a switch like transistor except that Memristor is a two terminal device while transistor is a three terminal device. Memristor is manufactured by two thin layers and these layers are sandwiched between platinum nano-wires and layers are also in nanometer size. These layers are of doped TiO2- x and another is undoped TiO2. Change in resistance occurs in these layer because one TiO2 layers receives oxygen ions and other TiO2 layer losses the oxygen

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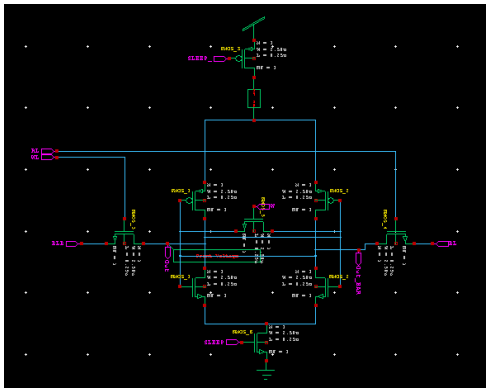
ions i.e. movement of mobile ionic charge inside the TiO2 layer result in change in Memristor resistance. That is why it is called variable resistance and it is used in designing of memories. This is the reason that Memristor can help in reducing total power in the Memristor based SRAM. In this paper, Memristor based 7T SRAM has been designed. Fig3. Shows the Memristor based 7T SRAM cell. Memristor M1 is connected between Vdd supply and at centre point of 2 PMOS transistor. Using the Memristor technique in simple SRAM reduces the total power and leakage power.

MTCMOS

MTCMOS is a power reducing technique that helps in reducing leakage power in the SRAM. The multi threshold CMOS technology has two main features. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. This technique based on disconnecting the low threshold voltage (low- Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as "power gating". The Memristor based SRAM using MTCMOS is shown in Fig 4. The transistors having low threshold



voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation. MTCMOS(multithreshold CMOS) reduces leakage current during standby mode and attains high speed in active mode.

Fig3.Memristor based 7T SRAM using MTCMOS

IV. PROPOSED DUAL SLEEP

However, area requirement is max for this technique since every transistor is replaced by three transistors. Dual sleep Technique[8] is (Fig:5) uses the advantage of using the two extra pull- up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common. For a certain logic circuit less number of transistors are enough to apply.

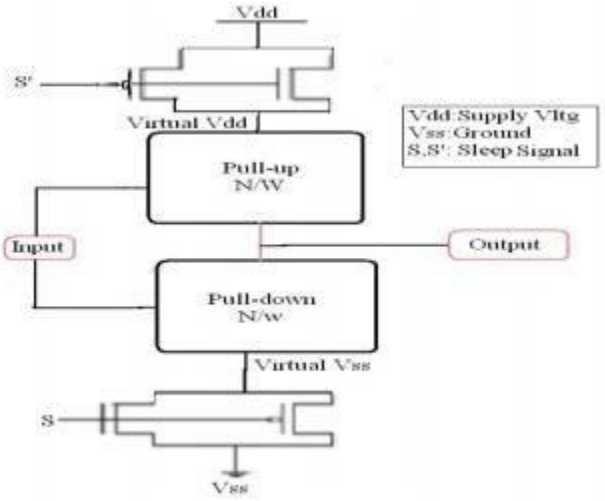


Fig5: Dual Sleep Technique

The method is dual stack approach [1], in sleep mode, the sleep transistors are off, i.e. transistor N1 andP1 are off. We

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do so by making S=0 and hence S'=1. Now we see that the other 4 transistors P2, P3 and N2, N3 connect the main circuit with power rail. Here we use 2 PMOS in the pull down network and 2 NMOS in the pull- up network. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit.

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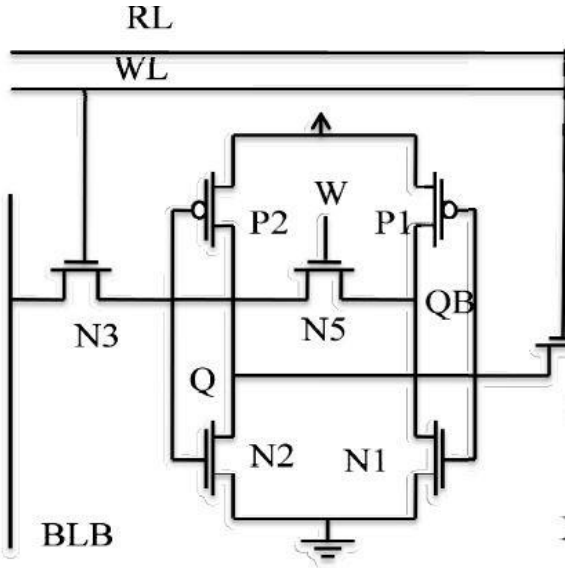

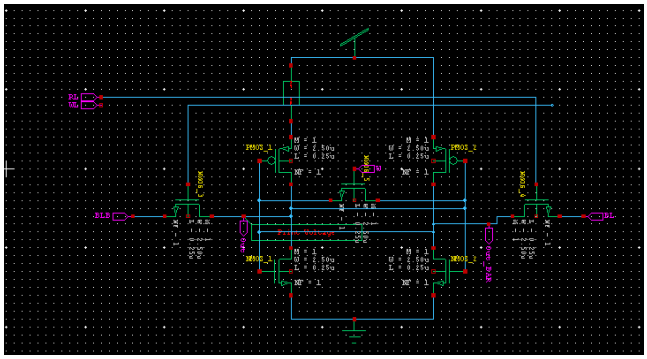

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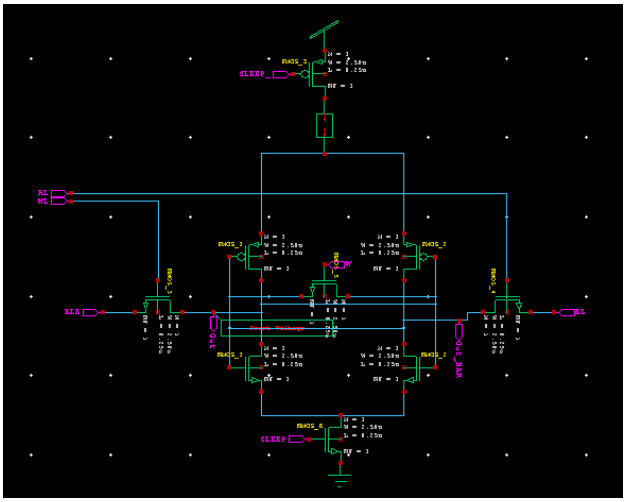

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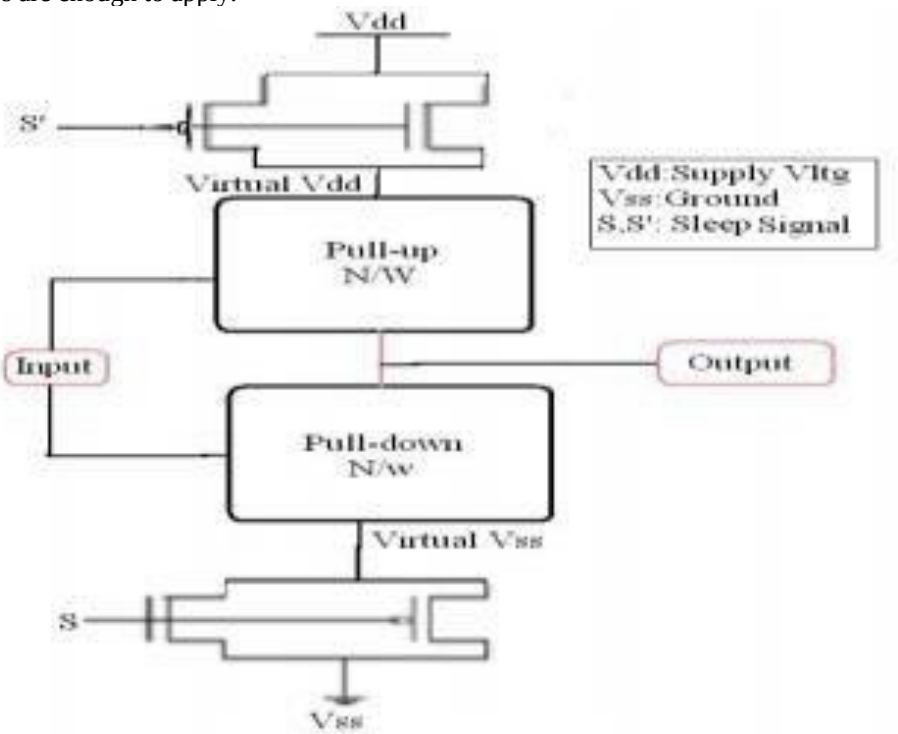

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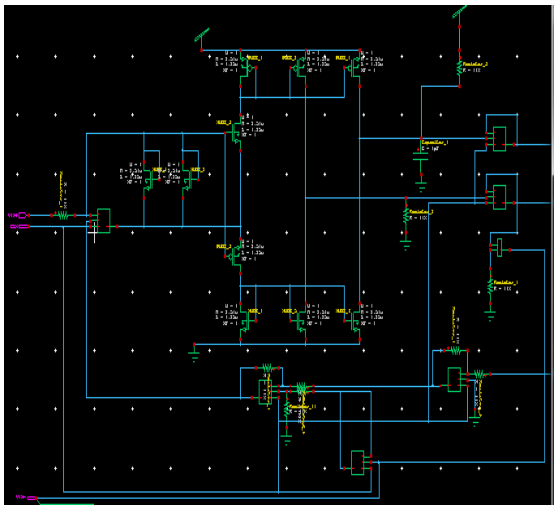
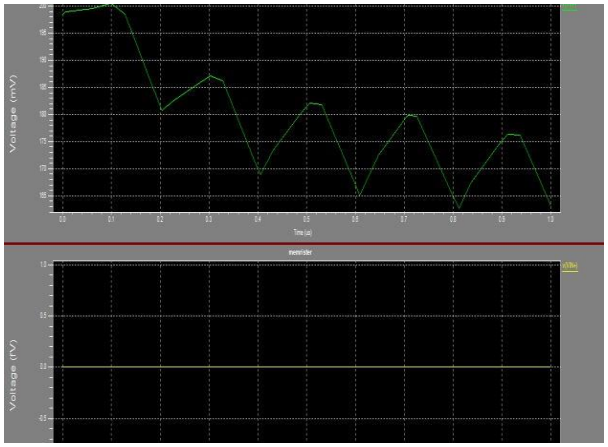
V. SIMULATION RESULTS:

Memristor Circuit

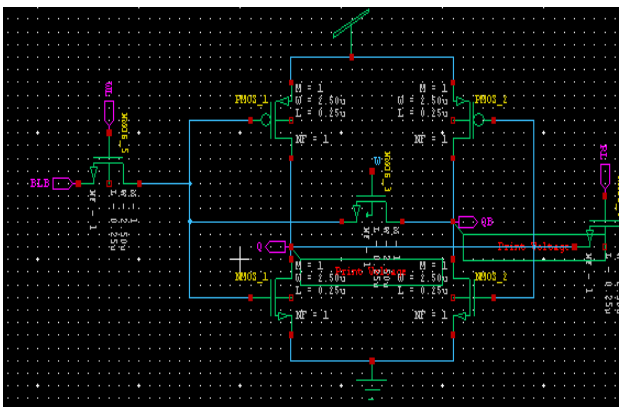


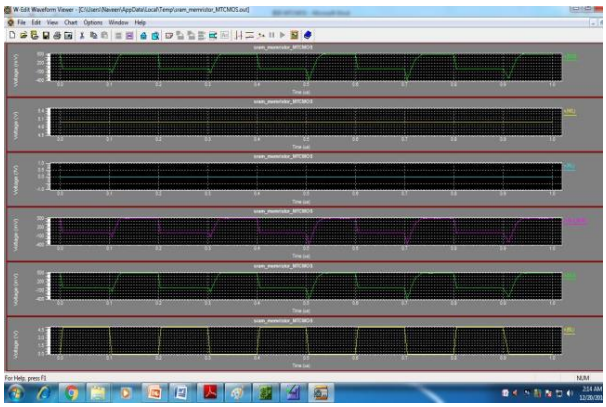
Waveform of Memristor:



7T SRAM:

Waveform of 7T SRAM:





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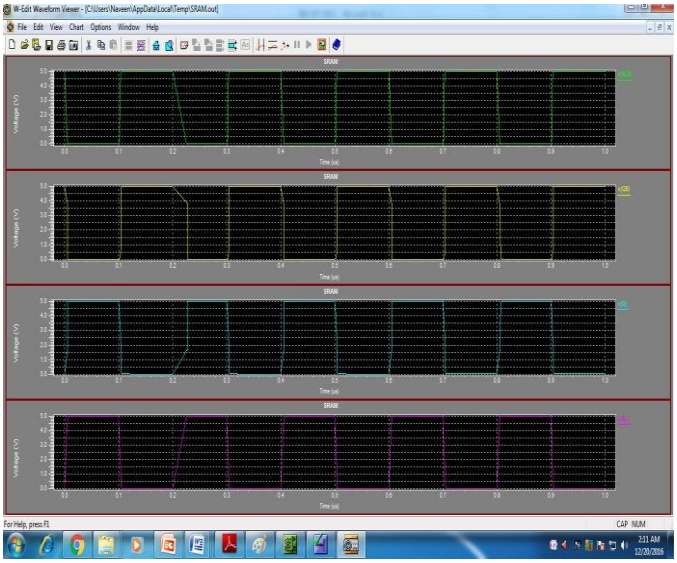
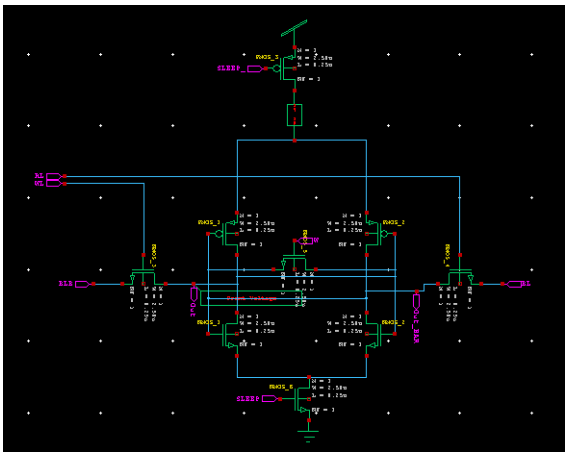


MEMRISTOR BASED 7T SRAM USING MTC

Power Results:

7T SRAM	4.095348e-003 watts
7T SRAM using Memristor	3.773604e-003 watts
7T SRAM using MTCMOS	5.860291e-007 watts



VI.CONCLUSION:

Sub threshold leakage power consumption is a great challenge in nano-meter scale (CMOS) technology, although previous techniques are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, based upon technology & design criteria the designers can choose the techniques. In this paper, we provide novel circuit structure in terms of static & dynamic powers named as "Power gated sleep method" it's a new remedy for designers. This technique shows the least speed power product among all techniques. The Proposed technique achieving ultra-low leakage power consumption with much less speed, especially it shows nearly 50-60% of power than the existing. So, it can be used for future IC'S for area & power Efficiency.

REFERENCE

1. Vijay Singh Baghel and Shyam Akashe, "Low power Memristor Based 7T SRAM Using MTCMOSTechnique," IEEE, Fifth International Conference on Advanced Computing & Communication Technologies in MP,India, 2015.
2. Thangamani.V, "Memristor-Based Resistive Random Access Memory: Hybrid Architecture for Low PowerCompact Memory Design," IISTE, Control Theory and Informatics ISSN 2224-5774 (Paper) ISSN 2225-0492 (Online) Vol.4, No.7, 2014.
3. Uma Nirmal, Geetanjali Sharma, Yogesh Sharma, "A Low Power High Speed Adders using MTCMOS Technique,"JOURNAL OF ELECTRONIC SCIENCE AND TECHNOLOGY12, NO. 2, JUNE 2014. Nobuaki Kobayashi, Ryusuke Ito and Tadayoshi Enomoto, "A High Stability, Low Supply Voltage and Low Standby Power

DOI: 10.17148/IJIREEICE.2022.10230

Six-Transistor CMOS SRAM," IEEE 978-1-4799-7792-5/15/$31.00 ©2015

4. Farshad Moradi and Jens K. Madsen, "Robust Subthreshold 7T-SRAM Cell for Low-Power Applications," IEEE,2014.
5. Mika Kutila, Ari Paasio and Teijo Lehtonen, "Comparison of 130 nm Technology 6T and 8T SRAM Cell Designs for Near-Threshold Operation," IEEE ,978- 1-4799-4132-2/14/$31.00 ©2014
6. G.-F. Wang, W. Kang, Y.-Q. Cheng, J. Nan, J.-O. Klein, Y.-G. Zhang, and W.-S. Zhao, "Low ower Computing Paradigms Based on Emerging Non-Volatile Nanodevi