



VLSI IMPLEMENTATION FOR VIDEO COMPRESSION

D V Manjunatha¹, K Gaurav Shet², Jayasoorya³, Yashwanth V⁴, Sampath N M⁵

¹Senior Professor and HOD, Dept. Of ECE, Alva's Institute of Engineering and Technology, Moodbidri, Karnataka

^{2,3,4,5}Students, Department of Electronics and Communication Engineering,
Alva's Institute of Engineering And Technology, Moodbidri, Karnataka

Abstract: Visual communications are evolving rapidly for media, telecommunications, and computing industries. The availability of digital media and transmission sources has led to significant progress in this field. In addition, workstations and personal computers are widely used platforms for interactive multimedia applications. Recent developments in image displays, digital storage, computing, and communication channels have made digital audio and video the very popular media sources which are economically viable as well. Several video compression schemes are used to cut down storage and transmission cost. To improve universal interchange of audio-visual data, there is a great demand for international standards for transmission and coding formats. In VLSI technology, recent advancements have come as a boon to fulfill high video coding requirements and hardware issues. This paper suggests three most important architectural approaches for VLSI implementation and suggests the most popular and widely used algorithms for video compression.

Keywords: VLSI implementation, VLSI video compression, VLSI technology

I. INTRODUCTION

In the Very Large Scale Integration or VLSI process, thousands of transistors are combined in one integrated circuit (IC) chip. In the 1970s, complex communication and semiconductor devices were being developed when the development of VLSI was started. Before the arrival of VLSI technology, a lot of IC chips had limited functions to conduct. An electronic circuit might have a ROM, CPU, RAM and some glue. IC designers can insert all these components in a single chip with VLSI process. Over the past few decades, electronics have come a long way, especially because of significant advances in system design applications and huge scale integration systems. With the advancement of VLSI, the number of applications of IC chips in controls, high performance computing, video and image processing, telecommunications, and consumer electronics. The modern technologies like low bit-rate video, high resolution and cellular networks provide a lot of applications, portability, and processing power to the users. This trend is all set to grow significantly with implications on system design and VLSI design. Figure 1 illustrates the design flow of VLSI IC circuits. The blocks represent the several design levels in the design flow –

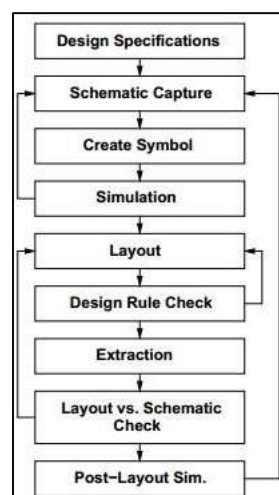


Fig. 1 – VLSI Design Flow



Design Specifications are the first step which describes the functionality, architecture, and interface of the IC chip abstractly. Later on, behavioral description is formed to analyze design with performance, functionality, compliance, and other configurations.

The HDLs are used for RTL description. Its simulation is done to check its functionality. EDA Tools are then used. Then, logic synthesis tools convert RTL description to gate-level netlist, which is a circuit description in terms of connectivity and gates among them, which are made to meet the power, timing, and area specifications. A physical layout is finally made to be verified and sent for fabrication.

Video compression can cut down the number of bits required to represent a specific video sequence or image. It is widely used by a program with a particular formula or algorithm to look for the best way to limit the data size. H.265/HEVC or H.264/AVC are the algorithms used to shorten the raw content size up to 1000 times. The “baseband” bandwidth for HD 1080p60 real-time video is 3 Gbps. The resultant video stream network can be around 1 to 10 Mbps with which resultant files or real-time video streams can be transmitted easily across the modern networks. Usually, audio compression is done for proper utilization of resources. Video compression is especially beneficial for making the most of storage with significantly shrink file sizes. Video compression is widely used in all aspects of networking and computer architectures.

Video compression is the widely used term that consists of a method to shred the data size for encoding digital videos. This method provides benefits like lower transmission bandwidth and smaller storage requirements for video content.

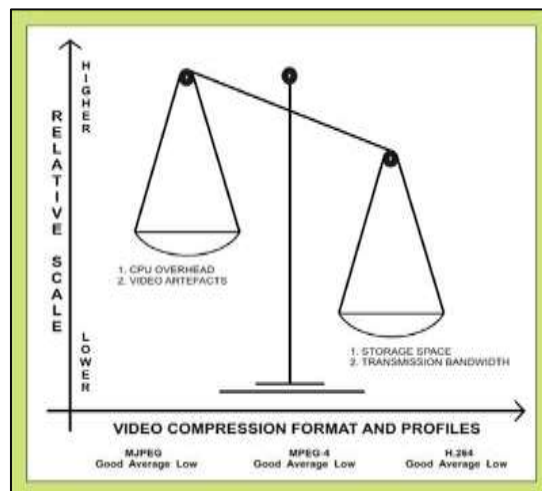


Fig. 2 – Video Compression Benefits

Video compression usually has elision which is not considered important for watching video and an effective format (video compression codec) that provides the above benefits without compromising video quality after compression and without asking for major hardware overhead for this compression. There are different compression levels applied within a specific codec of video compression. Better compression means better savings in transmission bandwidth and storage space and lower quality (such as pixelated images, blockiness, rings, blurring, etc.) uses higher computing power.

Named after the developers, Joint Photographic Experts Group, JPEG is a widely used lossy compression method used for digital images, especially captured through digital photography. M-JPEG or MJPEG emerged from JPEG for multimedia applications and digital video recording devices. Each frame is compressed individually as a JPEG file. Developed by Motion Pictures Expert Group (MPEG), MPEG4 Part 2 is a successor to MPEG-1 and MPEG-2 and provides higher compression factors like MPEG-4 AVC or MPEG-4 Part 10. This standard is jointly maintained and developed by Telecommunication Standardization Sector (ITU-T) and MPEG.

Inter-frame and Intra-frame are the approaches of video compression. Intra-frame compression consists of video frame to compress and Inter-frame consists of multiple succeeding/preceding frames in a range to compress the existing frame contents. The MJPEG standard is the intra-frame compression and MPEG-1 (VCD) and MPEG-2 (DVD), H.264 and MPEG-4 are inter-frame compression standards. MPEG4, H.264, and MJPEG are the trending and widely-used video compression standards [4]



II. DISCUSSION

Algorithm 1 - New Cross Diamond Search algorithm (VLSI Implementation of Lossless Video Compression) Compression refers to the shortening of size of data to save transfer time and storage space. Lossless Data Compression and Lossy Data Compression are two types of compression modes. While Lossy data compression enables only approximation of data to be rebuilt from compression, Lossless Data Compression enables rebuilt decompression of original data to improve the performance of the system from compression. Video compression is widely used to cut redundancy in videos and it is one of the latest coding techniques.

B. Soorya proposes New Cross Diamond Search algorithm for lossless video compression. There will be only nine checking points to calculate absolute difference to figure out the least value, which is lesser than other algorithms. It finds only the motion vector with this least value and there is less checking point than diamond search algorithm. The best part of New Cross Diamond Search Algorithm is that it is 40% faster without compromising picture quality [1].

The authors propose a New Cross Diamond Search Algorithm and its performance are compared with various algorithms through several search points and error metrics in the new cross diamond algorithm. With fewer search points than 3-Step Search, this algorithm has no compromise on performance. It also takes less computation time and results in better performance.

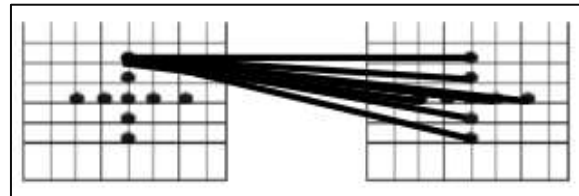


Fig. 3 – Cross Diamond Search Algorithm

This way, New Cross Diamond Search (NCDS) is found to be a computationally efficient algorithm for compressing images. This technique is great for both temporal and spatial image. It even outperforms various other models thanks to the small step size and compact search pattern for computational efficiency, namely Diamond Search, New Three Step Search, and Three Step Search. This algorithm is the best choice for H.264 AVC and MPEG-4 video coding standards as it delivers better performance and is easy to implement and less computationally complex. The search pattern with varied size and shape can highly impact search performance in motion estimation. The authors propose an NCDS algorithm with asymmetric diamond search pattern on the basis of motion vector distribution and research on search pattern. Here, they propose using two asymmetrical search patterns instead of diamond-shaped or square shaped search patterns. It is, hence, found that the NCDS algorithm performs better than other popular fast block matching algorithms in simulation results.

Algorithm 2 - VLSI Implementation of Adaptive DCT Video Compression, Digital Signal Processing or DSP blocks are widely used in several portable devices for multimedia applications. Majority of these blocks use video and image compression algorithms. Most of the computing architectures rely on the fact that a little bit of relaxation in correctness of output may result in lower and easier implementations. Over the past couple of years, the research to input information. This issue can be addressed with reconfigurable estimates for MPEG algorithms to save power and maintain peak threshold from signal to noise to every video.

Zhong-Li He proposed an adaptive bit masking approach to truncate pixels of previous and existing frames for motion estimation (ME) as per the quantization. But this truncation of coarse-grained input can be applied only to special use cases of ME and it doesn't give good results for discrete cosine transform (DCT) blocks, which needs strict control on errors [3]. S. Sai Prabhu & T. Kavitha proposes dynamically reconfigurable approximation to ensure better control over quality metrics in application levels while making the most of power consumption advantages of approximation of hardware. They also propose approximating adders of DCT and ME blocks of MPEG encoding. Their technique can adjust hardware approximation with the characteristics of video dynamically. It provides a control knob to the users with dynamic reconfiguration that can change the video output quality as well as power consumption for multimedia devices that are powered by batteries [2].

In this project, a reconfigurable approximate architecture has been proposed for MPEG encoders for power and area optimization without compromising output quality in various videos. The dynamic reconfiguring of hardware adders is the concept of this proposed architecture on the basis of input characters. It is observed in experimental results that the proposed architecture outputs 24% efficient area similar to baseline approach in which quality is not compromised with fixed approximate hardware used in various videos. Hence, this project proposes a simple approach for CSLA architecture by saving 24% space. This work also reduces the number of gates providing great benefits in reducing area. Finally, the modified CLSA framework is simple, efficient, and low area-constraint for VLSI implementation.



This ME approach is very helpful to achieve great improvements in MPEG Encoder when it comes to PSNR, Compression Ratio, and MSE.

An important part of inter-frame encoding is used in determining motion vectors (MVs) from calculation differences. Each non-encoded frame is split into 16x16p blocks or lower. An MB is associated with each MV, which has data about the displacements of MBs in the existing frame against the reference. The sum of absolute differences (SADs) minimum value is extracted from an MB regarding all MBs of the reference frame.

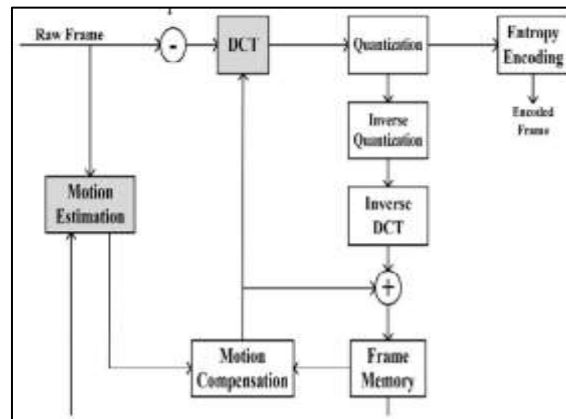


Fig. 4 – MPEG Encoder [2]

A residual error is calculated along with MVs and it is compressed with DCT. Hence, it is obvious that DCT and ME blocks are the costliest aspects of MPEG encoders in terms of computation requirement [2].

Algorithm 3 - VLSI Implementation for Basic ARPS Algorithm for Video Compression Adaptive Road Pattern Search or ARPS algorithm considers the motion coherent in a frame. It means the chances are high that existing macro block will have the same motion vector if macro blocks are moved in a specific direction around the existing macro block.

The motion vector of macro blocks is used in this algorithm immediately to forecast its motion vector. Here are the steps of running ARPS algorithm –

- Start from the origin, i.e. the search location of the centre.
- Find the block's motion vector.
- Step size to be set as $S = \max(|X|, |Y|)$. Here, (X, Y) is the coordinate of the motion vector which is predicted.
- Search for distributed road pattern points across the origin at S.
- Set the point as origin with least weight.
- Conduct the search with SDSP or Small Diamond Search Pattern on the new origin.
- Repeat the above step until the Centre of SDSP has the least weighted point.

Road pattern search keeps the search where the possibility of finding an ideal match is high. If (0,0) is the value of predicted motion vector, computational time will not be wasted in LDSP and it quickly uses SDSP, which is the best part of ARPS over DS. In addition, the ARPS saves computation time if the motion vector is not too close to the Centre as it jumps directly to the proximity and uses SDSP, while DS takes computation time for LDSP. The sum of absolute differences or (SAD) is a unit to determine the similarity in image blocks in processing digital images. The absolute difference is calculated between each pixel in the block and the corresponding pixel in the existing block. SAD is the easiest metric which consists of every block pixel and is as fast as simple.

There are two main blocks in the given architecture – URP module (for small patterns) and ARP module (for large patterns). Fig. 5 illustrates the architecture proposed by Sudharsan. B. & Dr. Diwakar R. Marur as a block diagram which consists of both URP and ARP modules [6]. This algorithm first applies ARP and then URP module. On the other side, Jayaprakash.P presents a powerful hardware architecture for implementing SAD in real-time with a multi-level and proposed SAD calculator. They put special emphasis on memory access design to balance both memory bandwidth and memory use. Other architectures compare and evaluate the performance of proposed design as throughput, memory bandwidth, hardware complexity, and operating cycles. This paper proposes efficient ARPS



algorithm architecture for estimating motion to cut down the computational complexity. This way, search speed can be improved well without compromising accuracy in motion estimation [5].

III. CONCLUSION

In this paper, it is observed that H.264 AVC and MPEG-4 are some of the widely-used and trending video coding standards because of their improved performance, ease of implementation, and low computational complexity. If someone is looking for all these benefits, the New Cross Diamond Search Algorithm (NCDS) algorithm is the ideal option because it is applicable for both temporal and spatial image and its search pattern is known for its compact shape. Considering the wide use of video coding in multimedia applications, motion estimation is a very popular technique that can cut down the temporal redundancy. MPEG and JPEG are the video and image compression codecs widely used for their power efficiency. But they may not be adaptable to input data and conventional architecture usually resolve the hardware approximations. This way, digital signal processing blocks are widely used in multimedia and smart devices. In order to optimize memory bandwidth and usage, throughput, operating cycles, and hardware complexity, the basic ARPS algorithm is proposed with VLSI implementation. It is also known to reduce computational complexity to improve search speed without compromising on accuracy. When it comes to video compression, lossless data compression is widely used as it improves computing performance and enables reconstructing original data for decompression. Video compression also reduces redundancy in modern coding techniques. This way, the New Cross Diamond Search Algorithm is considered to be ideal for lossless video compression.

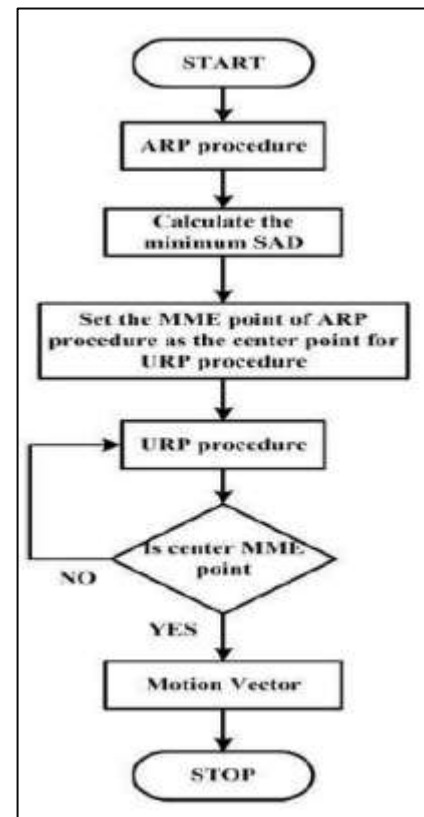


Fig. 5 – Block Diagram of ARPS

IV. REFERENCE

- [1]. Soorya, B., Shamini, S.S. and Sangeetha, K., 2017. VLSI Implementation of Lossless Video Compression Technique Using New Cross Diamond Search Algorithm. *International Journal of Communication and Computer Technologies*, 5(1), pp.27-31.
- [2]. Prabhu, S.S. and Kavitha, T., 2017. Area Effective VLSI Implementation of Adaptive DCT Video Compression. *International Journal of Applied Sciences, Engineering and Management*, 06(06), pp. 39-45.
- [3]. He, Z.L., Tsui, C.Y., Chan, K.K. and Liou, M.L., 2000. Low-power VLSI design for motion estimation using adaptive pixel truncation. *IEEE Transactions on Circuits and Systems for Video Technology*, 10(5), pp.669-678.
- [4]. Mistral Solutions. 2021. Video Compression Standards – Pros & Cons. [online] Available at: <<https://www.mistralsolutions.com/articles/video-compression-standards-pros-cons/>> [Accessed 19 April 2021].
- [5]. Jayaprakash, P., Mallaiiah, A. and Lakshmi, T.V., 2011. VLSI Implementation for Basic ARPS Algorithm for Video Compression. *International Journal of Systems, Algorithms & Applications*, 1(1), p.11.
- [6]. B., S. & Marur, D.R., 2017. VLSI Architecture for ARP and URP modules of ARPS algorithm used in HD video processor. *International Journal of Pure and Applied Mathematics*, 115(6), pp.475-482. Available at: <http://www.ijpam.eu> [Accessed April 19, 2021].
- [6]. P. Pirsch et al., VLSI architectures for video compression—a survey, *Proceedings of the IEEE* 83 (2) (1995) 1055-1070.
- [7]. T. Fryza, Compression of Video Signals by 3D-DCT Transform. Diploma thesis, Institute of Radio Electronics, FEKT Brno University of Technology, Czech Republic, 2002.
- [8]. G. M.P. Servais, .Video compression using the three dimensional discrete cosine transform., in *Proc.COMSIG*, pp. 27.32, 1997.
- [9]. R. A.Burg, .A 3d-dct real-time video compression system for low complexity single chip vlsi implementation., in the *Mobile Multimedia Conf. (MoMuC)*, 2000.
- [10]. A. N. N. T. R. K.R., .Discrete cosine transforms., in *IEEE transactions on computing*, pp. 90.93, 1974.
- [11]. T.Fryza and S.Hanus, .Video signals transparency in consequence of 3d-dct transform., in *Radioelektronika 2003 Conference Proceedings*, (Brno, Czech Republic), pp. 127.130, 2003.
- [12]. N. Boinovi and J. Konrad, .Motion analysis in 3d dct domain and its application to video coding., vol. 20, pp. 510.528, 2005.
- [13]. E. Y. Lam and J. W. Goodman, .A mathematical analysis of the dct coef_cient distributions for images., vol. 9, pp. 1661.1666, 2000.
- [14]. Bhojani, D.R. “4.1 Video Compression” (PDF). Hypothesis.Retrieved 6 March 2013.
- [15]. “FPGA Implementation of a Novel, Fast Motion Estimation Algorithm for Real-Time Video Compression”, *FPGA 2001*, CA. USA, S. Ramachandran and S. Srinivasan, Feb. 2001
- [16]. Renxiang Li, Bing Zeng, and Ming L. Liou, A New 3-Step Search Algorithm for Block Motion Estimation, *IEEE Trans.Circuits And Systems For Video Technology*, vol 4., no. 4, pp. 438-442, August 1994
- [17]. Z. Taghavi and S. Kasaei, “A memory efficient algorithm for multidimensional wavelet transform based on lifting,” in *Proc. IEEE Int. Conf. Acoust Speech Signal Process. (ICASSP)*, vol. 6, pp. 401-404, 2003.
- [18]. M. Weeks and M. A. Bayoumi, “Three-Dimensional Discrete Wavelet Transform Architectures,” *IEEE Transactions on Signal Processing*, vol. 50, no. 8, pp.2050-2063, Aug. 2002.



[19]. T.Acharya, C.Chakrabathi, "A survey on lifting based discrete wavelet transform architecture." J.VLSI Signal Process.42,321-339(2006)

ABOUT THE AUTHORS



D V Manjunatha currently working as a senior professor and HOD, in the Department of Electronics and Communication Engineering, Alva's Institute of Engineering and Technology. He studied B.E (ECE) from MSRIT Bangalore, and MTECH (VLSI) from UTL Technologies, and also he had done his Ph.D. from NHCE, VTU.He is having 23 years of experience in Academics, Teaching, Industry and Research. He participated and presented research papers in both National and International conferences, seminars and workshops. He also published 20+ Research papers in national and international peer reviewed journals and many awards.



K Gaurav Shet currently pursuing his BE in ECE at Alva's Institute of Engineering and Technology, Moodbidri.His couple of interests includes VLSI, Embedded Systems, IOT and MATLAB.



Yashwanth V currently pursuing his BE in ECE at Alva's Institute of Engineering and Technology, Moodbidri.His couple of interests includes Verilog and VLSI.



Jayasoorya currently pursuing his BE in ECE at Alva's Institute of Engineering and Technology, Moodbidri.His couple of interests includes VHDL and Front end Development.



Sampath N M currently pursuing his BE in ECE at Alva's Institute of Engineering and Technology, Moodbidri.His couple of interests includes VHDL and PCB Designing.