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Verification of Advanced Extensible Interface (AXI) Bus using UVM Methodology

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Abstract: To speed up SoC integration and promote IP reusability, many bus-based communication architecture standards have emerged over the past several years. Verification of complex System-on-Chip (SoC) designs demands the need for a highly reusable testbench. The existing methodologies are Open Verification Methodology (OVM), Verification Methodology Manual (VMM) and many other which are tool dependent and not have greater flexibility for development of testbench. Universal Verification Methodology (UVM), the proposed one provides a class library for building advanced reusable verification environment. Advanced Extensible Interface (AXI) which is the most commonly used bus protocol is verified using UVM methodology. This paper also presents the different verification strategies such as Assertion based, Coverage driven, Random functional, Static functional, Dynamic functional and Equivalence Verification Simulation is performed using Questsim tool.

Keywords: SoC, UVM, AXI

I.INTRODUCTION

Integrated circuits have entered the era of System-on-a-Chip (SoC). SoC refers to integration of more different function IP's. The designers simply integrate their owned IPs with third party IPs into the SoC to significantly reduce design cycles. Now the common problem is communication among IP's. The interfaces to these IP's differs from company to company. AXI is the most commonly used on chip bus protocols in the day-to-day high performance System On Chip (SOC's)

The AMBA AXI protocol is a standard bus protocol and most of the semiconductor companies design supports AXI bus interface. AXI protocol is a complex protocol because of its ultra-high-performance. It is a part of Advanced Microcontroller Bus Architecture (AMBA) developed by ARM Company. It is suitable for memory controllers with high initial access latency. AXI-UVM has separate address/control and data phases. It supports multiple outstanding addresses without order response supports for unaligned data transfers using byte strobes instead of supporting burst based transactions with only start address issued. It provides high-frequency operation without using complex bridges to meet the interface requirements of a wide range of components.

Nowadays, verification engineers are more compared to designers, with the ratio reaching 2 or 3 to one for the most complex designs. Therefore an efficient verification environment is needed which most is challenging for complex protocols. This can be easily verified using the UVM and can also be reused for other IPs. The Universal Verification Methodology (UVM) offers base class libraries for developing reusable, robust and scalable test benches. An UVM testbench is composed of reusable verification components such as monitor, agent, driver, sequencer and environment which helps verification engineer to find more bugs earlier in the design process.

II.PROBLEM STATEMENT

Exponentially increasing complexity of chips particularly SOC's made verification more challenging. Verification takes the lion's share of the ASIC design cycle. ASIC verification & simulation need to take place for the sustainability of functions in the device. Today, verification has reached the stage where conventional direct testing methods are no longer useful.

The tools and techniques to be used have to be decided upon early in the design cycle to get the best value for the new verification methods. Use of reusable standards in verification which is the proposed one reduces the time required to build and verify the SOC infrastructure which shortens the overall risk associated with the design as in

III. DESIGN AND IMPLEMENTATION

AXI is a burst based protocol. The AXI architecture describe an interface between a single AXI master and AXI slave, representing IP cores that exchange information with each other. Multiple memory-mapped AXI masters and slaves can be connected together using a structure called an Interconnect block.

- 2 Read channels

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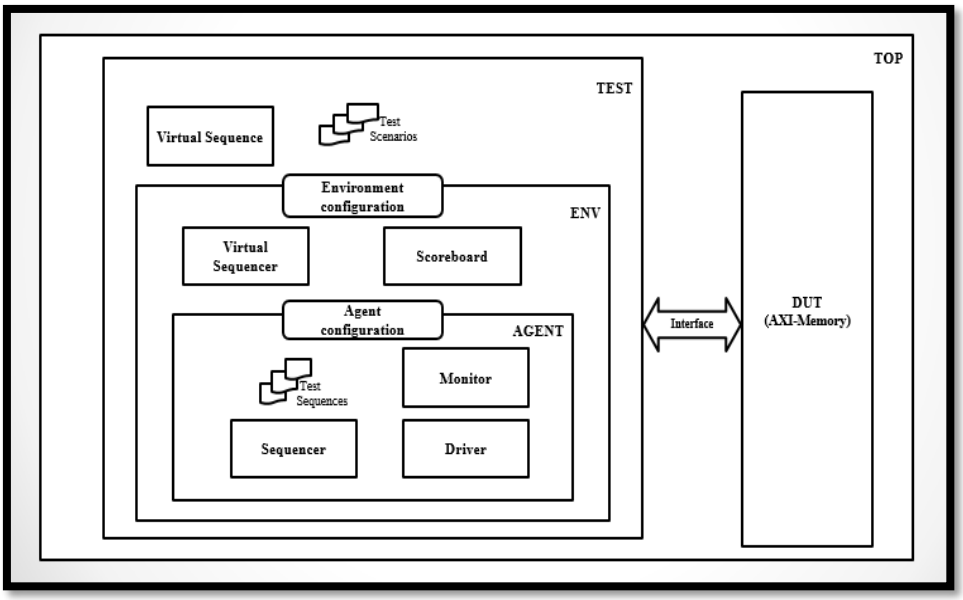
- Read address
- Read data
- 3 write channels
- Write address
- Write data
- Write response
- separate address/control and data phases
- uses burst-based transactions with only the start address issued
- separate read and write data channels, that can provide low-cost Direct Memory Access (DMA)
- support for issuing multiple outstanding addresses and out-of-order transaction completion
- permits easy addition of register stages to provide timing closure
- is suitable for high-bandwidth and low-latency designs
- provides high-frequency operation without using complex bridges
- meets the interface requirements of a wide range of components
- is suitable for memory controllers with high initial access latency
- provides flexibility in the implementation of interconnect architecture

III.VERIFICATION APPROACH

Exponentially increasing complexity of chips particularly SOC's made verification more challenging. Verification takes the lion's share of the ASIC design cycle. ASIC verification & simulation need to take place for the sustainability of functions in the device. Today, verification has reached the stage where conventional direct testing methods are no longer useful.

The tools and techniques to be used in a project have to be decided upon early in the design cycle to get the best value for the new verification methods. Use of reusable standards in verification which is the proposed one reduces the time required to build and verify the SOC infrastructure which shortens the overall risk associated with the design. Thus, the new reusable methodologies and different verification strategies used are-

- Coverage driven Verification
- Assertion based Verification
- Random functional verification
- Dynamic functional verification
- Static functional verification



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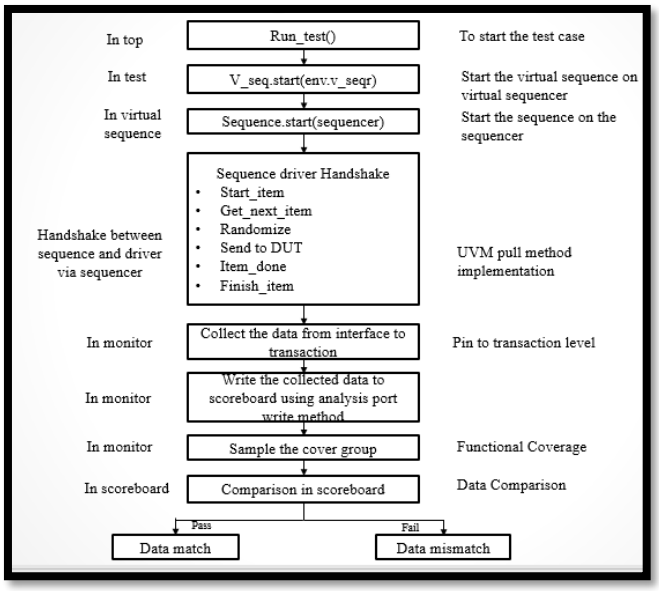

V. EXPERIMENTAL RESULTS

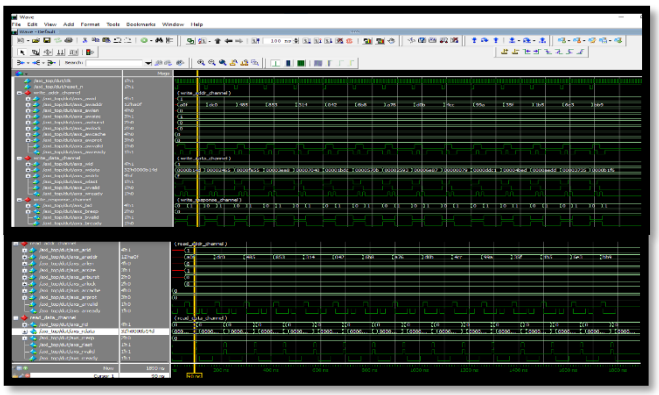

Fig: AXI Signal Waveforms

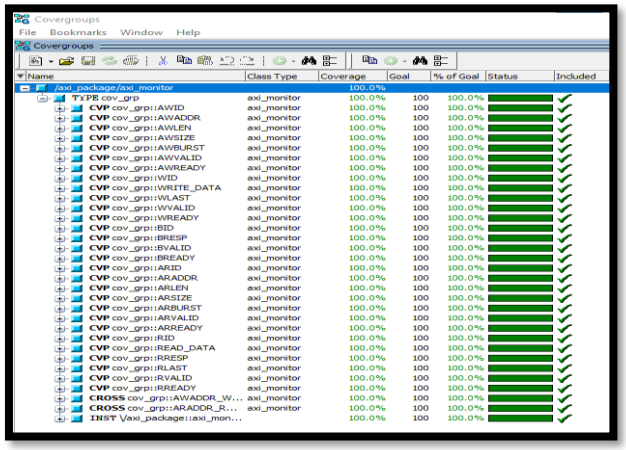

Fig: Functional Coverage

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Fig: Assertion Coverage

VI. CONCLUSION

The AMBA AXI specification signifies a major evolutionary step in interconnect technology for System on-chip designs. The project helped to achieve the verification of AMBA AXI bus. Here all the signals are verified using UVM. The master sends the address and data to the slave and gets the response effectively by the slave. In this paper, environment for verification of AXI is achieved and it checks for normal read and write transactions and out of order transaction. UVM provides a rich set of base class library and features required for efficient verification. It gives an environment that is robust, easy to understand and thus, reusable by others vendors.
Using UVM, requires less time to generate a testbench as it offers higher level of abstraction. It covers almost all the possible scenarios and corner cases and thus, increases the functional coverage.

Code coverage	92%
Functional Coverage	100%
Assertion coverage	100%

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