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Analysis of New Reduced Device Count MLI Using Different PWM Techniques

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Abstract: -. In this paper a "Analysis of New Reduced Device Count MLI Using Different PWM Techniques". Since Penetration of multilevel inverters (MLI) in to high power and medium voltage application has been increasing because of its advantages. . The invention of MLI led to the increase in power rating of the devices, as the number of output voltage levels also increased. Even though many MLI topologies have been proposed over the years the elementary concept of a multilevel inverter remains the same, i.e., to achieve higher power output using several series connected power semiconductor switches and multiple low valued DC sources. And DC to AC convertors are playing an important role in various medium and high power applications.

Keywords: Multilevel Inverter , PWM Techniques , MLI Simulation, 5-level Topology

I. INTRODUCTION

The advancement in power electronic devices, digital control systems and advance sensors, the role of power electronic converters in the modern power system has been envisaged. DC to AC convertors are playing an important role in various medium and high power applications, which include variable frequency drives, FACTS, HVDC transmission systems. A multilevel inverter is power electronics device this is used for high-power high-voltage utilization consisting of Uninterruptible power supplies. The basic two level inverter is shown in Fig.1 From the output voltage waveform it can be seen that the inverter only outputs two voltage level of. The basic two level inverter suffered from various disadvantages such high harmonic content at the output, high stress and high EMI.

The idea of multilevel inverter was first introduced by Baker et al in 1970. It was introduced to remove the disadvantage of the conventional two-level inverter.

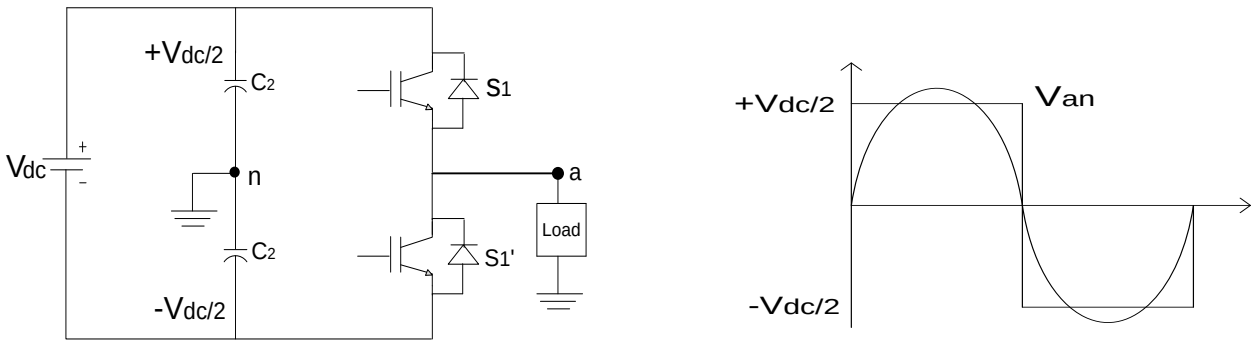

Fig.1 Single phase two level inverter with output voltage waveform

II. MULTILEVEL INVERTER STRUCTURES

The introduction of the three level inverter the term MLI came into existence. The invention of MLI led to the increase in power rating of the devices, as the number of output voltage levels also increased The conventional MLI structures ca divided into three types: diode clamped (neutral point clamped), flying capacitor (capacitor clamped) & cascaded H-bridge inverter.

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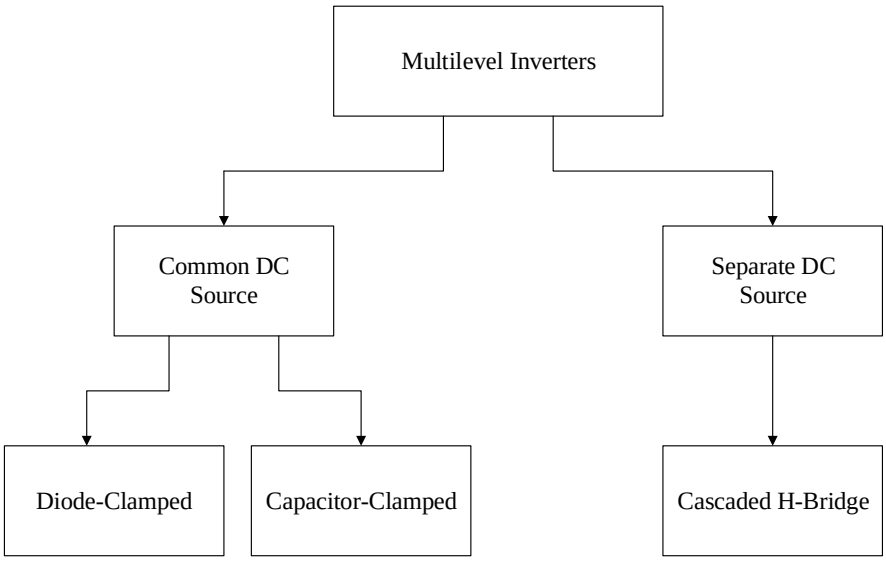
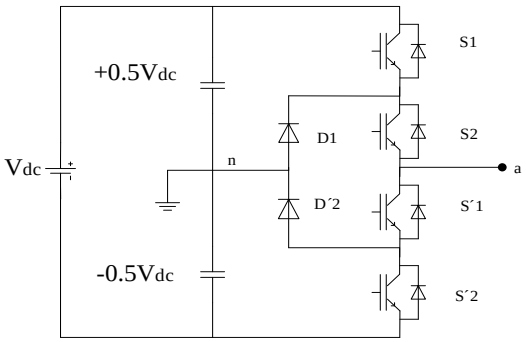


Fig.2 Classification of MLI structures

Diode Clamped Inverter : The Diode Clamped Inverter is Two pairs of power semiconductor switches are connected in parallel to the two series connected capacitors. Fig 3(a) shows a single phase three level DCMLI. And Switching state and the output voltage waveform for a three level diode clamped MLI is shown in Fig 3 (b)



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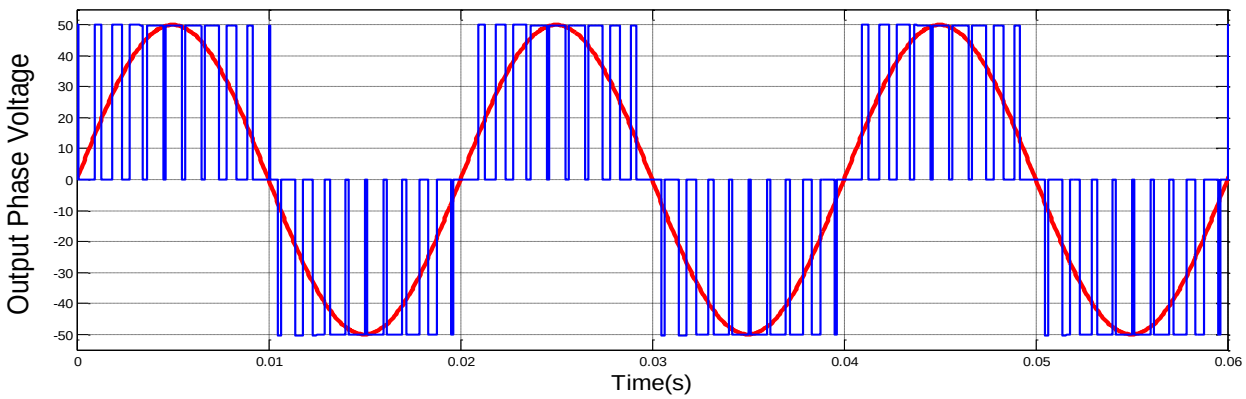

(b)

Fig. 3 Three level DCMLI (a) Equivalent Circuit Diagram (b) Output Voltage Waveform

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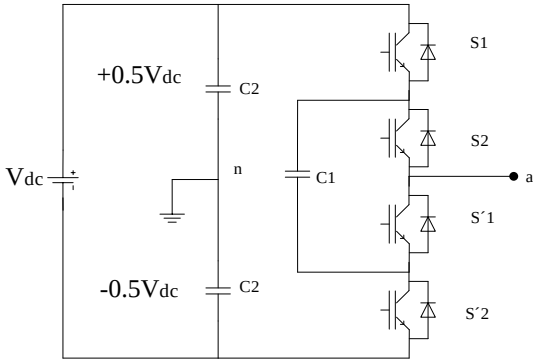
Flying Capacitor Inverter : The flying capacitor inverter also known as the capacitor-clamped inverter was introduced in 1990s by T. Maynard et al.. Fig 4 shows a three level flying capacitor inverter, along with the equivalent switching state and output voltage waveform. The switch pairs S_1-S'_1 is turned on the capacitor C_1 gets charged and when S_2-S'_2 is turned off the capacitor gets discharged.



(a)

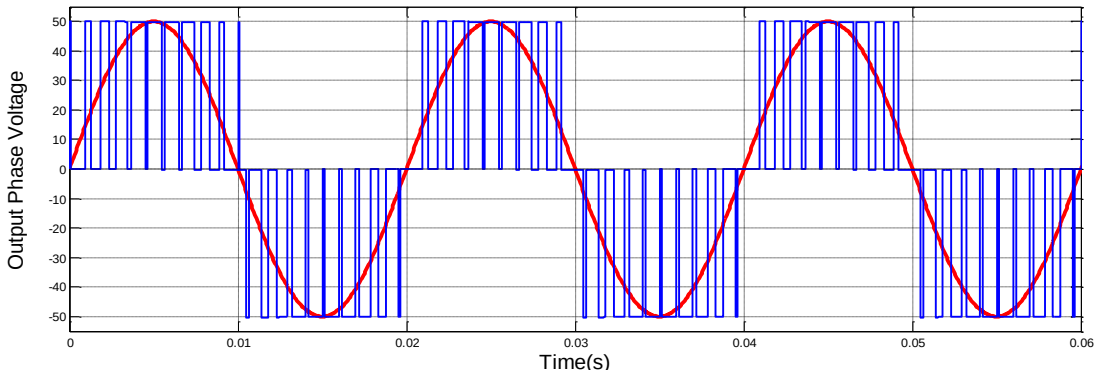
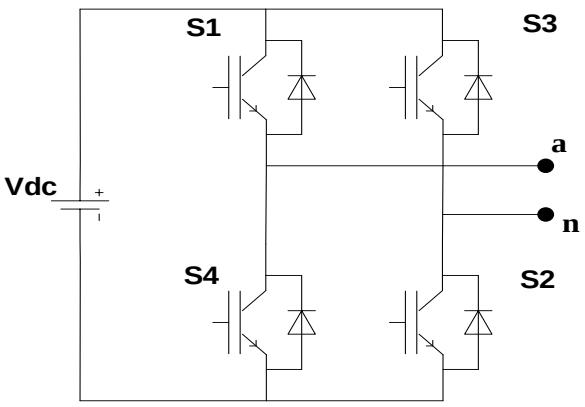


Fig. 4 Three level FCMLI (a) Equivalent Circuit Diagram (b) Output Voltage Waveform

Cascaded H-Bridge : The Cascaded H-Bridge inverter is made up of multiple series string of single-phase full bridge inverters. Fig 5 shows a single H-bridge which can output three discreet voltage levels. The switches S_1 and S_2 are turned –on output voltage is $+V_{dc}$; when switches S_3 and S_4 is turned on the output voltage is $-V_{dc}$; when either pair S_1 and S_3 or S_2 and S_4 is turned on the output voltage is zero.



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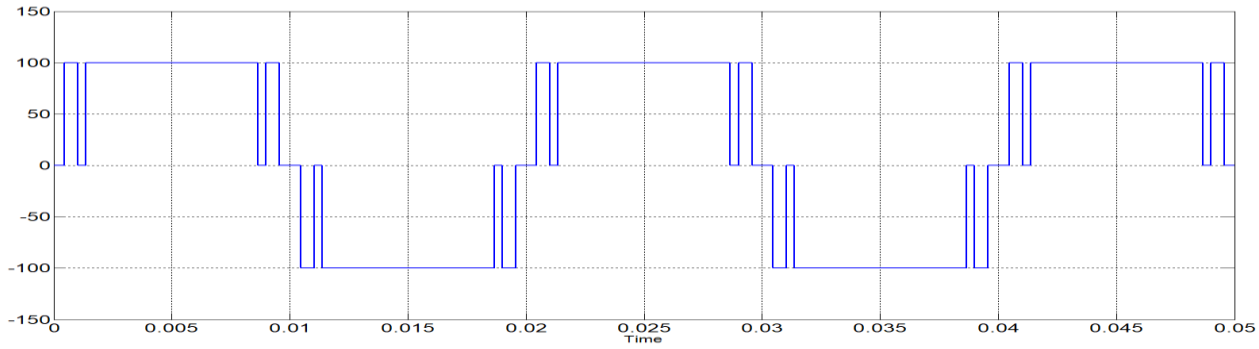

(b)

Fig.5. Three Level Cascaded H-bridge MLI (a) Equivalent Circuit Diagram (b) Output Voltage Waveform.

III. 5- LEVEL SWITCHED CAPACITOR TOPOLOGY

The basic structure of the 5-level topology is shown in Fig.6 it consists of two H-bridges. One of the H-bridge is connected to an input DC source. The neutral point of both the H-bridge is connected via a bidirectional voltage blocking switch. This 5-level inverter circuit is able to produce voltage boosting factor/gain of two.

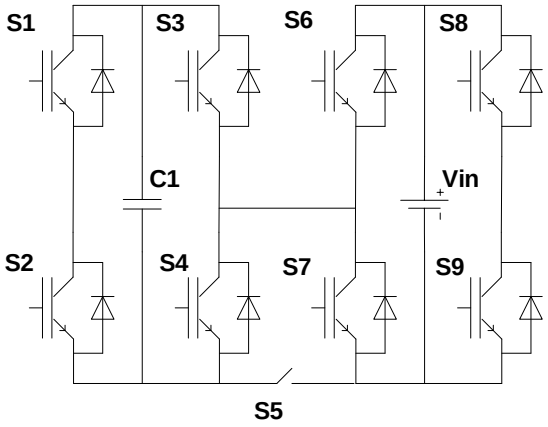

Fig 6, Five- topology level

IV. OPERATION OF THE NEW 5- LEVEL SWITCHED CAPACITOR MLI TOPOLOGY

Fig.7 shows the equivalent switching state for the proposed 5-level inverter. The capacitor C_1 gets charged to V_{dc} whenever it connected across the source and gets discharged whenever it's in series with the source transferring the stored energy back to load. In first state the capacitor C_1 is connected across the source and in the second state the source and the capacitor both are connected in series.

First state is achieved when switches S_3, S_5, S_6 is turned on the capacitor C_1 gets connected across the source V_{dc}. $V_{bus} = 0$

Capacitor fully charged and switches S_1 turned on, the output voltage across the bus is.

$$V_{bus} = V_{dc}$$

The switches S_1, S_4, S_6, S_9 is turned on and the capacitor is connected in series with the source.

$$V_{bus} = V_{c1} + V_{dc}$$

The low voltage stress across the power semiconductor switches results in use of low voltage rating switches.

The 5-level MLI topology produces a maximum voltage stress of V_{dc} which is two times less than the maximum achievable output voltage. The low voltage stress across the power semiconductor switches results in use of low voltage rating switches. The fact that low voltage stress appear across the switches can be varied by examining the equivalent switching state.

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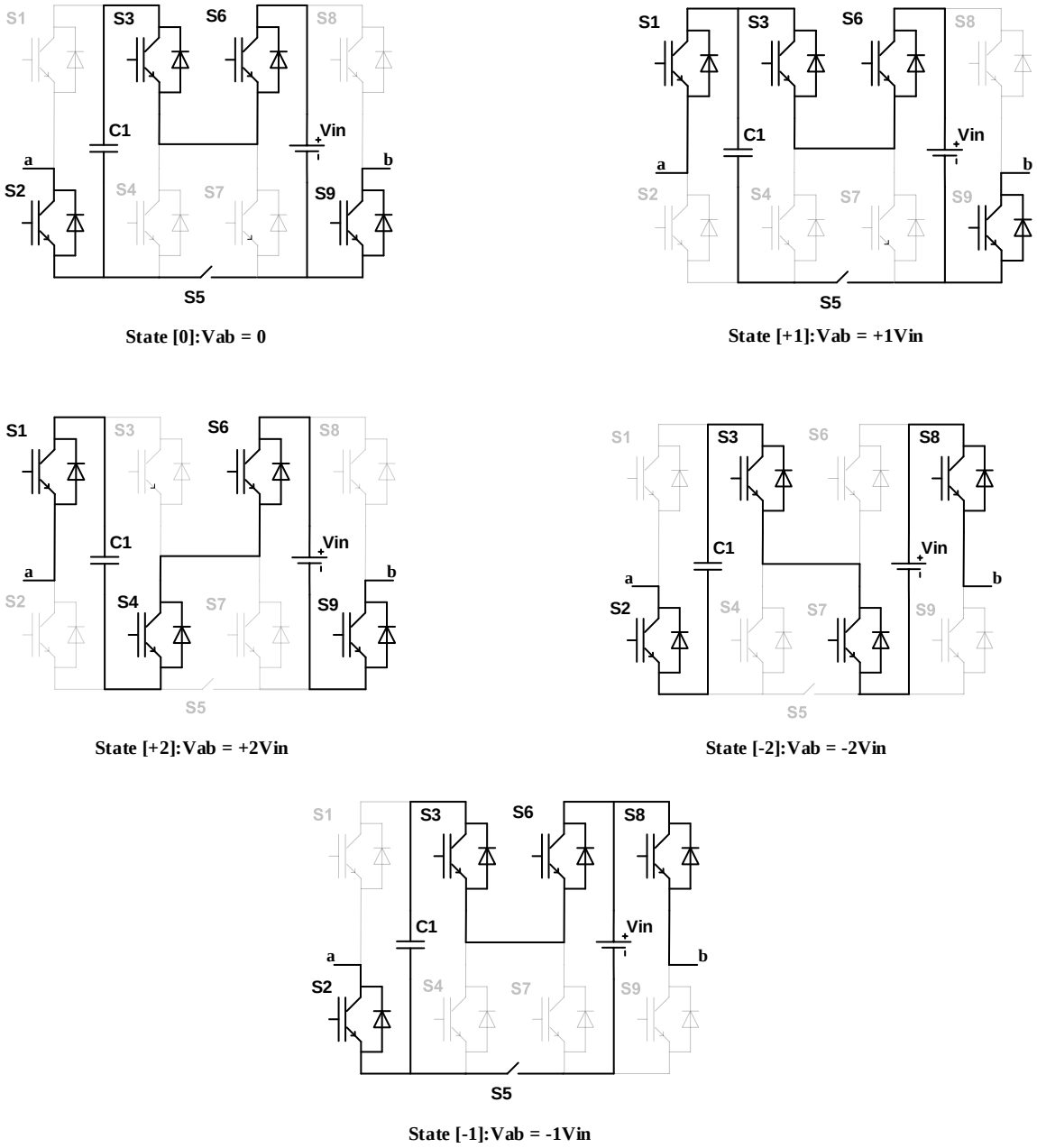

Fig 7. Equivalent Switching State for all Voltage Steps

Table 1 Switching state for 5-level SC MLI

SWITCHED	STATES				
	0	**+1**	**+2**	**-1**	**-2**
S1	OFF	ON	ON	OFF	OFF
S2	ON	OFF	OFF	ON	ON
S3	ON	ON	OFF	ON	ON
S4	OFF	OFF	ON	OFF	OFF

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S5	ON	ON	OFF	ON	OFF
S6	ON	ON	ON	ON	OFF
S7	OFF	OFF	OFF	OFF	ON
S8	OFF	OFF	OFF	ON	ON
S9	ON	ON	ON	OFF	OFF

V. SIMULATION OF 5-LEVEL SWITCHED CAPACITOR TOPOLOGY

The 5-level switched capacitor MLI is modelled using MATLAB. Fig 8 shows the MATLAB model for the 5-level MLI. The gate control signals for the switches are obtained from the aggregated waveform using logic circuit and a lookup table.

A Universal control scheme is employed to control all the switches in the MLI. In this control scheme each carrier wave is compared with the modulating signal, such that for all carrier signal above zero reference, if modulating signal is greater than carrier signal the output becomes '1'and '0' otherwise. For all carrier signal below the zero reference, if modulating signal is greater than carrier signal output of each comparison becomes '0' and '-1' otherwise. The result so obtained is added up to form an aggregated waveform having the same wave shape as the output voltage. The gate control signals for the switches are obtained from the aggregated waveform using logic circuit and a lookup table.

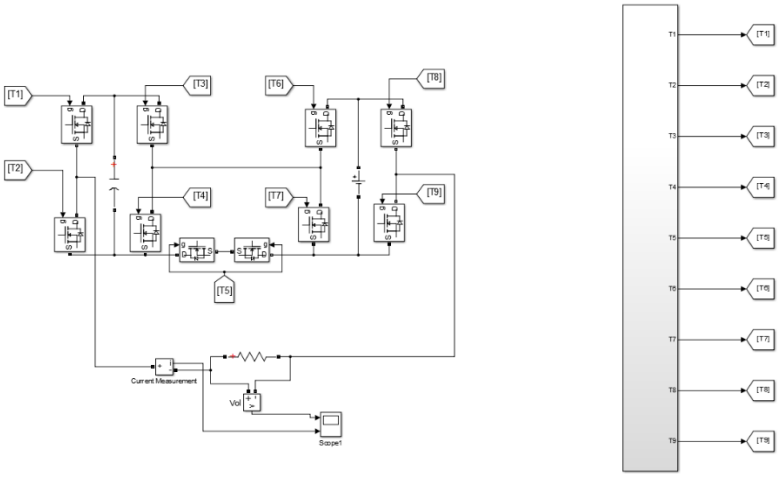
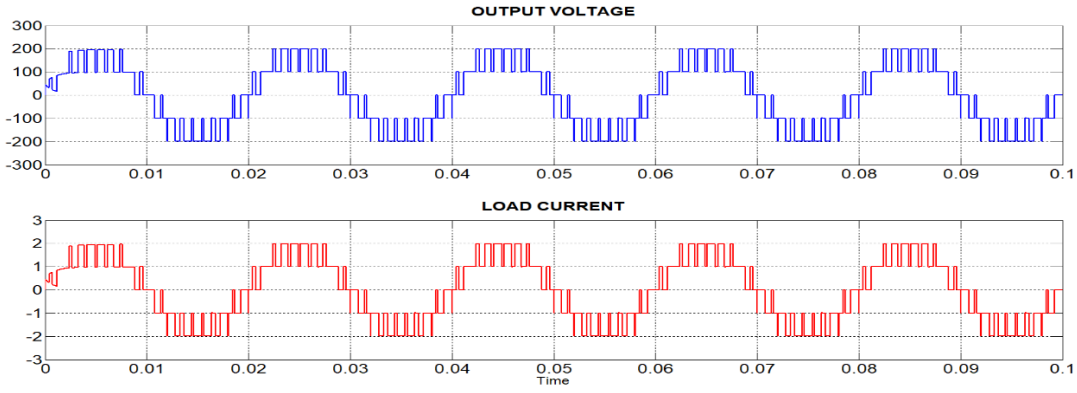


Fig.8 MATLAB model of 5-level SC MLI

Simulation Result

Fig. 9 shows the output voltage and current for a 5-level inverter with resistive load at $m_a = 0.9$ and $m_f = 20$ for different PWM techniques. And Table 5.1 shows the percentage THD of 5-level MLI when driven using different PWM technique.



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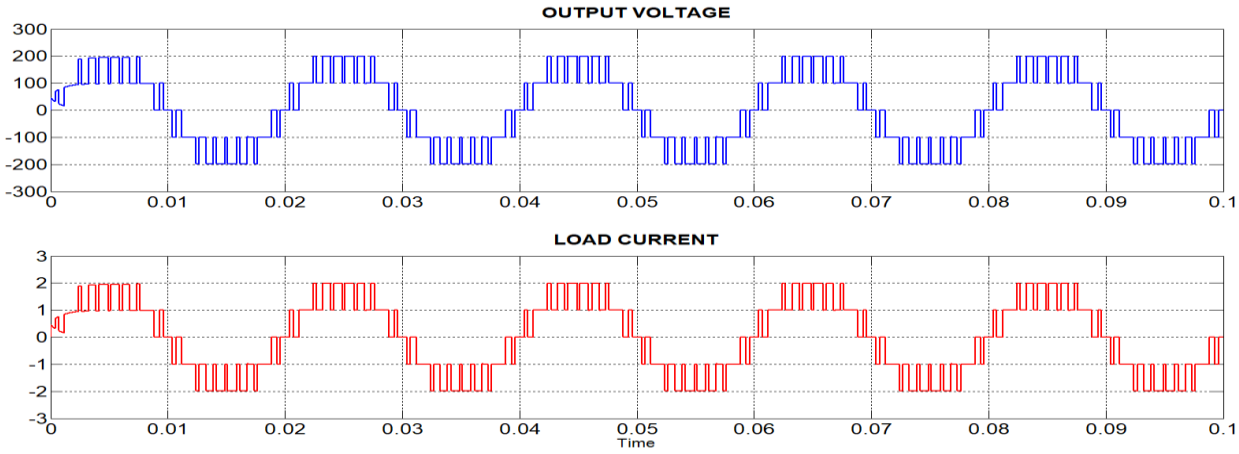

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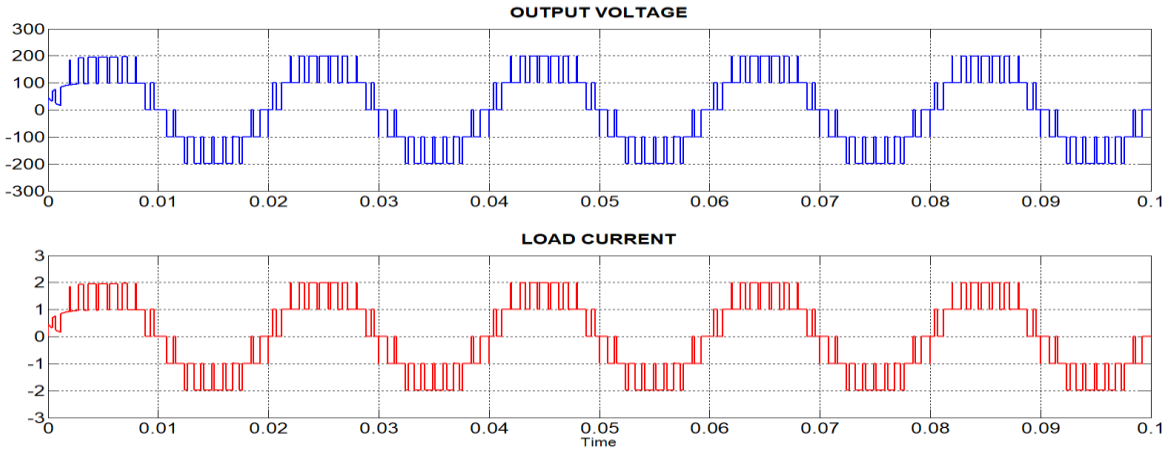

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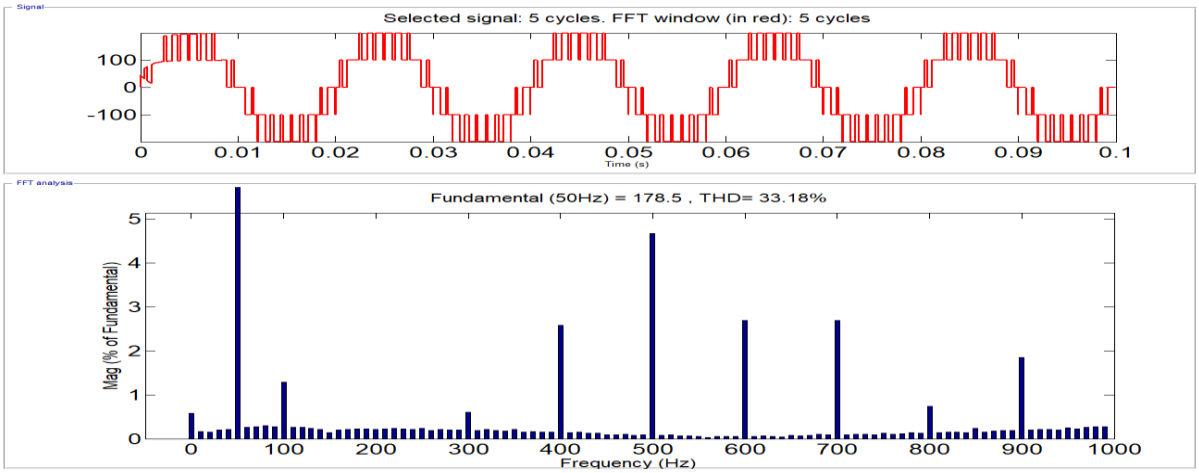

(d)

Fig.9 Results for pure resistive load; (a) load voltage and load current waveform with PD-PWM, (b) output voltage and load current with POD-PWM, (c) output voltage and load current waveform with APOD-PWM, (d) output voltage and load current waveform with PS-PWM.

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TABLE II : % THD for all PWM Techniques Using Sinusoidal Reference Wave

Modulation Index (M_a)	PD PWM %THD	POD PWM %THD	APOD PWM %THD	PS PWM %THD
1	26.79	27.07	26.77	26.69
0.9	33.18	33.49	33.18	33.19
0.8	38.16	38.38	38.16	38.12
0.7	41.19	42.26	41.18	41.29
0.6	43.95	44.58	43.96	44.02

VI. CONCLUSION

The circuit analysis and operation of each SC MLI is explained in this work. The output voltage and load current waveform for resistive load at $m_a = 0.9$ and $m_f = 20$ is also simulated and presented in this work. The output voltage waveform further verifies the voltage boosting ability of the new SC MLI. The implemented 9-level MLI is able to generate a quadruple voltage gain, which is highest among all the three levels implemented in this work. Multi-carrier PWM method is applied to the new topology to trigger the power switches for controlling the voltage levels generated on the output. It was shown that the presented topology can be used in high-power applications.
The five switch five level and a six switch seven level multilevel inverter is proposed. A simplified pulse width modulation technique also has been implemented for proposed inverters. Based on the PWM wave forms a digital switching logic has been developed and implemented to the control logic. The five level and seven level inverters are analyzed with R and RL load and the results are presented. The total harmonic distortion is also measure for both the levels.

FUTURE WORK

In this dissertation work performance evaluation of 5, 7, 9 level SC MLI is done using various SPWM techniques. The presented work can be further extended in the future by employing advanced PWM techniques like SHE, MPWM, 3rd Harmonic injected PWM e.tc. Further more the work presented here employs one performance parameter i.e. percentage THD for the performance evaluation. The work could be further extended my using more performance evaluation factors like Form Factor and Crest factor. The use of different modulating waveform other that the sinusoidal wave like 3rd Harmonic infused reference wave, trapezoidal reference wave can also provide a more comprehensive evaluation of the new SC MLI.

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