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Conceptual modeling of advanced automat using Verilog HDL

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Abstract: This project describes the designing of an automatic vending machine using Finite State Machine as this technique has more advantages compared to previous ones used for vending machine design. We have stated the suitable FPGA board for this automated dispenser. Microprocessor and microcontroller devices have very small random access memory And there are many other issue like high power Consumption, Low reprogramming ability and low Operating frequency But FPGA based technology is avoided from these issues. In supporting this requirement, the manipulation of vending machine is identified as a tool to promote modern and healthy living style, besides to simplify the cooking process. Nowadays with the increasing quantity of waste generated and restricted lowland house for waste disposal The vending machine accepts plastics as inputs in any sequence and delivers products when required weight of plastics is deposited and gives the food products. FPGA based vending machine in less time consuming, uses less power and also rapid proto typing. The FPGA based machine is likewise more adaptable, programmable and can be re-customized. Wastages of plastics are inserted into the machines. The machine accepts that plastics and items will dropped on the tray. The efficient algorithm for this automat is implemented in Verilog HDL and simulated using Xilinx ISE simulator tool.

Keywords: Verilog HDL; Xilinx ISE simulator; vending machine; Automat; Conceptual mode; simulation; FSM; FPGA board.

I. INTRODUCTION

Conceptual modeling is the most important aspects in the process of simulating model development because it will gives significant affects, on the quality and efficiency of simulation project. In other words, conceptual modeling involves deciding the way in which the virtual world of the simulation model should work, typically the entities that contains and all the interaction, rules, and equations that determines their behaviors. Thus, the design of the model will give impact on all aspect of a simulation study, in particularly the data requirements, development process speed for the model, validity of the model, speed of experimentation and reliability of the model result. Hence, it becomes the most difficult and leas/t understood stage in the modeling process. This project describes the process of creating the conceptual model for simulation of wastage of plastics is used to finding the way to food in vending machine. Generally, the problem is being studied because this initiative

promotes consumer to eat healthy food in faster way. Vending machines such an auto self-service medium; which able to cater consumer needs by pressing the selected button and after a while consumer can get the required food .Conceptual modeling is the most crucial part in developing simulation model; since in this part, the developer need to identify the variables; recognize the desired simulation flows and transform the deliverables into visualized form which can be understood by all parties related to the project. The implementation of vending machine is being considered since the tool is substantial in reducing staff costs, particularly if a 24 hours service is considered The main objective of our project is: To design a model of an automat that dispenses four items (such as candy, muffins, breads and snacks). When, a minimum amount of wastage of plastics such as (plastic cups, plastic cans and plastic papers) to be inserted. The FPGA based vending machine supports four products and three kinds of plastics. The vending machine accepts plastics as inputs in

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any sequence and delivers products when required amount is deposited and gives the food products. If the timer is ON condition, when the user not using the machine and if the timer is OFF condition, when the user using the machine. Here in this project, we proposed an efficient algorithm of vending machine on FPGA board. The proposed algorithm is implemented in Verilog HDL and simulated using Xilinx ISE simulator tool.



Fig.1 Block diagram

II.OVERVIEW AND HISTORY

For a long while microcontrollers and microprocessors were the only way to implement embedded systems and any other automated devices. These devices have very small random access memory (RAM) and there are many other design aspect issues like high power consumption, low reprogramming ability and low operating frequency. To avoid these issues present trends are shifting from the microprocessor to FPGA technology[5]. FPGA[6] referred to as Field Programmable Gate Arrays. FPGA boards consist of electrically programmable logic blocks known as configurable logic blocks(CLBs), huge memory blocks and the high number of input-output banks (IOBs). For example SPARTAN-6 FPGA board, it consists of 9152 logic cells, 576Kb max block RAM, 160 I/O pins with 1.2V to 3.3V I/O voltage [7]. The main advantage of FPGA is its re-programmability. We can find also an error block at any time and we can reprogram that to the desired operation any number of times .Based on that programmability electrically CLBs. The typical flow is : identify the error block \rightarrow change that logic function \rightarrow compile it \rightarrow reprogramme it on the board. Implementing the design requires little knowledge of the FPGA architecture and implementation programs[8]. FPGA has a wide range of applications in instrumentation.If design is based Finite State Machine(FSM)[9], the any on state response fully depends on the frequency of the clock signal. By changing the clock frequency up to a certain range of values, we can improve the speed of machine operation. FSMs are of two types, as shown in Fig.1 one is the MEALY machine: Outputs are functions of inputs and present states. Another one is the MOORE machine: Outputs are the functions of only present states. These dispensers are mostly mealy based FSM.



Fig. 2: Moore and Mealy Machines block diagram

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III. METHODOLOGY

Working :

• Initially when the START button is pressed, the machine will be ready for the users to sense the product(check whether material is plastic or not). This state is the initial state of the design.

• After this the machine will check the weight of plastics inserted

• The machine can accept only three types of plastics such as (plastic cups, plastic cans and plastic papers)

• If considered amount of weight (>400gms) is present in plastic then user will able to select the product to be dispensed. This state can be one of the select1, select2, select3 and select 4.

• Let us suppose that the user selects 1 input. The machine will firstly check the weight of the plastics then the machine accepts that plastics and items will dropped on the tray.

• When the desired amount of plastics inserted the machine will go to the product state and will be delivered at the product output.

• If products are not available in the machine then the control unit will demand for servicing and after service the machine will get reset.

- This methodology is explained using a flow diagram shown in Fig,
- A weight count signal is used for calculating the total plastics inserted to the machine.

• And if the more amount of plastics inserted to the machine that will calculate the weights and it gives the equivalent product for that plastics.

IV. IMPLEMENTATION

In our proposed method two designs developed have the difference of IO standards[7]. The Customer has to select the product and plastic mode from the keypad. Once the plastic will be inserted completed, the product will be dispensed and the product display count will update.

A. Input combinations of Automated dispenser

The input combinations of the designed automated dispenser. To start and get the product using any kind of plastic mode

B. RTL Schematics

The RTL schematics [16] two designs are shown here



Fig.3: Automated Dispenser design with only selected product count display



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Automated Dispenser design with only selected product count display: In the first design, the dispenser will display only selected product count. Automated Dispenser design with all product count display: But in the second design, the dispenser will display all products count. For this design all three FPGA board's

Below diagram: Automated Dispenser design with all product count display



The experimental setup of this dispenser is that we have used Verilog HDL[4] and the PlanAhead design and analysis tool[17] (available in the ISE Design Suite [3]). We have created a PlanAhead project sourcing HDL model(s) and targeting specific FPGA devices. By using the provided user constraint file (UCF) to constrain pin locations [18]. We can manually place and route the signals or we can make the tool itself place and route the signals. We synthesized, implemented the design. Finally, we have generated the bitstreams for two designs for the above-mentioned FPGA boards.

V. POWER COMSUMPTION

In this proposed automated dispenser we are using low voltage variants of CMOS. The experimental setup of this dispenser is that we have used Verilog HDL[4] and XPower analyzer (XPA)tool [22] (available in the ISE Design Suite [3])was used for calculating the power[23]. This tool can be used for more accurate estimates and power analysis since XPower Analyzer utilizes the logic and routing resources of the actual design. Total dissipating power is the summation of clock power, logic power, signals power, IOBs power and active leakage power



6.RESULT

Fig 4.RTL View



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Below simulation diagram represent If clock value is 0 and the plastic inserted 400 kg running the process. And the state are 100 and the next state are 101.

		1,310.000 ns												
Name	Value		1,290 ns		1,300 ns		1,310 ns		1,320 ns	1	1,330 ns		1,340 ns	1
la clock	1													
🗓 reset	0													
Pastic[2:0]	010							010						
ါ <mark>ြ</mark> vend	0													
🔻 📑 state[2:0]	100	010	100	101	000	010	100	101	000	010	100	101	000	010
16 [2]	1													
16 [1]	0													
16 [0]	0													
🔻 📷 change[2:0]	010	000	010	001	000		010	001	000		010	001	000	
16 [2]	0													
16 [1]	1													
16 [0]	0	-												
🔻 🃷 next_state[2:0]	101	100	101	000	010	100	101	000	010	100	101	000	010	100
16 [2]	1													
16 [1]	0													
16 [0]	1													
		X1: 1,3	10.000 ns											

Fig 5.Simulation Result

VI.CONCLUSION

It was observed through different scenarios, that FPGA based vending machine give fast response and also show low power consumption and easy to use by an ordinary person. Our results clearly indicate that FPGA based solution increases the efficiency and accuracy of vending machines. Also we can monitor the FPGA based vending machine with the main frame computer. Its algorithm is very flexible and reliable as the vendor can easily enhance the algorithm for large number of products and coins of different denominations at low cost as compared to microprocessor based vending machine.

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