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# Simulation, Analysis and Comparative Study of Three Phase Multilevel Inverters

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**Abstract:** Multilevel inverter has appeared as one of the important topologies in the area of high power and medium voltage situation. These "multilevel inverters" have attracted numerous applications irrespective of the power ratings because they can efficiently realize lower harmonics with reduced switching frequency and also produce high voltages with reduced "Total Harmonic Distortion" (THD). This paper uses MOSFETs and IGBTs to model "Diode clamped" and "Cascaded H-bridge multilevel inverter" and analyse the harmonic content. In addition, through a comparative analysis of the topologies, this paper demonstrates the features of the different "multilevel inverter" topologies. The performance of the proposed topologies is realised using MATLAB/Simulink.

**Keywords:** Multilevel Inverter (MLI), Diode Clamped Multilevel Inverter (DCMLI), Cascaded H-bridge Inverter (CHB), Pulse Width Modulation (PWM), Total Harmonic Distortion (THD).

## I. INTRODUCTION

Over the past few years, energy demand across the world is growing very fast, due to which the generation and consumption of electrical enrgy is shooting up at a rapid rate. Many renewable energy sources such as solar generates DC, however for grid connected solar PV system, this has to be converted to AC with proper magnitude and frequency [1]. Also, not all of the loads (appliances/ machines) use DC power supply, but many of them require an AC power as their primary source. This is where inverter is needed to convert DC energy to AC energy. However, as the inverters created large interest in the industrial applications where it was used in many high power and voltage applications, but due to its drawbacks it created many grids associated problems [2]. Later on, tremendous improvement was made in the area of inverter technology in terms of number of output levels and switching techniques. This is where MLI stood as a solution to the basic structure of inverter by modifying the parameters such as size and components in order to achieve different levels.The concept of MLI was introduced in 1975 by Nabae which was presented in IEEE conference and the same concept was published in the IEEE transactions in "Industrial Applications". "Multilevel inverters" have also recognized for their capacity on high power and medium voltage function, and because of their ability to provide higher power quality and reduced switching losses.

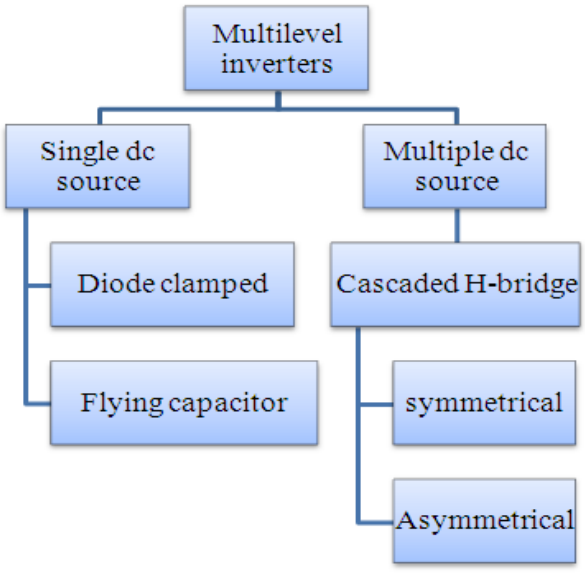


Fig 1. Classification of MLI's

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CLASSIFICATION OF MULTILEVEL INVERTERS

There are three different topologies proposed for multilevel inverters, they are:

A. Diode Clamped Multilevel Inverter.
B. Flying Capacitor Clamped Multilevel Inverter.
C. Cascaded H-bridge Multilevel Inverter.

A. Diode Clamped Multilevel Inverter: The diode-clamped inverter is also known as the neutral-point clamped inverter (NPC). It comprises of two pairs of series connected switches which is connected in parallel with two series capacitors where the anode of the upper diode is connected to the centre point of the capacitors and the diodes are used as clamping devices. The middle point of the two capacitors can be defined as the "neutral point". These inverters use diodes to reduce the voltage stress of power devices. The number of levels of phase voltages at the output is in accordance with the number of capacitors present in single phase. A m-level diode clamped inverter need:

- Number of dc bus capacitors (Ndc) = (m-1)
- Number of clamping diodes (Ncd) = (m-1)(m-2)
- Number of semiconductor switches (Nss) = 2(m-1)

B. Flying Capacitor Clamped Multilevel Inverter: Meynard and Foch introduced a flying-capacitor-based inverter in 1992. Flying capacitor inverter uses capacitors in place of clamping diodes used in diode clamped inverters, other than this its structure looks similar to that of diode clamped inverter. It is of a series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The output is half of the input DC voltage. The voltage over each capacitor and switch is Vdc.

An 'm' level inverter need:

- Number of voltage sources Ndc = (m-1)
- Number of switching devices Nsd = 2(m-1)
- Number of balancing capacitors Nbc= (m-1)(m- 2)/2
- Number of DC bus capacitors Nc = (m-1)

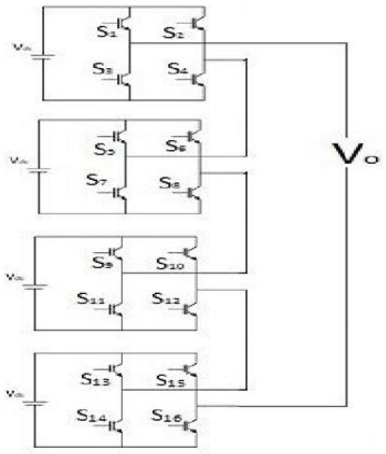
C. Cascaded H-bridge Multilevel Inverters: The cascaded H-bridge inverter has created enormous interest because of its higher demand in medium-voltage high-power inverters. This topology consists of a series of power conversion cells and power can be easily scaled. It consists of H-bridge cells where each individual cell can give three different voltages like zero, positive DC, and negative DC. The output voltage generated by this multilevel inverter is actually the sum of all the voltages generated by each cell i.e. if there are n cells in a H-bridge multilevel inverter then number of output voltage levels will be 2n+1.

A m-level cascaded H-bridge inverter need:

- Number of separate dc sources (Ndcs) = (m-1)/2
- Number of switches (Nsw) = 2(m-1)

## II. METHODOLOGY

A. Three phase five level Diode Clamped MLI.



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As the name indicates, the greater number of diodes are used to limit the voltage stresses i.e., as the clamping device to clamp the dc bus voltage so as to achieve proper steps in the output voltage. A diode clamped multilevel inverter consists of (m-1) capacitor on the dc bus and produces m levels on the output phase voltage.
Fig2 shows the Single Phase Five Level Diode Clamped Multilevel Inverter Topology. This multilevel inverter produces five level output with four capacitors on the dc bus along with eight switching devices and six clamping diodes in series.
In a five-level inverter leg,
m= 5
m-1=4 capacitors
2(m-1) = 8 Switches (s1, s2, s3, s4……s8).
The three phase DCMLI has three legs of which each leg consists of eight switches. For an m-level inverter, there are (m-1) switching cells. Thus, for m=5, there are 4 cells.

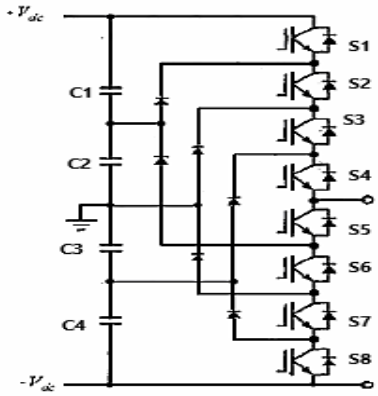


Fig 2. Single phase five level DCM inverter

WORKING:
In cell 1- S2, S3 and S4 are always ON whereas S1 and S5 are turned on alternatively to produce an output voltage of Vdc/2 and Vdc/4, respectively.
In cell 2- S3, S4, and S5 are always ON whereas S2 and S6 are switched on alternatively to produce an output voltage of Vdc/4 and 0.
In cell 3- S4, S5 and S6 are always ON whereas S3 and S7 are switched alternatively to produce an output voltage of 0 and –Vdc/2.
In cell 4- S5, S6 and S7 are always ON whereas S4 and S8 are switched alternatively to produce an output voltage of –Vdc/4 and –Vdc/2, respectively.

B. Three phase Cascaded H-bridge MLI.

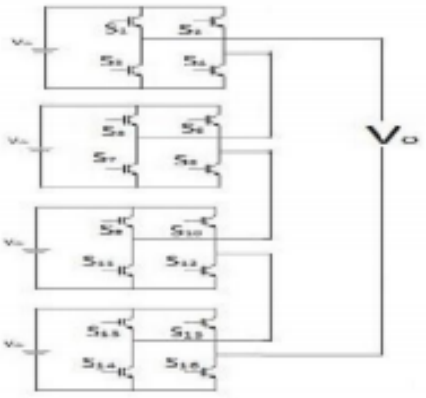


Fig 3. Single phase nine level CHB MLI

The CHB multilevel inverter have found wide application in high power inverters most importantly for its low total harmonic distortion (THD) and dv/dt. Cascaded multilevel inverter has a unique design and uses a smaller number of components which makes it an advantage.

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In this paper the Seven and Nine level three phase cascaded h-bridge multilevel inverters are proposed. The nine-level multilevel inverter is obtained by cascading four full bridge (H bridge) inverter circuit. It is similar to the seven level; the four full bridge inverters are connected in series and each full bridge is fed from separate dc source. This inverter does not require any voltage-clamping diode or voltage balancing capacitors unlike diode clamped inverter. Fig 3 shows the three phase nine level CHB inverter. There are four full bridges, each bridge has four switches therefore total 16 switches in single phase. To understand the operation, let us consider single phase

WORKING:
The S1, S2, S5, S6, S9, S10, S13, S14 switches are turned ON to get 0V.
The S1, S4, S5, S6, S9, S10, S13, S14 are turned ON to obtain voltage V.
The switches S2, S3, S5, S6, S9, S10, S13, S14 are turned ON to obtain -V.
The S1, S4, S5, S8, S9, S10, S13, S14 are switched ON to get the 2V.
The S2, S3, S6, S8, S9, S10, S13, S14 switches are turned ON to obtain -2V.
The switches S1, S4, S5, S8, S9, S12, S13, S14 should be ON to obtain 3V.
The switches S2, S3, S6, S7, S10, S11, S13, S14 are turned ON to obtain -3V.
The switches S1, S4, S5, S8, S9, S12, S13, S16 are turned ON to get 4V.
The S2, S3, S6, S7, S10, S11, S14, S15 are turned ON to obtain -4V.

## III. SIMULATION RESULT AND ANALYSIS

### A. THREE PHASE FIVE LEVEL DIODE CLAMPED INVERTER.

Five output-voltage levels of diode clamped MLI: 0, Vdc/4, Vdc/2, Vdc/2, Vdc/4, 0, -Vdc/4, -Vdc/2, -Vdc/2, -Vdc/4 are produced by proper selection of switching devices. The generated five output voltage levels switching sequence is as shown in Table-1. The given table is one of the possible switching sequences needed to generate the required level. Fig 4 shows the three phase five level diode clamped inverter, fig 5 shows the obtained THD as 30.81% and fig 6 is the output waveform.

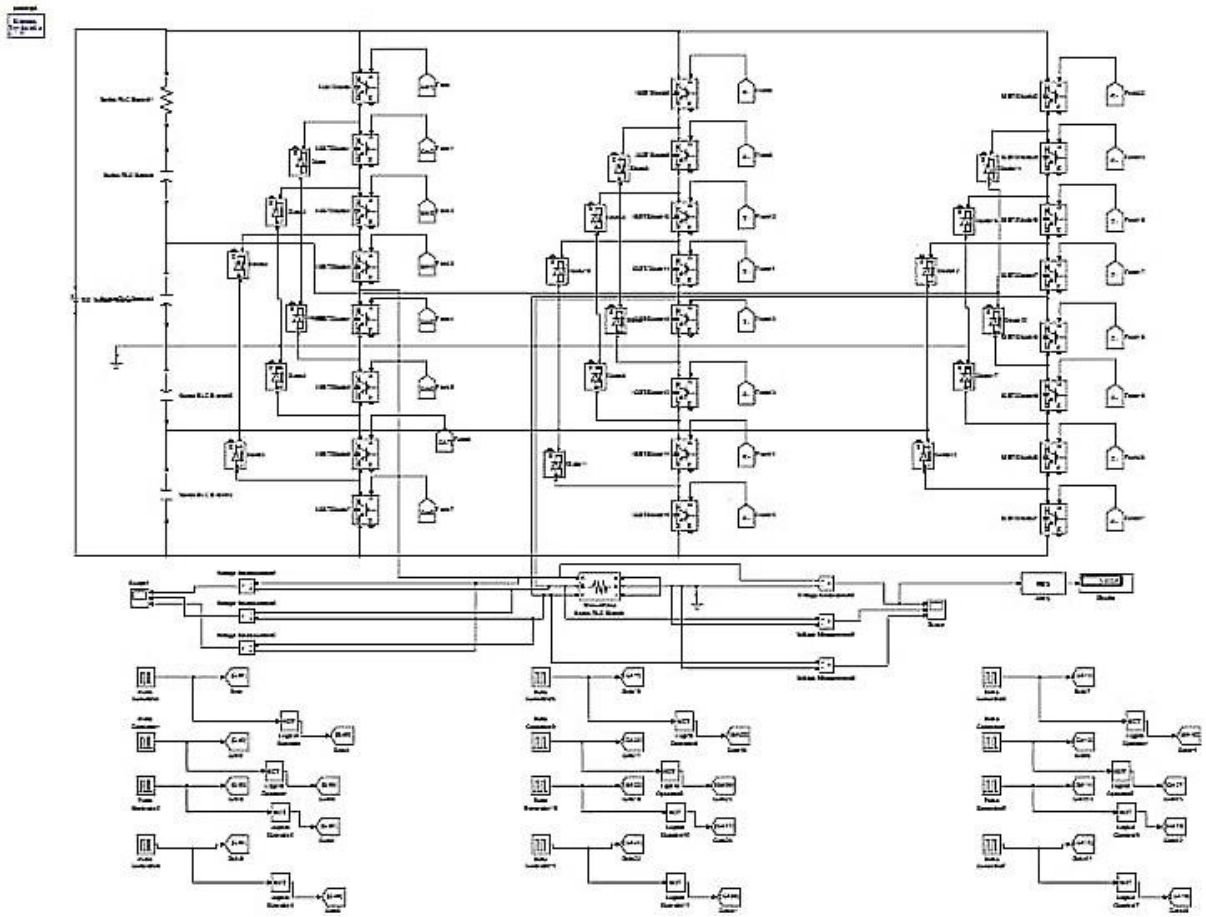

Fig 4. Three phase five level diode clamped inverter circuit.

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Table-1: Switching sequence of the five level DCMLI.

| Voltage levels | Switching sequence | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| Vdc/4 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| Vdc/2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Vdc/2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Vdc/4 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| -Vdc/4 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| -Vdc/2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| -Vdc/2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| -Vdc/4 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

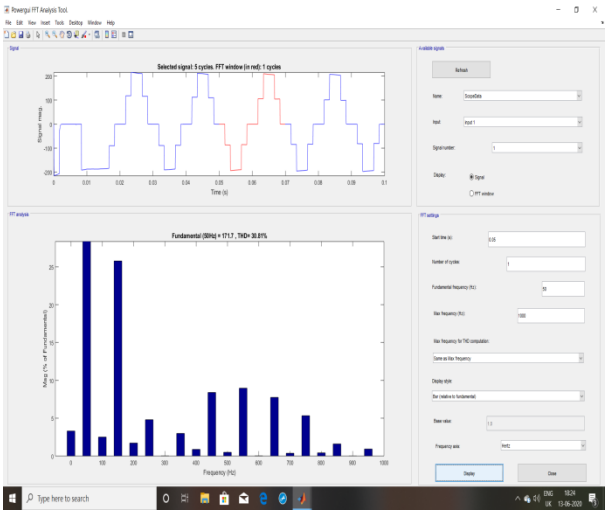

Fig 5. The THD analysis of the system.

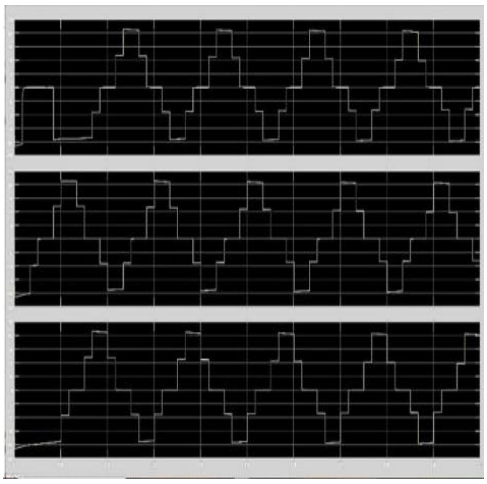

Fig 6. The three phase output waveform.

B. THREE PHASE SEVEN LEVEL CASCADED H-BRIDGE INVERTER.

Seven output voltage levels of cascaded h-bridge MLI: 0, V, 2V, 3V, 3V, 2V, V, 0, -V, -2V, -3V, -3V, -2V, -V are produced by the appropriate selection of switching devices. Fig 7 shows the simulated three phase seven level CHB inverter, fig 8 shows the obtained THD as 14.54% and fig 9 is the three-phase output waveform. The generated seven output voltage levels switching sequence is as shown in Table-2, which is one of the possible switching sequences to generate the required level.

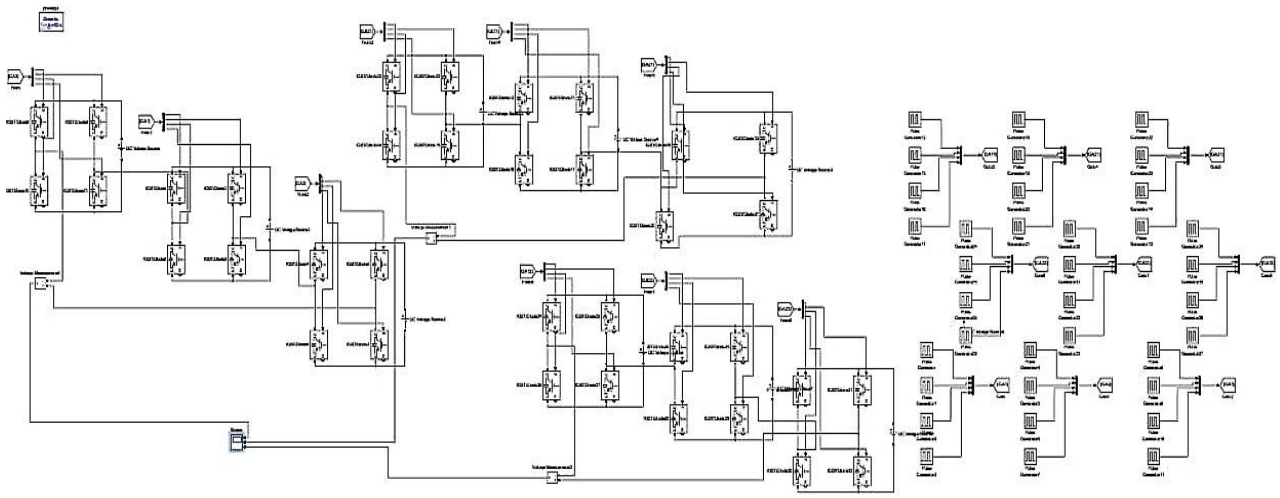

Fig 7. Three phase seven level CHB inverter circuit.

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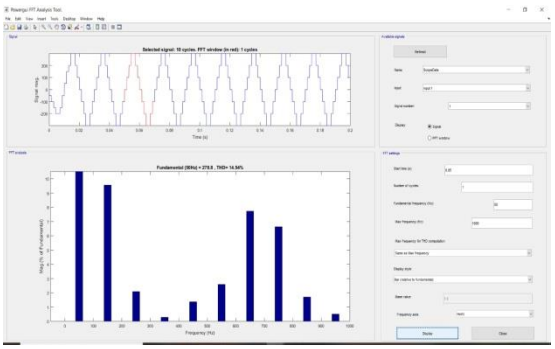

Fig 8.The THD analysis of the system

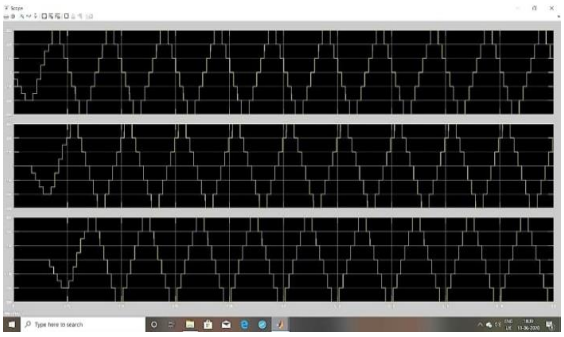

Fig 9.The three-phase output waveform.

Table-2: Switching sequence of the seven level CHB MLI.

| Voltage levels | Switching sequence | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| V | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 2V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 3V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 3V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 2V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| V | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| -V | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| -2V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| -3V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| -3V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| -2V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| -V | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

C. THREE PHASE SEVEN LEVEL CASCADED H-BRIDGE INVERTER.

Nine output voltage levels of cascaded h-bridge MLI: are produced by the selection of switching devices. The generated seven output voltage levels switching condition is shown in Table-3. In the given table, one of the possible ways of switching sequence is shown to generate the required level. The fig10 is MATLAB simulated model of three phase nine level CHB inverter, fig 11 shows the obtained THD as 6.81%, fig 12 is the nine-level output waveform.

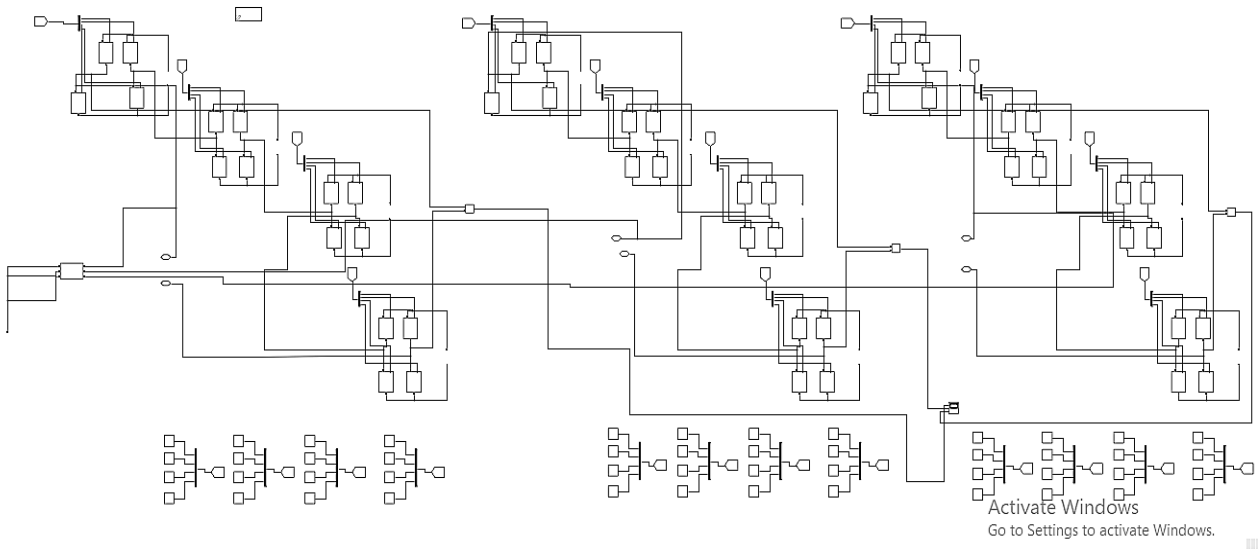


Fig 10. Three phase nine level CHB inverter circuit.

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Table-3: Switching sequence of the nine level CHB MLI.

| Sl. No. | Vdc | T11 | T12 | T13 | T14 | T21 | T22 | T23 | T24 | T31 | T32 | T33 | T34 | T41 | T42 | T43 | T44 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 2 | V | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 3 | 2V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 4 | 3V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 5 | 3V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 6 | 4V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 7 | 4V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 8 | 3V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 9 | 3V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 10 | 2V | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 11 | V | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 12 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 13 | -V | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 14 | -2V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 15 | -3V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 16 | -3V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 17 | -4V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 18 | -4V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 19 | -3V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 20 | -3V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 21 | -2V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 22 | -V | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

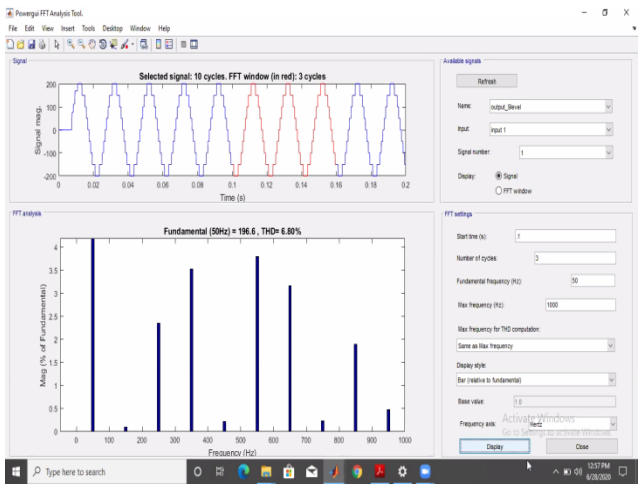


Fig 11.The THD analysis of the system.

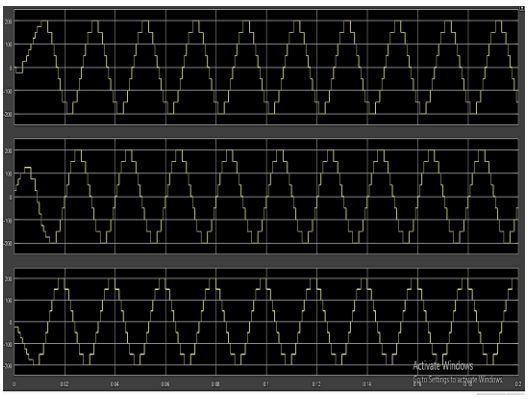

Fig 12.The three phase output waveform.

D. COMPARISON

The below table shows the comparative study of all the above mentioned types of three phase multilevel inverters simulated above.

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Table-4: Comparative study

| SL.NO. | Parameter | DIODE CLAMPED | CASCADED H-BRIDGE | CASCADED H-BRIDGE |
|---|---|---|---|---|
| 1 | Output levels | 5 | 7 | 9 |
| 2 | Total no. of switches | 24 | 36 | 48 |
| 3 | Number of DC sources | One DC source of 100V | Three DC source of 100V | Four DC source of 100V |
| 4 | THD | 30.81% | 14.54% | 6.81% |
| 5 | Type of load | RESISTIVE LOAD | RESISTIVE LOAD | RESISTIVE LOAD |

## IV. CONCLUSION

From all the above discussion, it can be concluded that multilevel inverters with proper switching angle and conduction period can eliminate considerable amount of harmonics and further THD can be even more reduced by adding filters of proper frequency. The major scope of this work in the future is the hardware implementation for both domestic and industrial purposes. It is possible to realize different power electronics system applications such as drives, EV's and etc and also it can be made more cost effective by implementing it with digital signal controller.

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