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# A Novel Design and Analysis of Reversible Carry Look Ahead Adder using VHDL and Quantum Dot Cellular Automata

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**Abstract:** Carry-Look Ahead adder is one of the essential components used in different digital logic circuits for its fast and efficient computation capability. This paper primarily focuses on the design and simulation of 4-bit CLA adders which are implemented using two different technological perspectives, the conventional CMOS technology using VHDL and Quantum Computing using Quantum-dot Cellular Automata (QCA). Both designs are based on reversible logic to reduce heat dissipation, better testing of faults in circuits, and nearly energy-free computation. VHDL has been the most effective hardware descriptive language when it comes to digital circuit designs but with the advancement of technology, implementation of circuits using QCA is considered an alternative approach. This research work will impart an in-depth comparison between the two domains of technology on one of the most useful combinational logic circuits, the CLA Adder.

**Keywords:** CLA Adder, Quantum Cellular Automata, VHDL, Reversible Logic Gates.

## I. INTRODUCTION

Modern VLSI systems have a higher rate of power dissipation due to the intensity of switching of the internal signals. In the year 1960, R. Landeur stated that kT*log2 joules of energy are released for each lost bit in an irreversible logic computation where k stands for Boltzmann's constant and T is the temperature at which the said process takes place [1]. Thus, an important criterion for efficiency is dissipation of low heat while operation can be fulfilled by using reversible gates. This is due to the bijective property of these gates.

A Carry-look ahead adder or fast adder is used to curb propagation delay generated in full adders. In comparison to full adder, CLA adder is more effectual in terms of operational speed despite more complexity in its circuit. It improvises the speed by eliminating the carry bit propagation at each step of computation.

CMOS VLSI Technology has put its remarkable contribution in designing low power circuits. In the design, one of the most important tools that is required to design, simulate and synthesis is VHDL. VHDL or Very High-Speed Integrated Circuit Hardware Description Language is a hardware language which is used in digital IC's for implementation of circuit designs. It enables us to make minimum abstraction gate level designs. VHDL gives a text-based model which is used to describe a logic circuit [2]. This model is a synthesizable block of code using which hardware components can be made. This synthesized code is simulated using a bunch of simulation models which is known as the test-bench model and the results are displayed for logic circuits that interfaces to the design. It is an integrated amalgamation of languages like sequential, concurrent, net-list, timing and waveform generation. So VHDL is assembled to perform all such functionality of the above-mentioned languages. This hardware description language will be extensively used in this paper to design and synthesis logical code blocks in the domain of CMOS Technology.

On the other hand, Quantum Computing [3] has seen substantial growth in recent years, due to its faster processing speed and the less spatial requirement for circuit integration as compared to the traditional CMOS Technology. QCA which is an abstract model of Quantum Computing can be used in the design of integrated circuits. Designs based on QCA consume less power due to the fact that they represent logic states through qubits unlike conventional CMOS using voltage representations [4]. A qubit or quantum bit is the basic unit of information in Quantum mechanics. It is a modular approach to circuit design which is more compact and efficient. The relative evaluation on the designs of CLA adder using reversible logic gates between CMOS Technology and Quantum Computing Technology will be provided in this paper. It will comprise certain parametric comparison between the two domains as shown in VHDL & QCA Designer [5].

## II. IMPLEMENTATION IN VHDL & QCA

The designs in VHDL are shown by the RTL schematics in Fig. 1, 2 and 3 for MTSG [6], HNG [7] and PTR [8] gates respectively. The shown figures are architectural model of the reversible 4-bit CLA adder using the different gates. It



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shows the various gates used along with the connections, output and garbage outputs. Here the term Garbage outputs solely imply that those outputs do not take part in this particular design and not useless at all. The designs in QCA are implemented using the QCA designer tool and the diagrammatic representation of the circuitry are shown in fig 4, 5 and 6 for MTSG, HNG and PTR respectively.

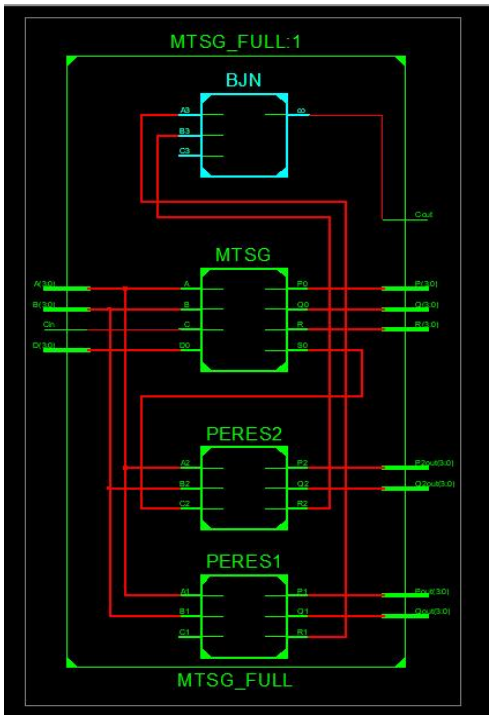


*Fig 1: RTL Schematic of CLA Adder using MTSG gate*

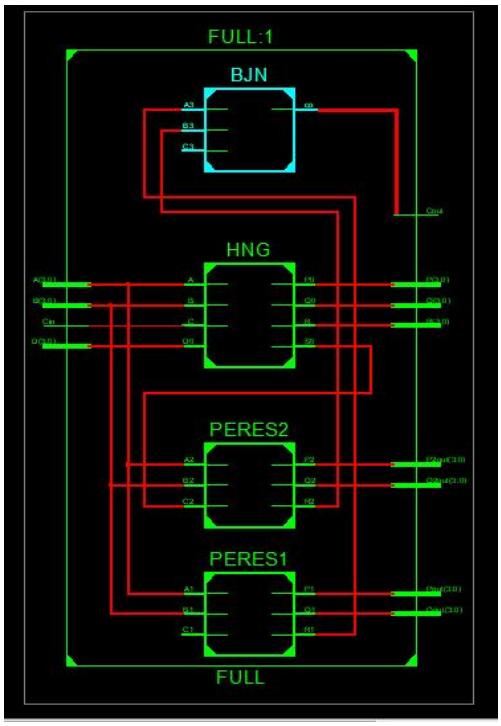


*Fig 2: RTL Schematic of CLA Adder using HNG gate*

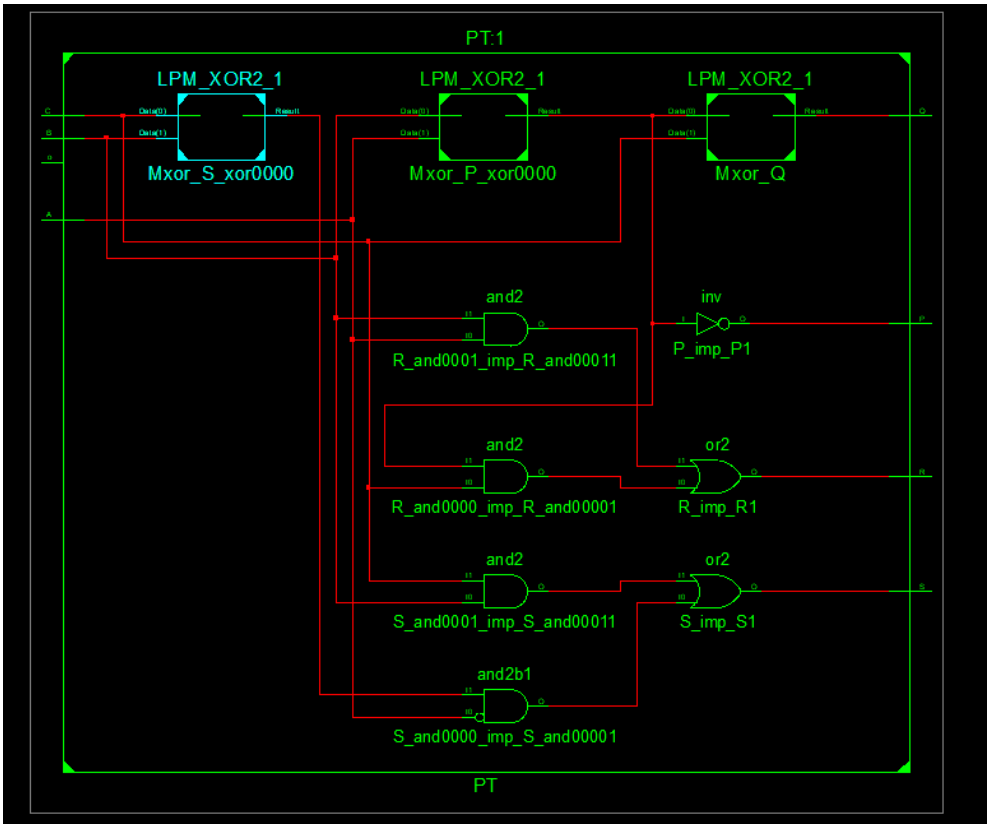


*Fig 3: RTL Schematic of CLA Adder using PTR gate*



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*Fig 4: QCA Implementation of 4 BIT CLA Adder using MTSG gate*

*Fig 5: QCA Implementation of 4 BIT CLA Adder using HNG gate*

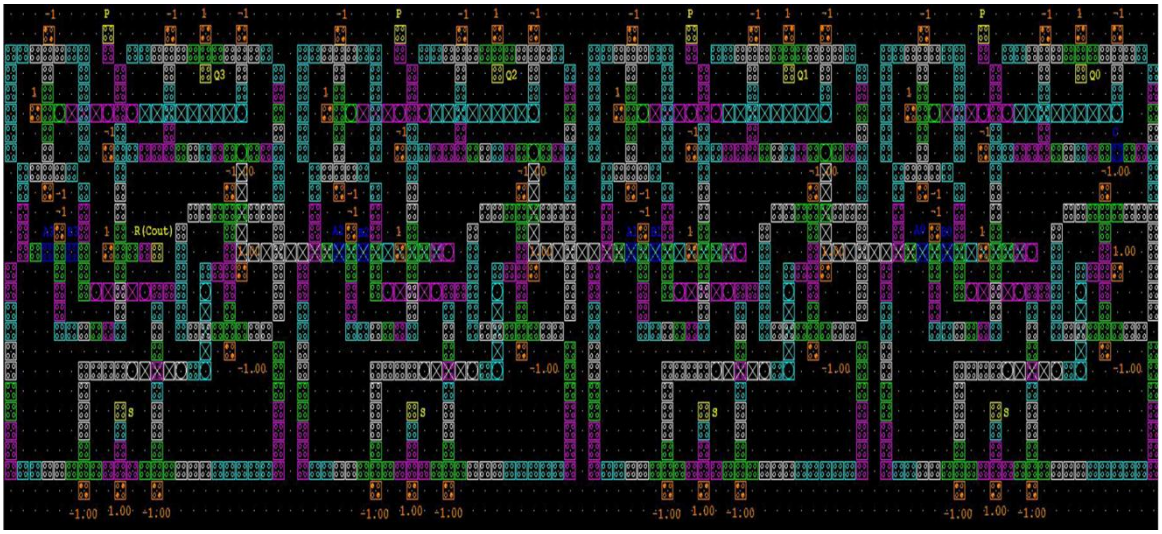

*Fig 6: QCA Implementation of 4 BIT CLA Adder using PTR gate*



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## III. RESULTS AND DISCUSSION

Table 1 describes the parameters generated while execution of a CLA adder in VHDL. The number of gates used by MTSG and HNG are 4, which includes MTSG/HNG respectively along with two Peres [9] and a BJN [10] gates. In case of PTR, there is only one gate used. The simulation time for each proposal are 1 us, which make VHDL a time efficient approach. The memory used the above mentioned 3 proposal are very less i.e. 29524 kb for MTSG and HNG and 30272 kb for PTR. The target device used in our proposal is xc3s400-5pq208.

*Table 1: Simulation parameters of VHDL*

| Gates | No. of gates used | Simulation time(μs) | Memory used(kB) |
|---|---|---|---|
| MTSG | 4 | 1 | 29524 |
| HNG | 4 | 1 | 30272 |
| PTR | 1 | 1 | 29992 |

*Table 2: Simulation parameters of QCA Designer*

| Gates | No. of cells used | No. of gates used | Clock cycle | Area required ($\mu m^2$) |
|---|---|---|---|---|
| MTSG | 1674 | 3 | 99 | 1.58 |
| HNG | 1674 | 3 | 99 | 1.58 |
| PTR | 1135 | 1 | 400 | 1 |

From the above table we can deduce that the number of cells required for realizing a CLA adder using MTSG and HNG are 321 and the both of them uses 3 reversible gates which are MTSG/HNG, Feynman [11]and BJN gates but in case of PTR only 265 cells and 1 reversible gate is required. This add as a benefit as the number of reversible logic gates required are very less.

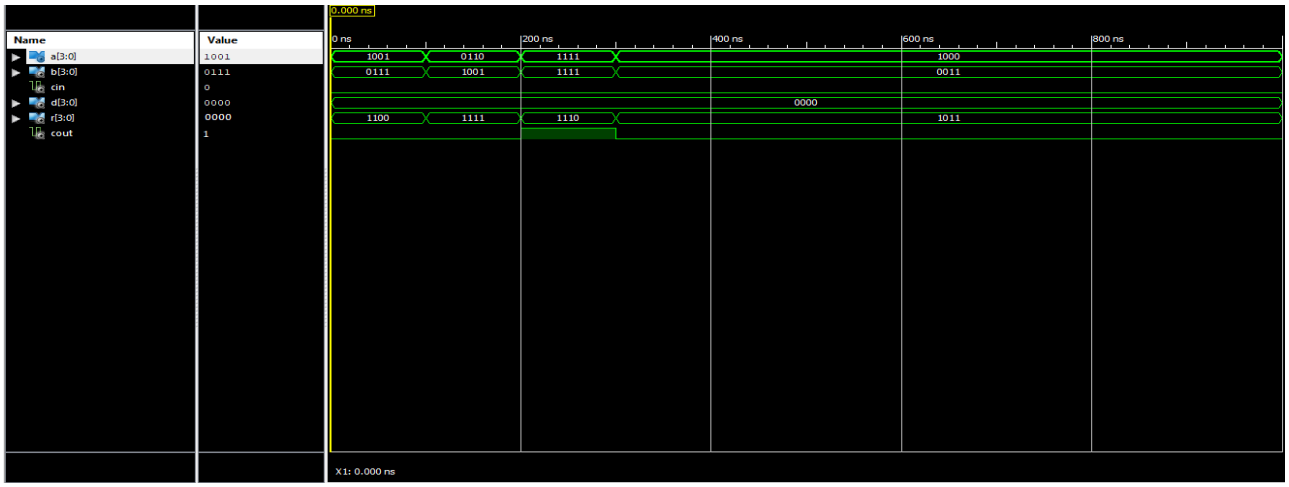


*Fig 7: Simulation of CLA Adder using MTSG Gate in VHDL*

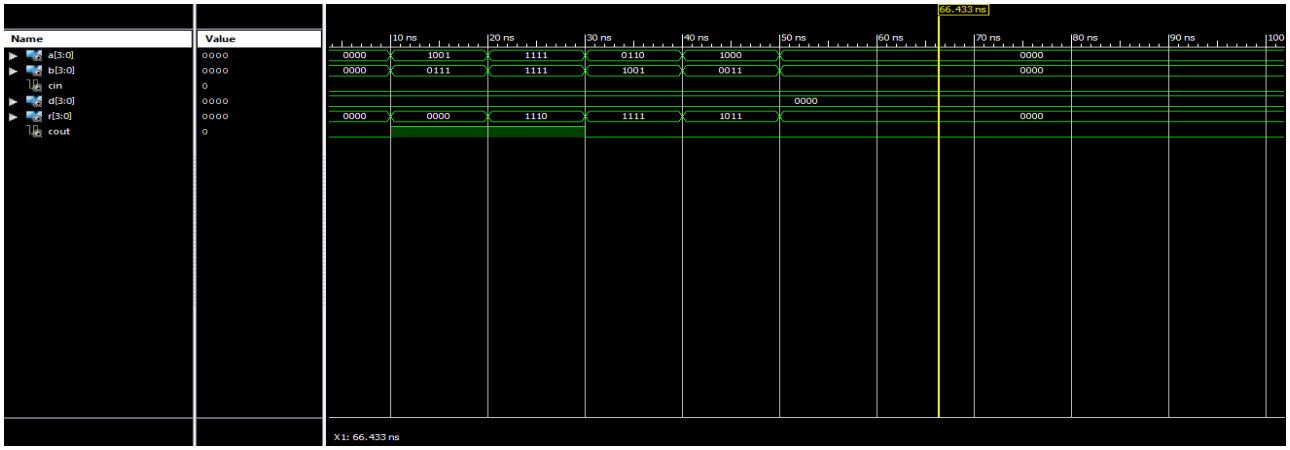


*Fig 8: Simulation of CLA Adder using HNG Gate in VHDL*



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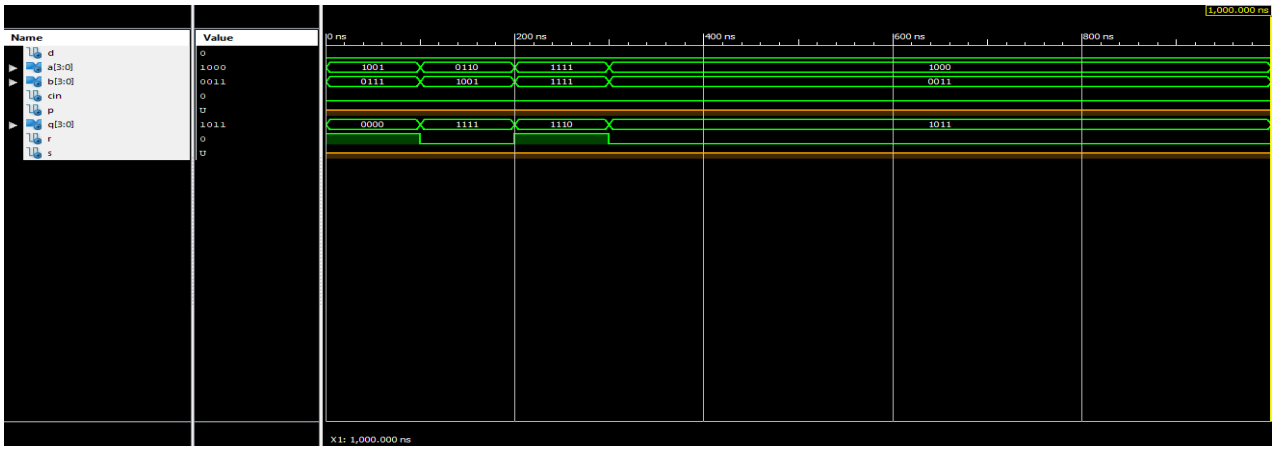


*Fig 9: Simulation of CLA Adder using PTR Gate in VHDL*

Furthermore, the delay produced by MTSG, HNG and PTR are of 99, 99 and 400 clock cycles respectively. This delay is produced due to one of the properties of quantum computing i.e. the output from previous block and the input to the next block have to be synchronous. The area required by above mentioned three gates also plays an important role and therefore the area of each are 1.58 $um^2$, 1.58 $um^2$ and 1 $um^2$.

## IV. CONCLUSION

It is quite evident from the above work that both the designs have their own fair share of pros and cons. There are several noticeable differences between the two. Firstly, In VHDL architecture we can see the total number of gates used is one more than that used in QCA for MTSG and HNG gates. This makes the circuit slightly more complex than that in QCA due to the increment of garbage outputs. In QCA however this is not the case as we use only three gates for the circuit design. Secondly, in case of QCA one major drawback is the clock synchronization which takes place when the bits travel from one gate to another. This is the sole reason why there are fewer applications of CLA adders in QCA domain. But design dimensions also play a role in efficient circuit designs which is where QCA takes an edge as circuit minimization in VHDL is not possible after an approximate range of 0.7nm but there are no such limitations in QCA.

## ACKNOWLEDGMENT

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