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Optimized ALU with BIST Implementation using Encounter Platform

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Abstract: This paper provides an Optimized Arithmetic Logical Unit (ALU) with BIST capability, ALU comprising of different arithmetic operations and logical operations is implemented. ALU is used in many processing and computing devices, due to rapid development of technology not only the faster arithmetic unit is required but also less area and low power arithmetic units are needed and due to the increasing integration complexities of IC's the Optimized ALU implemented sometimes may malfunction, so testing capability must be provided and this is accomplished by Built In Self-Test (BIST) for Optimized ALU. In this project the implementation will be done in Encounter platform.

Keywords: ALU, BIST, Vedic Algorithm, Cadence Encounter, Xilinx.

I. INTRODUCTION

Arithmetic Logic Unit (ALU) is an important and necessary unit present in every processor and all computing devices performing arithmetic operations like addition, subtraction, multiplication, increment, decrement, shifting and logical operations like and, or, not, exor. The ALU must be optimized and when manufactured they might have defects or might be faulty hence to increase testability Design for Testability (DFT) must be provided one such methodology is Built-In-Self Test (BIST). BIST technique provides little cost, a well-defined increase in the testability of the Circuit Under Test (CUT). The test pattern generator is a part of BIST implemented using Linear feedback Shift Register (LFSR), this increases the testability of ALU.

II. PROPOSED METHOD AND IMPLEMENTATION

Optimized ALU implementation for increasing speed and decreasing power and delay, fast adder like Carry Save Adder is implemented and fast multiplier like Vedic multiplier one of the vedic techniques is implemented, by using particular adder and multiplier units area, power and delay optimization is achieved in ALU. BIST uses test pattern generators to generate test patterns then these test patterns are applied to circuit under test that is ALU and the output is analysed and the functionality is tested.

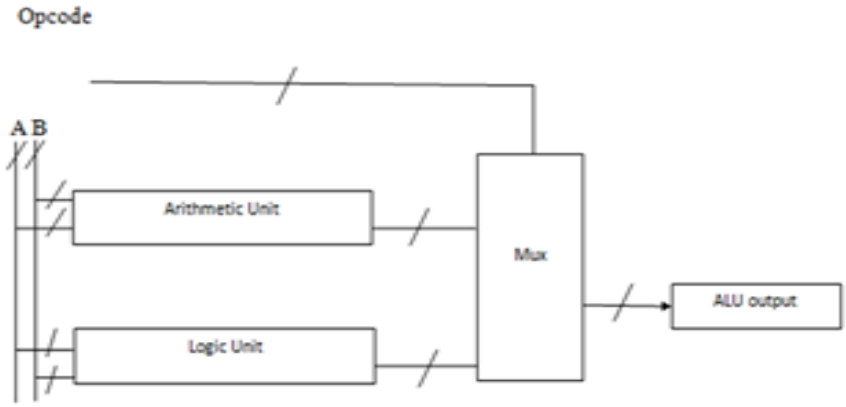

Fig1:ALU Architecture

Using carry save addition, the delay can be reduced. The methodology is to take 3 numbers that we want to add together, x + y + z, and convert it into two numbers c + s such that x + y + z = c + s, will be computed in short time. In carry save addition, we directly pass carry to final step.

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X:	1 0 0 1 1		X:	1 0 0 1 1		X:	1 0 0 1 1
Y:	+ 1 1 0 0 1		Y:	+ 1 1 0 0 1		Y:	+ 1 1 0 0 1
Z:	+ 0 1 0 1 1		Z:	+ 0 1 0 1 1		Z:	+ 0 1 0 1 1
S:	0 0 0 0 1		C:	1 1 0 1 1		S:	0 0 0 0 1
						C:	1 1 0 1 1
						Sum:	1 1 0 1 1 1

Fig2:CSA addition

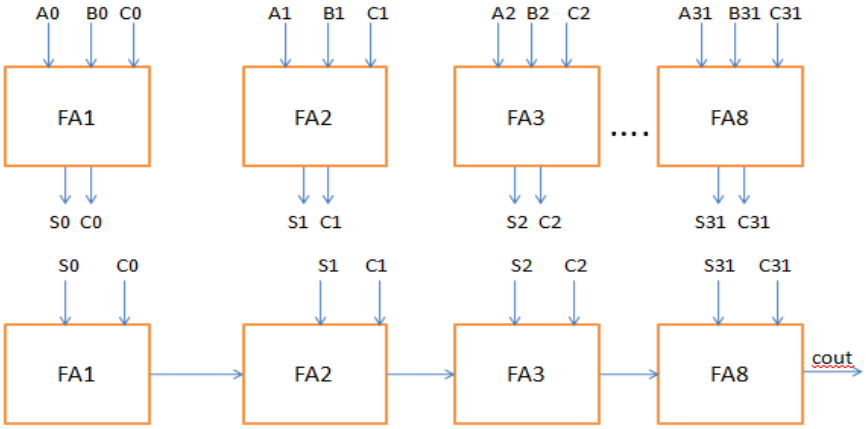
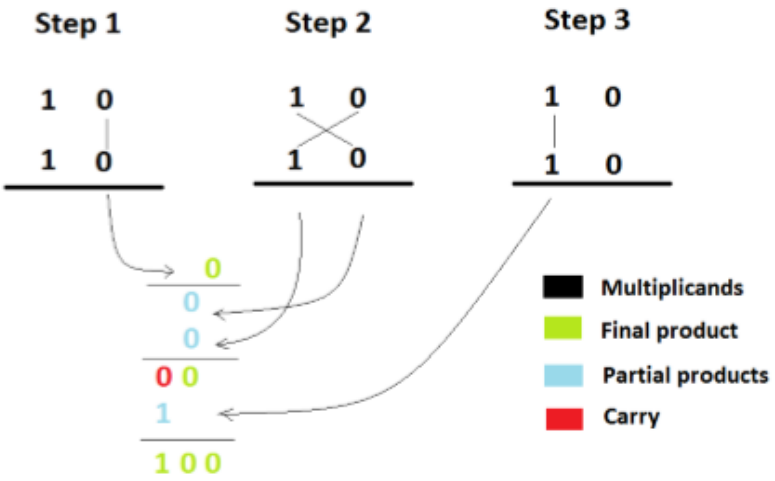


Fig3:CSA Architecture

Sl.No	Adder	Delay
1	CLA	648ps
2	CSA	144ps

Fig4: Comparision of adders

Subtraction: The 2's Complement Addition technique is used for subtraction, as adder block is optimised using carry save adder ,subtraction unit is also optimised.Multiplier unit is optimized using Vedic Multiplier technique this increases speed and decreases power.



2x2 Multiply Block

Fig5:Mutiplier Representation

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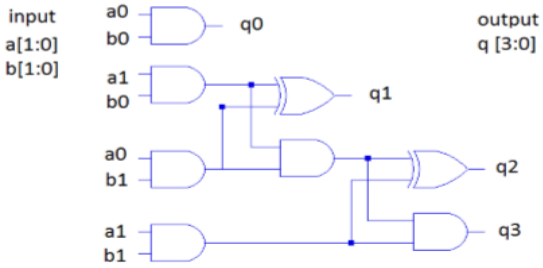


Fig6:2×2 Multiplier hardware representation

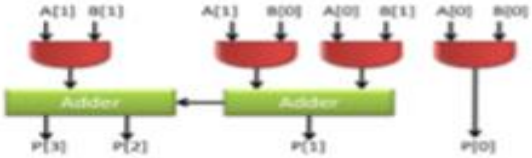
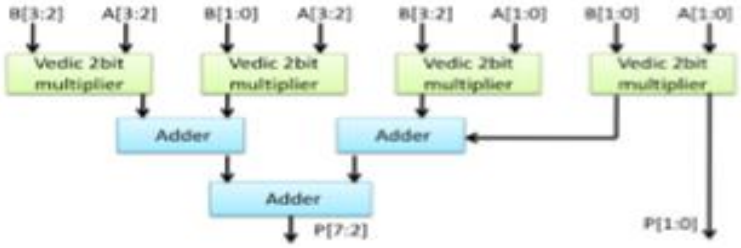


Fig 1. A 2x2 Vedic multiplier



4-bit Vedic multiplier using 2-bit multipliers

Fig7:4 bit multiplier

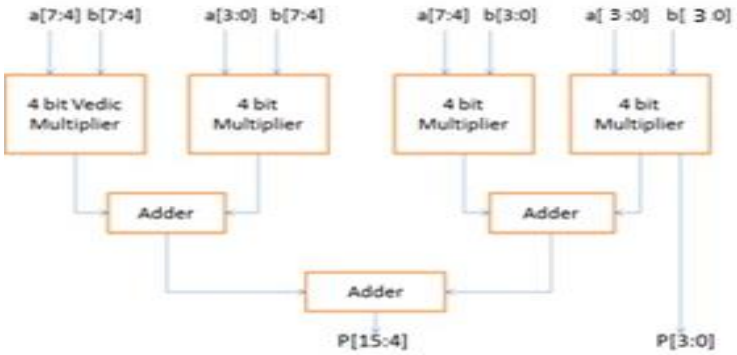


Fig8:8bit Multiplier

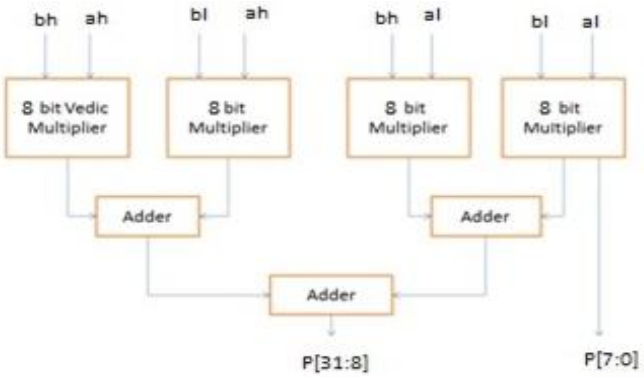


Fig9:16 bit multiplier

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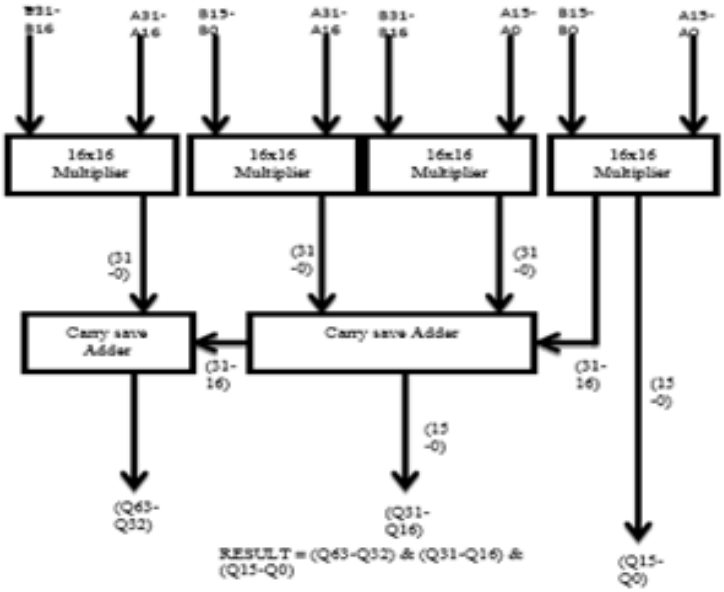
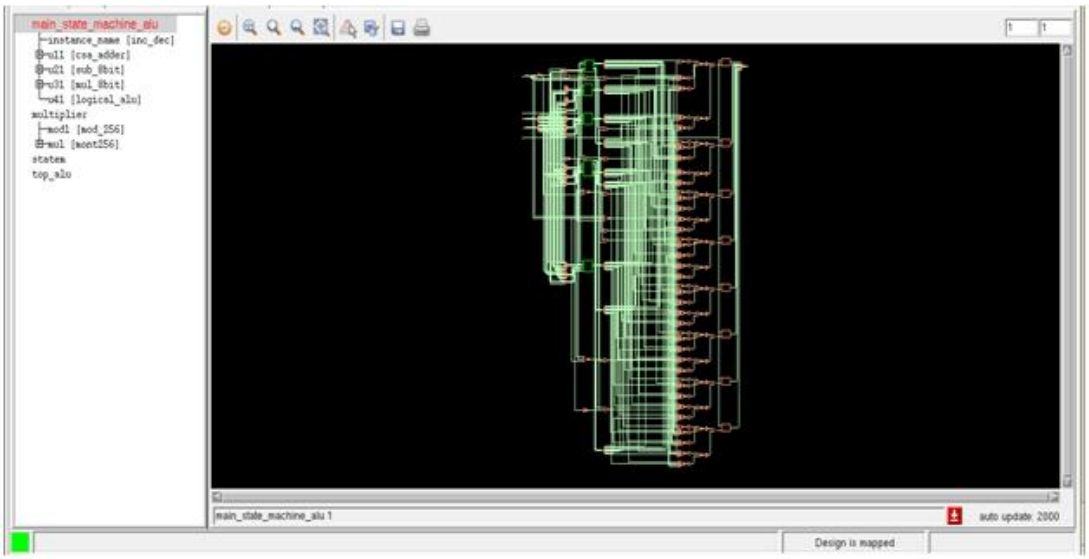


32 bit multiplier

Cell Area	Delay
1525	1139ps

Multiplier area and delay



Optimized ALU

After designing and implementing Optimized ALU , BIST has to be implemented, the diagram of BIST is as shown in the diagram, it has BIST controller which selects whether it should work either in testing mode or normal mode ,it has test pattern generators like LFSR linear feedback shift register which generates test patterns these test patterns are applied to circuit under test that is optimized ALU over here then the result obtained is analysed and checked for correctness of ALU. LFSR is an n-bit shift register which randomly produces test vectors till 2n-1 very quickly due to minimum usage of combinational.
logic. The usage of exclusive-OR gates and shift register produces binary sequence at each flip-flop. By proper selection of points at which we take the feedback from an n -bit shift register we can produce a PRBS of length 2n – 1, that includes all possible patterns of n bits, in which all-zeros pattern is excluded. In an LFSR, the bits at selected positions of shift register are fed back into the register's input bit.

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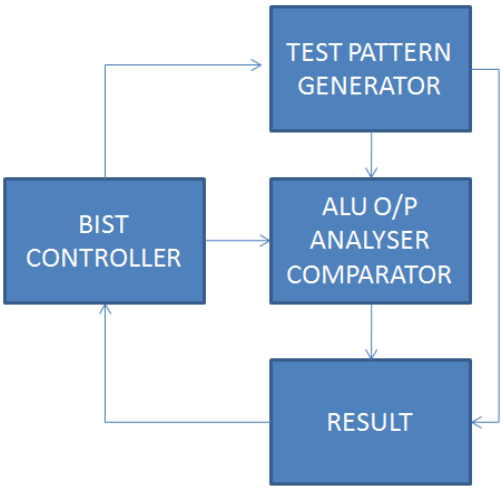

BIST

III. CONCLUSION

In this paper we have implemented Optimized ALU with BIST capability which has lesser area,power and delay implemented using carry save adder and vedic multiplier with testing capability provided by Built in Self Test provides testing capability.

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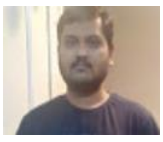
BIOGRAPHY



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