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VLSI Design of reversible Arithmetic and Logic Unit (ALU) using Verilog HDL

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Abstract: Reversible rationale is broadly being considered as the potential rationale configuration style for usage in present day nanotechnology and quantum registering with insignificant effect on physical entropy. Late advances in reversible rationale take into consideration improved quantum PC calculations and plans for comparing PC models. Huge commitments have been made in the writing towards the plan of reversible rationale door structures and number juggling units, nonetheless, there are very few endeavors coordinated towards the plan f reversible ALUs. In this paper, we propose the plan of two programmable reversible rationale door structures focused at ALU usage and their utilization in the acknowledgment of a productive reversible ALU is illustrated. The proposed ALU configuration is checked and its points of interest over the main existing ALU configuration are quantitatively dissected.

Keywords: VLSI,HDL,ALU,reverse concepts

I. INTRODUCTION

Reversible rationale is helpful in mechanical uses of nanotechnology, given that the erosion created by reaching corpuscles inside a restricted volume can be essentially decreased by taking out sliding contact utilizing mechanical reversible rationale [4]. What's more, reversible rationale is additionally relevant to fields, for example, quantum registering, since the laws of quantum material science are time reversible [5], and the bijection between the information and yield states empowers probabilistic calculations.

Any math rationale unit must have the option to deliver a assortment of rationale yields dependent on inputs dictated by the developer for execution in a guidance set engineering. Accordingly, reversible rationale gadgets utilized in an condition must have both fixed select information lines that get opcode signals controlled by the software engineer and changeless yield lines where the consequence of the consistent yield is created.

In this paper, we initially portray a few nuts and bolts of reversible rationale, present a few primers including a few definitions furthermore, hypotheses identified with programmable reversible rationale. Second, two novel 4*4 reversible rationale doors are proposed with negligible postponement, and might be designed to deliver a assortment of sensible computations on fixed yield lines dependent on programmable select info lines. Third, the plan of a reversible ALU is given which is executed the proposed doors and dissected.

II. REVERSIBLE LOGIC GATES

Feynman / CNOT Gate:

The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q= A^B) .

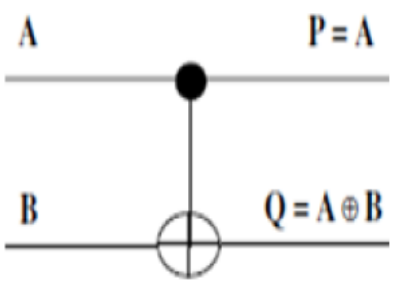

Fig 2.1 Reversible Feynman/CNOT gate (FG)

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2.1Truth Table For CNOT Gate

INPUT		OUTPUT	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fredkin gate

The Fredkin gate (also CSWAP gate) is a computational circuit suitable for reversible computing, invented by Ed Fredkin. It is universal, which means that any logical or arithmetic operation can be constructed entirely of Fredkin gates. The Fredkin gate is the three-bit gate that swaps the last two bits if the first bit is 1.

Definition

The basic Fredkin gate[1] is a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B ⊕ AC and R=A′C ⊕ AB. Quantum cost of a Fredkin gate is 5.

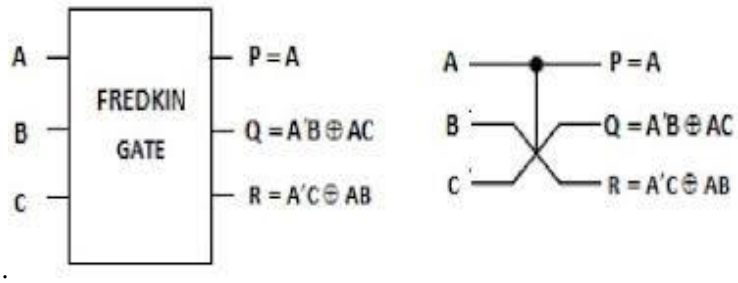

Fig 2.2 Reversible Fredkin Gate

The Fredkin gate is the reversible three-bit gate that swaps the last two bits if the first bit is 1.

Truth table Matrix form

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

2.2 Truth Table For Fredkin Gate

It has the useful property that the numbers of 0s and 1s are conserved throughout, which in the billiard ball model means the same number of balls are output as input. This corresponds nicely to the conservation of mass in physics, and helps to show that the model is not wasteful.In computer science, the Toffoli gate (also CCNOT gate), invented by Tommaso Toffoli, is a universal reversible logic gate, which means that any reversible circuit can be constructed from Toffoli gates. It is also known as the “controlled-controlled-not” gate, which describes its action.

Any reversible gate must have the same number of input and output bits, by the pigeonhole principle. For one input bit, there are two possible reversible gates. One of them is NOT. The other is the identity gate which maps its input to the output unchanged. For two input bits, the only non-trivial gate is the controlled NOT gate which XORs the first bit to the second bit and leaves the first bit unchanged.

Unfortunately, there are reversible functions that cannot be computed using just those gates. In other words, the set consisting of NOT and XOR gates is not universal. If we want to compute an arbitrary function using reversible gates,

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we need another gate. One possibility is the Toffoli gate, proposed in 1980 by Toffoli.This gate has 3-bit inputs and outputs. If the first two bits are set, it flips the third bit. The following is a table of the input and output bits:

Truth table Permutation matrix form

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

2.3 Truth Table Of Toffoli Gate In Permutation Form

It can be also described as mapping bits a, b and c to a, b and c XOR (a AND b).

The Toffoli gate is universal; this means that for any Boolean function f(x1, x2, ..., xm), there is a circuit consisting of Toffoli gates which takes x1, x2, ..., xm and some extra bits set to 0 or 1 and outputs x1, x2, ..., xm, f(x1, x2, ..., xm), and some extra bits (called garbage). Essentially, this means that one can use Toffoli gates to build systems that will perform any desired Boolean function computation in a reversible manner.

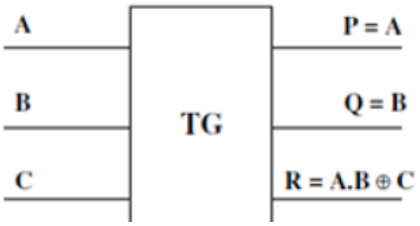

Fig.2.3 Reversible Toffoli Gate

III. ARITHMETIC LOGIC UNIT

Design of ALU using Proposed Gates

Two 1-bit ALUs are presented in this section. The first utilizes the MRG gate and HNG gate to produce six logical calculations: ADD, SUB, XOR, XNOR, OR and NOR. The ALU has 8 inputs and 8 outputs. The inputs consist of three data inputs (A, B and Cin) and five fixed input select lines. The eight outputs are: A, S0, S3 and S4 propagated to the output, A __B, SUM, Cout, Overflow and Result. The cost of this 1-bit ALU is 24, and the worst-case delay is 16. For nbit ALU devices, an addition cost of 2 is incurred per bit in order to propagate S1 and S2 to other bits. Therefore, the total cost for an n-bit ALU is 26n-2.

IV. RESULTS AND DISCUSSION

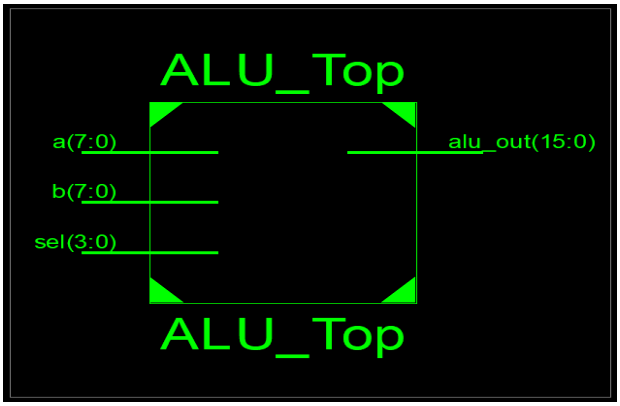

Fig 4.1. Top level Block

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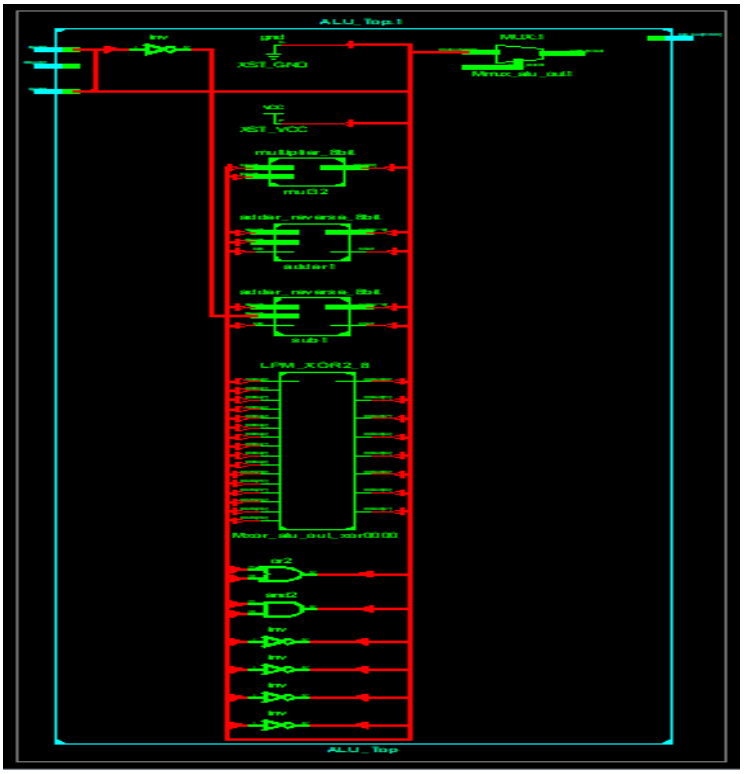

Fig 4.2. RTL Schematic

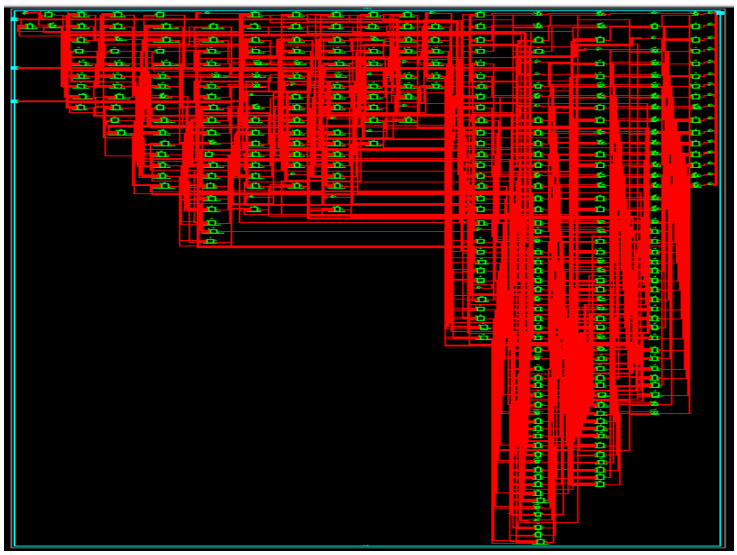

Fig 4.3. Technological Schematic

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	137	4656	2%
Number of 4 input LUTs	251	9312	2%
Number of bonded IOBs	36	232	15%

Fig 4.4. Design summery

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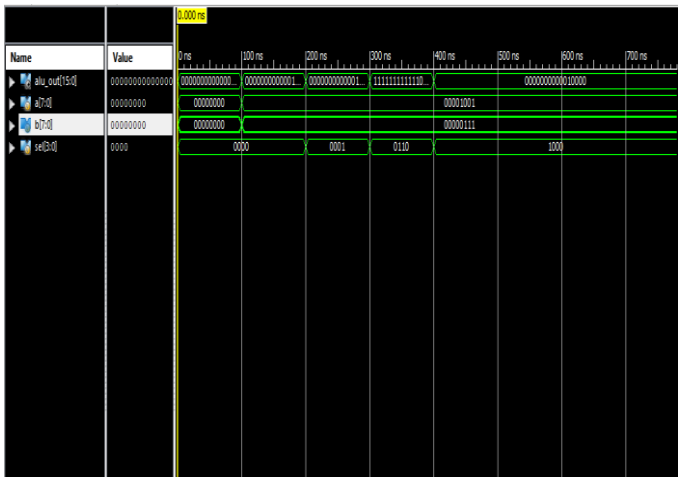

Fig 4.5. Simulation output

V. CONCLUSION

The idea of a programmable reversible rationale structure and hypotheses were recommended that present new measurements for reversible rationale structure. Two profoundly programmable, minimal effort and low-defer 4*4 reversible rationale doors were introduced, checked and contrasted with comparable rationale structures previously distributed. The proposed MRG and PAOG coordinated the HNG as the best existing 4*4 reversible doors in terms of cost, delay and legitimate yield counts. The entryways were then executed in reversible math rationale units. These new ALU plans are favorable to recently distributed work in executions that favor low postponement and high consistent count yield, which is alluring for acknowledgment of a reversible focal preparing unit.

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