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An Elaborated Study of DC-DC Buck Regulator Based Small Signal Model and Lag Lead Compensator with Sign Inverter

Mohamed A. A. Abdel-Rahman

Electrical Engineering Department, Faculty of Engineering, Al-Baha University, Al-Baha, Saudi Arabia

Abstract: The objective of this paper is to present a detailed study to design, model and simulate buck regulator with an analog lag lead compensator cascaded by sign inverter, then transpose into its equivalent digital form. The ease of implementation and the advantages given by the adaptability to the changes in the closed loop enable the digital controllers to become widely used during the last few decades. This is attributed to the tremendous growth in integrated circuits (ICs) technology and skyrocketed development in semiconductor devices which in turn fulfill the highly demanded microprocessors to more current at low voltages. Specifically, they received special attention in different applications such as renewable energy sources, Switched Mode Power Supplies (SMPS), drive systems, and High-Voltage DC (HVDC) transmission, etc. We have performed two algorithms, the first to design analog compensator aiming at achievement of specified requirements while the second to obtain the six transfer functions concerning the various (state/input/output) variables of the buck converter based on the small signal and averaged state space models. This facilitates obtaining an appropriate equivalent digital compensator using Bilinear Z-Transform (BZT), Matched Pole-Zero (MPZ) and Zero Order Hold (ZOH) methods. Also, simulative results have been depicted via MATLAB/Simulink model utilizing SimElectronics Toolbox. Moreover, these models represented by the state and output equations, enable the other modeling approaches to be computationally implemented. A special emphasis of our work is placed on the circuit and transfer function models. In addition, the dynamic response of our intended compensator under input voltage change and load current variations is illustrated. Simulation results ensure that the output voltage and inductor current can return to steady state even when they are affected by such variations, with a small overshoot and settling time for the investigated waveforms. As a result of the above, a precise and robust closed loop controller that can satisfy high degree of stability and performance conditions of the DC-DC synchronous buck regulator has been accomplished. Finally, the performed algorithms have paved the way towards practical implementation by microcontroller /DSP controller/ FPGA controller. In case of a change in converter parameters, the new values of the z-coefficients for the digital compensator are evaluated and programmed by software and no need for the designer to solder or redesign the printed board which is in opposite to the analog compensators.

Keywords: State-Space Averaging Model; Lag Lead Compensator; SMPS Regulator; Transfer Function Model; Input voltage and Load Variations; Bilinear Z-Transform (BZT); MPZ and ZOH Methods

I. INTRODUCTION

The general procedures addressed by the researchers [1,2,3,4] to derive the s-domain transfer functions for power converters (Buck-Boost-Buck Boost) including the modulator, switching circuit and the output filter can be summarized as: a) analyzing the physical model for the two duration periods ($T_{on} = d \cdot T_{sw}$ and $T_{off} = (1-d)T_{sw}$) to obtain the state space and output equations derived by using the Kirchhoff's voltage law applied to the external loop and the Kirchhoff's current law applied to the output node. b) providing an averaged model by adding the state and output equations corresponding to the two durations of part (a) in which the time variance is removed, c) pointing out the steady state model by putting the derivative of equilibrium variables to zero, d) substituting each one of the input, control, output and state variables by the additive steady state and small signal components ($d = D + \hat{d}$) in the averaged model of part (b), e) removing the steady state model as well as the multiplicative terms of any two small signal components and keeping the small signal ones, f) obtaining the six-domain transfer functions by taking Laplace transform according to the intended variables shown in table-1. Switched Mode Power Supplies (SMPS) are becoming common place and have replaced in most cases the traditional linear ac-to-dc power supplies as a way to reduce power consumption, heat dissipation, size and weight. SMPS can now be found in most PC's, power amplifiers, TV's, DC motor drives,… etc., A state space averaging methodology is a mainstay of modern control theory because it provides insights on zero state response and zero input response. Many authors have analyzed the transient performance of

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power converter for buck regulator using mathematical model, circuit model, state space model and transfer function model [5-13]. In our study we concentrated on the transfer function model for investigating the output voltage under the effect of input voltage and load variations. For verification purpose, we compared our results with that obtained by the circuit model. Also we interested in analyzing the closed loop buck regulator. Therefore, we have designed the lag lead analog compensator with sign inverter [14] by performing a Matlab program to determine its element values (six resistors and two capacitors) that satisfy specific requirements (PM and e_{ss}). The pros and cons of the previously mentioned models are discussed in [15]. This paper is organized as follows: The analysis of analog lag lead compensator with sign inverter is discussed in section II. The digital compensator using bilinear z-transform method is included in section-III. Simulation results are demonstrated in section IV. Concluding remarks and future work are summarized in section V.

Table-1: Summary of buck converter transfer functions

Non-ideal case

$$Q=\frac{\sqrt{LC}}{(r_L+r_C)C+(L/R)},\quad \omega_o=(1/\sqrt{LC}),\quad \frac{r_L}{R}<<1,\quad \frac{r_C}{R}<<1$$

$$\Delta(s)=1+(s/Q\omega_o)+(s/\omega_o)^2$$

$G_{\upsilon_o d}(s)=\frac{\upsilon_o}{d}\approx\frac{V_g(1+sr_CC)}{\Delta(s)}$	$G_{\upsilon_o\upsilon_g}(s)=\frac{\upsilon_o}{\upsilon_g}\approx\frac{D(1+sr_CC)}{\Delta(s)}$
$Z_{out}(s)=\frac{\upsilon_o}{i_o}\approx\frac{r_L(1+(sL/r_L))(1+sr_CC)}{\Delta(s)}$	$G_{i_g d}(s)=\frac{i_g}{d}\approx\frac{(V_g/R)(1+sRC)}{\Delta(s)}$
$G_{i_g i_o}(s)=\frac{i_g}{i_o}\approx\frac{(1+sr_CC)}{\Delta(s)}$	$G_{i_g\upsilon_g}(s)=\frac{i_g}{\upsilon_g}\approx\frac{(D/R)(1+sRC)}{\Delta(s)}$

II. ANALOG LAG LEAD COMPENSATOR WITH SIGN INVERTER

The closed loop of switched mode power supply buck regulator based pulse width modulator, buck converter and compensator is shown below:

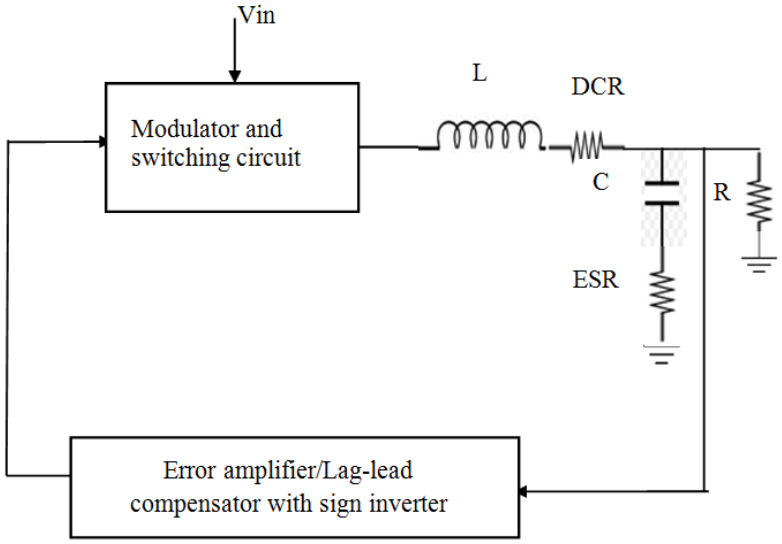

Fig. 1 shows the functional block of the closed loop buck regulator.

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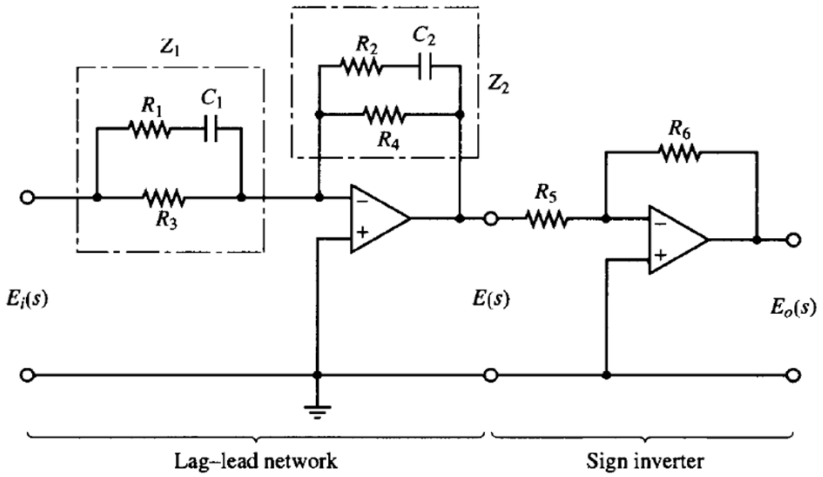

Fig. 2 shows the Lag lead compensator with sign inverter having six resistors and two capacitors

The open loop transfer function of the power converter (output filter and modulator) in Fig, 1 can be expressed as:

$$G_{\upsilon\upsilon_g}(s)=\frac{1+sr_C\,C}{s^2L\,C\left(1+\frac{r_C}{R}\right)+s\left(C\left(r_C+r_L\right)+\frac{L}{R}+C\frac{r_L\cdot r_C}{R}\right)+\left(1+\frac{r_L}{R}\right)}\frac{V_{in}}{V_{ramp}}, \tag{1}$$

where r_C : is the equivalent series resistance (ESR) of the output capacitor, and r_L : DC resistance (DCR) of the inductor , *R:* is the load resistor, V_{in} : is the input voltage and V_{ramp} is the peak to peak voltage of ramp signal. The transfer function of the lag-lead compensator with sign inverter in Fig. 2can be written as:

$$\frac{E_o(s)}{E_i(s)}=\frac{R_4R_6}{R_3R_5}\left[\frac{(R_1+R_3)C_1s+1}{R_1C_1s+1}\right]\cdot\left[\frac{R_2C_2s+1}{(R_1+R_4)C_2s+1}\right]=\frac{kc}{\alpha_g\,\alpha_d}\left(\frac{s+\mathrm{zcd}}{s+\mathrm{pcd}}\right)\cdot\left(\frac{s+zcg}{s+pcg}\right), \tag{2a}$$

$$\text{where } \alpha_g=\frac{zcg}{pcg}>1,\ \alpha_d=\frac{zcd}{pcd}<1,\ \ pcd=\frac{1}{\mathrm{c}_1R_1},\ zcd=\frac{1}{\mathrm{c}_1(R_1+R_3)},\ zcg=\frac{1}{\mathrm{c}_2R_2},$$

$$pcg=\frac{1}{\mathrm{c}_2(R_2+R_4)}\ \text{and}\ \ \mathrm{kc}=\frac{R_4R_6}{R_3R_5}. \tag{2b}$$

The steps applied to the design can be disseminated as follows:

1) Given the desired phase margin (ϕ_m) at a specific crossover frequency f_{cross} and the steady state error e_{ss} .
2) Compute the magnitude G_p and phase ϕ_p of the buck power converter using Bode function at f_{cross} .
3) Solving the two coupled nonlinear equations related to the magnitude and phase of each one of the lag and lead parts to determine their poles and zeros satisfying the following conditions:

   (a) Magnitude of the lag part at f_{cross} is equal to 0.99 and its phase, ϕ_c $\left(-0.05^o<\phi_c<0\right)$.

   (b) Multiplication of the lead part and buck converter magnitudes including the constant kc calculated by the given steady state error value at f_{cross} is equal to 1. Also the phase of the lead part is the boost required to be added for achieving desired phase margin PM.

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Table-2: Lag-lead compensator elements corresponding to the desired phase margin PM, and steady state error values e_{ss} at specific crossover frequency f_c for the DC/DC buck Regulator.

Crossover frequency f_c[kHz]	Phase Margin PM [deg]	Steady state Error e_{ss}	V_{out} [V]	R_b [kΩ]	R_1 [kΩ]	R_2 [kΩ]	R_3 [kΩ]	R_4 [kΩ]	R_5 [kΩ]	R_6 [kΩ]	C_1 [nF]	C_2 [μF]
5	60	0.022	8	0.6	1.16	1.28	6.45	32.8		2		
7	70	0.025	10	1.1	1.24	9.73	14.7	29.8		4.9		
9	80	0.018	12	2.1	0.93	9	33.4	78.9	10	4.2	10	20
	95			1.9	0.40	9	30.6	78.8		3.9		
10	85	0.015	15	0.7	0.63	7	14.5	27.8		5.2		
11	90	0.02	18	0.9	0.56	6.5	22.7	27.3		8.3		
Power converter specifications		C=650 μF, L = 50 μH, ESR=0.01 Ω, DCR = 0.005 Ω, V_{in} = 20V, R=5 Ω, $V_{ref} = 0.696V$ and $V_{ramp} = 1V$.										

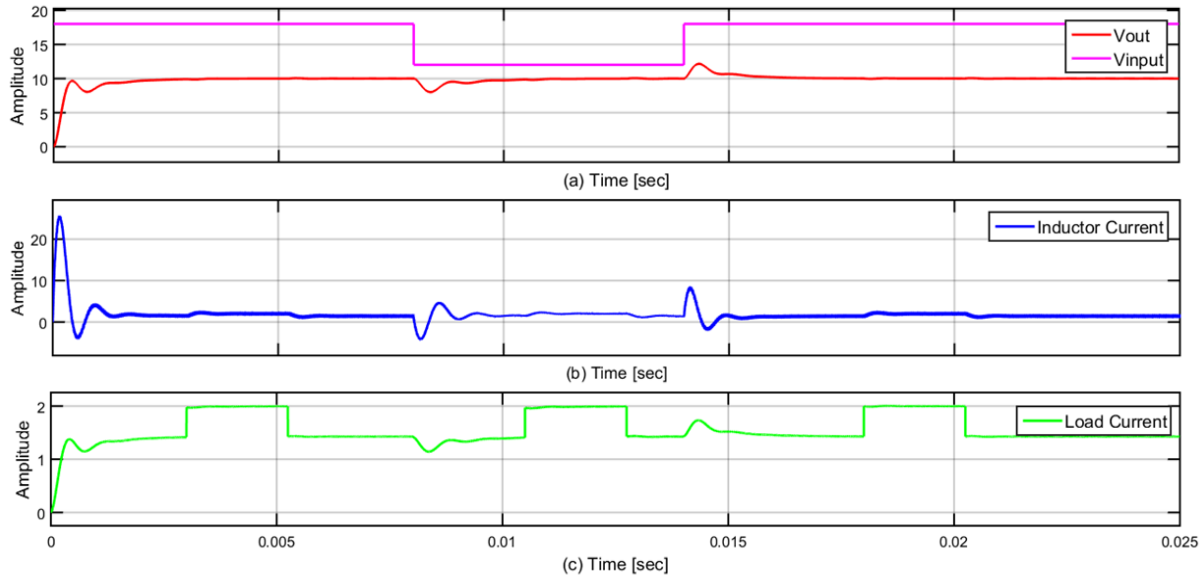

Fig.3 depicts the following waveforms related to input voltage change from 18 to 12V at time 0.008 sec. and from 12 to 18 V at 0.014 sec. The variation of load current is shown with load resistor change from R = 7 Ω to 5 Ω due to control periodic pulses, having period 0.0075 sec and duty cycle 0.3, starts at 0.003 sec. This results in a load current change from 1.43 A to 2 A and vice versa. (a) Input and output voltages. b) Inductor current. c) Load current

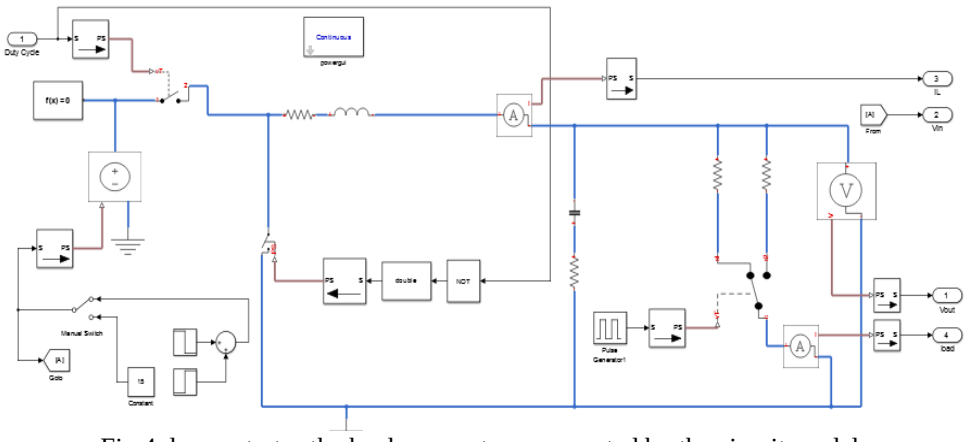

Fig.4 demonstrates the buck converter represented by the circuit model

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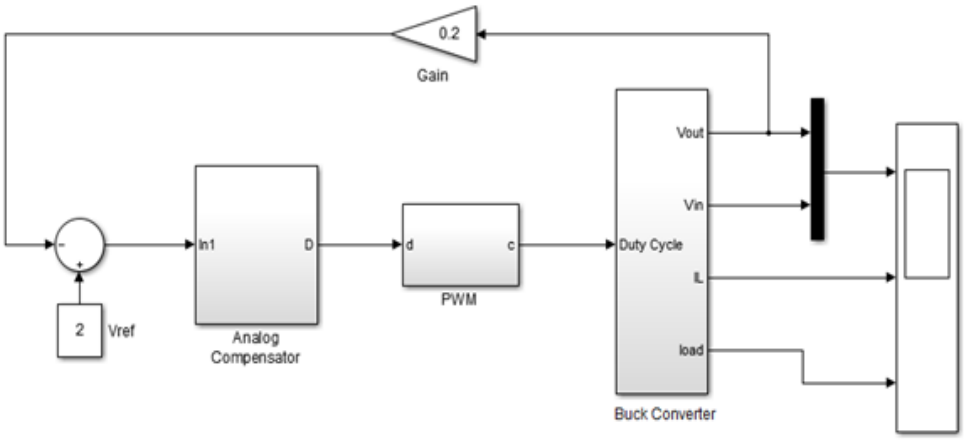

Fig.5 depicts the functional diagram of analog buck regulator using
lag lead compensator with sign inverter, pulsewidth modulator (PWM) and buck power converter.

In voltage mode control, applied in this work, an external signal [6-8,[11] is compared with the feedback control signal for generating the duty cycle to have the required output voltage as shown in Fig.5. This is clarified by subtracting reference voltage V_{ref} from the sensed output voltage and the resulted error signal is sent to the compensator unit. Then, a compensator output voltage V_c is compared with the ramp signal giving a pulsating signal with appropriate duty cycle. Consequently it feeds the drivers and switching circuit in such a way to minimize the output error.

III. DIGITAL COMPENSATOR

Based on the bilinear z-transform given in Eq.3a and the converter parameters given in table-2, the s-domain transfer

$$s = \frac{2}{T_s}\frac{(z-1)}{(z+1)} \qquad (3a)$$

function of the designed analog compensator and its z-domain transformed one satisfying $\mathrm{PM} = 80$ deg. and steady state error with step input e_{ss} = 0.015 at crossover frequency $f_{cross} = 6$ kHz and sampling frequency $f_s = 175$ kHz can be written as:

$$HC(s) = \frac{5.63\times10^{-7}s^2 + 0.00518s + 4.382}{4.205\times10^{-8}s^2 + 0.00724s + 1}, \quad (3b) \qquad HD(z) = \frac{9.207z^2 - 17.94z + 8.735}{z^2 - 1.34z + 0.3405} \quad (3c)$$

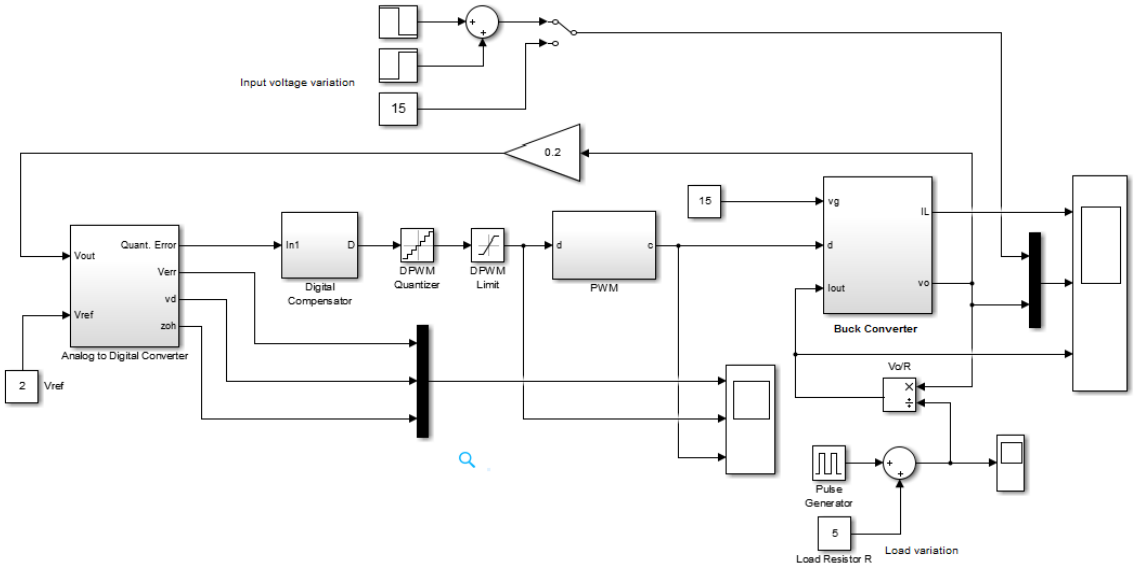

Fig.6 shows the functional block diagram of digital buck regulator including the effect of the load and input voltage variations. Also the buck converter is realized by the transfer function model.

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The parts of the system that model the digital controller [17-22] include: A/D converter, discrete time compensator, and digital PWM. Also by using the direct form II realization method to reduce the number of delays, As a result, the hardware description of our compensator can be implemented as following:

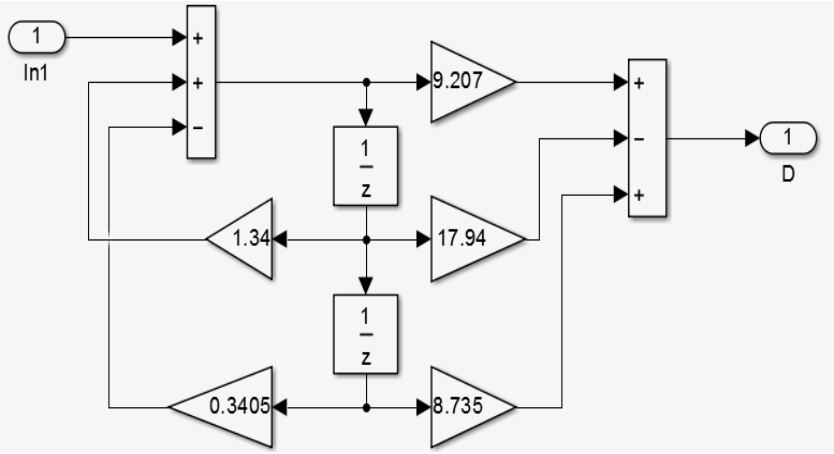

Fig.7 shows the realized digital compensator using direct form II method

IV. SIMULATION RESULTS

Table-1 included the transfer functions of DC-DC buck converter for non-ideal case using state space averaging method. This enables the circuitry, mathematical, and transfer function models to be to be simulated. Figures 1,2 show the functional diagram of buck regulator and circuit diagram of lag lead compensator with sign inverter respectively. The analog compensator elements are evaluated and clarified in table-2 which are obtained using a Matlab program performed to satisfy specific phase margin and steady state error values. These results related to given specifications of driving circuit, modulator and buck converter. The simulated response of the output voltage due to level change in input voltage and load is depicted in Fig.3. This is noticed at 0.008 sec for a step down change from 18 V to 12 V and a step up change from 12V to 18 V at time 0.014 sec. Also we demonstrated the change of load current and inductor current due to the load variations from (7 to 5) Ω and from (5 to 7) Ω, with period 0.0075 sec. and having duty cycle 0.3. It is obvious from the obtained results that the output regulated voltage keeps its value and settled after the small overshot time which indicates robustness of the designed buck regulator. Fig.4 demonstrates the circuit model for the buck converter which incorporated with buck regulator in Fig. 5 to emphasize the complete overview and high performance. Fig. 6 illustrates the functional diagram of closed loop digital regulator comprised of A/D, discrete time compensator and DPWM. Fig.7 depicts the realization of digital compensator using direct form II method.

V. CONCLUDING REMARKS

In summary, this paper covers the following: a) design of analog and digital buck regulator to satisfy desired requirements such as phase margin and steady state error at different crossover frequencies. b) applying the transfer functions derived by small signal model based state space representation to study the load and input variations in case of losses ($DCR \neq 0$ and $ESR \neq 0$). We apply the transfer function model, not preferred by the researchers, to our simulation. This is attributed to the parameter values like load resistor and input voltage are embedded inside the transfer functions (TFs) required to be implemented. To cope with this difficulty, a Matlab program has been accomplished to obtain explicit expressions for the intended transfer function in s-domain. Then, these TFs are incorporated in Simulink using the switching approach at the subsystem output under investigation. Such work will help students to acquire a comprehensive view of modeling, simulation and computational implementation of SMPS regulators at the scale of circuit analysis, control theory, differential equations, and digital signal processing. In addition, we addressed the circuit model to compare the results with that obtained by transfer function model. The equivalent digital compensator has been implemented with the closed loop buck regulator to benefit from its advantages like flexibility, cost, programmability, accuracy, size miniaturization, speed. A good agreement between the results obtained by the analog and digital buck regulators regards to the transient performance (overshoot, settling time, rise time, ripples). The notable difference between them is the phase margin erosion for the digital one which can be divided into two parts. The first part caused by the sampling and reconstruction processes while the second part originated from the computational delay. This will be covered associated with the hardware implementation of these regulators as a future work.

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REFERENCES

[1]. Tymerski R, Vorperian V. Generation, classification and analysis of switched-mode DC-DC converters by the use of converter cells. Telecommunications Energy Conference. 1986. p. 181-195.
[2]. Chen J, Ngo K.D.T. Alternate forms of the PWM switch model in discontinuous conduction mode. IEEE Trans. Aerosp. Electron. Syst. 2001.p. 754-758.
[3]. Sun J, Mitchell DM, Greuel MF, Krein PT, Bass RM. Average modeling of PWM converters in discontinuous modes. IEEE Trans. Power Electron.2001.p.482–492.
[4]. J.H. Su, J.J. Chen, and D. S. Wu, "Learning feedback controller design of switching converters via MATLAB/SIMULINK," IEEE Transactions on Education, vol. 45, pp. 307-315, 2002.
[5]. Assaf, D. Seshsachalam, D. Chandra, and R. Tripathi, "DC-DC converters via MATLAB/Simulink," in the Proc of WSEAS Conference on Automatic Control, Modelling and Simulation (ACMOS'05), Prague, Czech Republic, pp. 464-471, 2005.
[6]. A. Emadi, "Modelling and analysis of multi-converter DC power electronic systems using the generalized state space averaging method," in Industrial Electronics Society, 2001. IECON'01.The 27th Annual Conference of the IEEE, pp. 1001-1007, 2001.
[7]. J. Mahdavi, A. Emaadi, M. Bellar, and M. Ehsani, "Analysis of power electronic converters using the generalized state-space averaging approach," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 44, no. 8, pp. 767-770, Aug. 1997.
[8]. A. Kislovski, R. Redl, and N. Sokal, "Dynamic Analysis of Switching-Mode DC/DC Converters", New York: Van Nostrand Reinhold, 1994.
[9]. B. Choi, "Pulsewidth Modulated DC-to-DC Power Conversion: Circuits, Dynamics, and Control Designs," Hoboken, New Jersey: John Wiley & Sons, Inc., 2013.
[10]. M. K. Kazimierczuk, N. Sathappan, and D. Czarkowski, "Voltage-mode controlled PWM buck dc-dc converters," Proc. of the IEEE National Aerospace Conf. (NAECON'93), Dayton, OH, May 24-28, 1993, vol. 1, pp. 1253-1256.
[11]. M. K. Kazimierczuk and R. Cravens, II, and A. Reatti, "Closed-loop input impedance of the PWM buck-derived dc-dc converters", IEEE International Conference on Circuits and Systems, London, U.K., May 30-June 2, 1994, vol. 6 pp. 61-64.
[12]. A.J. Forsyth, S.V. Mollov, " Modeling and Control of DC-DC Converters" IEE Power Engin-eering Journal, vol. 12, no. 5, pp. 229–236, October 1998.
[13]. Monamed. A. Shrud, Ahmad Kharaz, Ahmed. S. Ashur, Mustafa Shater, Ismail Benyoussef, "A Study of Modeling and Simulation for Interleaved Boost Converter", Power Electronic & Drive Systems & Technologies Conference (PEDSTC), 2010, pp. 28-35.
[14]. Katasuhiko Ogata, 'Discrete-Time Control Systems', Prentice Hall,2ndEd.,New Jersey, 1994.
[15]. Rodney H.G TanI, Matthew Y. W. Teow," A Comprehensive Modeling, Simulation and Computational Implementation of Buck Converter Using MATLAB/Simulink" ,Energy Conversion(CENCON)",2014 IEEE Conference on 13-14 Oct.2014, pp. 37-42.
[16]. A.W.N. Husna, S.F. Siraj, M.Z. Ab Muin, "Modeling of DC-DC Converter for Solar Energy System Applications", IEEE Symposium on Computers & Informatics (ISCI), 2012, pp. 125-129.
[17]. S. Laali, H.M Mahery, "Buck DC-DC Converter: Mathematical Modeling and Transient State Analyzes", 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2012, pp. 661-667.
[18]. Dragan Maksimovic, Regan Zane, s.a, "Impact of Digital Control in Power Electronics", Power Semicond-uctor Devices and ICs, 2004, pp. 13-22.
[19]. Yan-Fei Liu, Eric Meyer and Xiaodong Liu, "Recent Developments in Digital Control Strategies for DC/DC Switching Power Converters", IEEE Transactions on Power Electronics, vol. 24, no. 11, nov. 2009, pp. 2567-2577.
[20]. Daniel W Hart, 'Power Electronics', McGraw-Hill Companies, 2011.
[21]. MATLAB SimElectronics Toolbox Release 2014a, The MathWorks, Inc., Natick, Massachusetts, United States, March 2014.
[22]. Asadi F, Eguchi K. Dynamics and control of DC-DC converters, San Rafael: Morgan and Claypool; 2018. p. 89-145.

BIOGRAPHY

Mohamed A. A. Abdel-Rahman was born in Mansoura, Egypt, on February, 1955. He received the Bachelor of Science degree in electrical engineering from the Military Technical College, Cairo, Egypt in 1979 and the Master of Science degree from the Faculty of Engineering, University of Alexandria, Alexandria, Egypt in 1990. He received his Ph. D. degree from Virginia Polytechnic Institute and State University, USA in 1997. He is working at Alexandria Higher Institute of Engineering and Technology (AIET), Alexandria, Egypt since 2008 until now as an Assistant Professor. He is presently on a sabbatical leave at Faculty of Engineering of Al-Baha University, Saudi Arabia Kingdom. His research and teaching interest areas include radar signal processing, digital power electronics, target tracking and phased array antennas.