

# Impact of Temperature on Electrical Characteristics of Ballistic Carbon Nanotube Field Effect Transistor for Different Dielectrics

Md Faysal Nayan

Department of EEE, Ahsanullah University of Science and Technology, Dhaka, Bangladesh

**Abstract:** Carbon Nanotube Based Field Effect Transistors (CNTFET) are being extensively studied as a counterpart device of silicon compatible CMOS. This paper presents a numerical simulation model of semiconducting carbon nanotube based field effect transistor to derive the electrical characteristics under ballistic regime. This technique is considered the approximation of non-equilibrium mobile charge density to get the fast and efficient modelling of drain current. The influence of gate dielectric constant and temperature on the performance of a carbon nanotube field-effect transistor has been studied by a numerical simulation model. Moreover, the impact of temperature has been portrayed for different gate voltage to observe the performance of the transistor.

**Keywords:** Chiral Indices; Ballistic; Temperature; Dielectric constant; Density of states; Fermi level

## I. INTRODUCTION

The world has already witnessed the advancement of electronics in terms of automation, computing, communication etc. However, advancement of electronics based on silicon device have faced problem due to scaling of transistor on a device [1],[2]. According to Moore's law, the number of transistor on a chip doubles every two years because of reduced dimension of transistor. Moreover, due to short channel, nanodevice has faced problem associated with fabrication and performance of the device [3],[4]. So that researcher has inspired to developed alternative technology for electronics. Carbon nanotube is a promising option to fabricate carbon nanotube field effect transistor due to its superior electrical and optical properties [1],[5],[6]. However, the intensive research based on the carbon nanotube field effect transistor has showed excellent opportunity to understand the ballistic transport and performance of the device. In large scale integration ballistic CNTFET shorter than mean free path of the acoustic phonon are the attractive option for semiconducting nanodevices [7]. In addition, The research are carried out to optimize the device performance regarding the ON/Off ratio [8]. Thermoionic emission and tunnelling could be the barrier to achieve high ON current depending on the temperature of the device environment [9]. Due to high carrier mobility and ballistic transport, CNTFET can provide high drain current, high speed switching, low power consumption. Compared to MOS field effect transistor CNTFET have showed outstanding opportunity in the research filed [3],[10]. Hence extensive research has to carried out to realize the potential of CNT on a nanoscale device [1],[2].

## II. PROPERTIES OF CARBON NANOTUBE

Carbon Nano Tubes (CNT) are allotropes of carbon and belong to the same family of graphene and fullerene. They exhibit a tubular or cylindrical geometry which composed of a single, rolled up graphene sheet. In graphene carbon atoms are arranged in a hexagonal lattice that forms a honeycomb structure [2], [11],[12]. If the lattice vectors of graphene sheet is  $a_1$  and  $a_2$  in real space, chiral vector is mathematically represented by the following equation [2].

$$C_h = na_1 + ma_2 \quad (1)$$

Where, n and m are called chiral indices &  $0 \leq m \leq n$ . The value of n & m can be used to determine both chiral angle and tube diameter. The diameter d of a carbon nanotube can be derived from the equation of chiral vector [11], [13].

$$d_t = \frac{a\sqrt{n^2+2mn+m^2}}{\pi} \quad (2)$$

The chiral angle is the angle between  $C_h$  and  $a_1$  represented in terms of chiral indices as

$$\cos \theta = \frac{2n+m}{a\sqrt{n^2+2mn+m^2}} \quad (3)$$

Using the concept of chiral vector, carbon nanotube can be classified as armchair (n, n) with a chiral angle of  $\theta = 30^\circ$ , zigzag (n, 0) with  $\theta = 0^\circ$  and chiral(n, m) types with  $0^\circ \leq \theta \leq 30^\circ$ . The condition of chiral angle is  $0^\circ \leq \theta \leq 30^\circ$  and the chiral index  $0 \leq m \leq n$  is due to rotational symmetry of graphene sheets [13].

The electrical behaviour of carbon nanotube can be classified as semiconducting or metallic depending on chiral vector. The nanotube is metallic if the difference of the vector integers n & m is a multiple of three which means that  $(n - m) = 3p$ ;  $p \in \mathbb{Z}$ . Otherwise it is semiconducting [2],[5]. In the density state diagram, the peaks are attributed to nature of band structure of single walled carbon nanotube & called as van Hove singularities & represents the energy levels of electron. The transition energy defined by the distance between van Hove singularities also known as bandgap [2],[11]. The equation of transition energy [14],

$$E_{ii} = \frac{j a_{cc} \gamma_0}{d_t} \tag{4}$$

Where,  $a_{cc}$  = nearest neighbor carbon-carbon distance,  $\gamma_0$  = interaction energy between carbon atoms and  $d_t$  represents the carbon nanotube diameter.

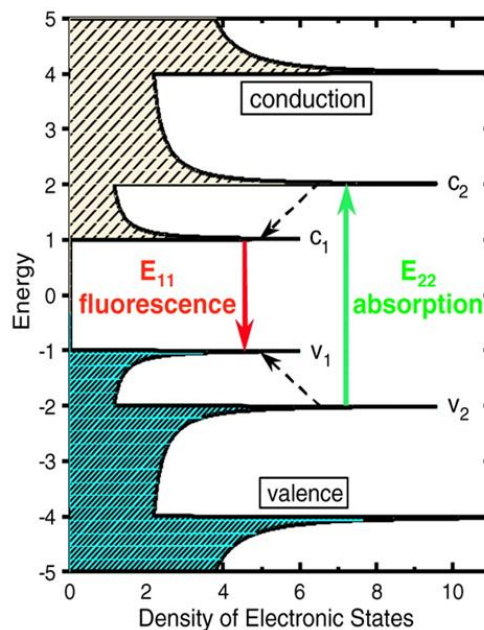


Fig. 1: Schematic density of electronic states for a single nanotube structure

### III. MATHEMATICAL MODEL FOR BALLISTIC CNTFET

The analytical model for investigation of electrical characteristics of carbon nanotube based field effect transistor consider the 2D model of ballistic transport of charge carriers in MOSFET [15],[16]. The schematic diagram of the model consists of three capacitors, which represent the effect of the three terminals on the potential at the top of the barrier. Furthermore, non-equilibrium mobile charge can be determined from the concept of local density of states of the top of the barrier, position of Fermi level of source and drain and self-consistent potential at the top of the barrier. The position of Fermi level of source and drain indicated as  $E_{F1}$  and  $E_{F2}$  respectively [15].

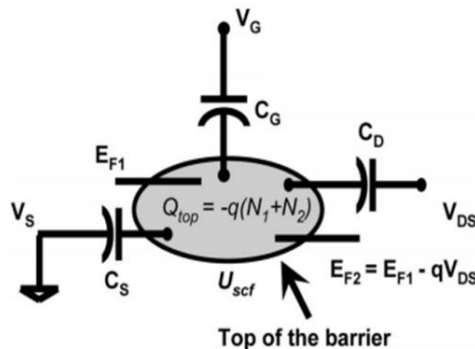


Fig 2: Two dimensional circuit model for ballistic CNTFET

The mathematical model of carbon nanotube field effect transistor considers the efficient calculation of mobile charge to determine the drain to source current. In this paper MATLAB based simulation is performed to under the ballistic transport in the transistor. To calculate the I-V characteristics of CNTFET , poisson equation is used to find carrier population in carbon nanotube. Charge density of carbon nanotube increased above a threshold voltage [17].

The calculation of current voltage characteristics starts with determination of mobile charge. Non equilibrium mobile charge is induced in the nanotube by applying the proper electric filed between source and drain terminal. If we apply  $V_{DS} > 0$  , then the equation of non-equilibrium charge density is [15] ,[16].

$$\Delta Q = q(N_S + N_D - N_0) \quad (5)$$

Where  $N_S$  is the density of positive velocity states filled by the source,  $N_D$  is the density of negative velocity states filled by the drain and  $N_0$  is the equilibrium electron density at the top of the barrier. The following equations of these densities can be determined using the concept of Fermi-Dirac probability function [15] ,[16].

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F) dE \quad (6)$$

$$N_S = \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f_1(E) \quad (7)$$

$$N_D = \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f_2(E) \quad (8)$$

Where,

$$f_1(E) = f(E - E_{F1} + U_{scf})$$

and

$$f_2(E) = f(E - E_{F2} + U_{scf})$$

Here,  $E_{F1} = E_F$  ,  $E_{F2} = E_F - qV_{DS}$

$$N_S = \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f(E - E_F + U_{scf}) \quad (9)$$

$$N_D = \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f(E - E_F + qV_{DS} + U_{scf}) \quad (10)$$

$E_F$  represents the Fermi level and  $f(E - E_F)$  is the equilibrium fermi function and E considers as the energy levels of nanotube per unit length.

$D(E)$  represent the density states of the carbon nanotube channel [16].

$$D(E) = D_0 \frac{E}{\sqrt{E^2 - (\frac{E_g}{2})^2}} y\left(E - \frac{E_g}{2}\right) \quad (11)$$

Where,  $D_0 = \frac{8}{3\pi v_{cc} a_{cc}}$  is the constant density of states of tube,  $E_g$  is the band gap.

$U_{scf}$  is self-consistent potential at the top of the barrier [15] ,[16].

$$U_{scf} = U_L + U_P \quad (12)$$

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \quad (13)$$

$$U_P = \frac{q^2}{C_{sum}} \Delta N \quad (14)$$

Where,  $U_L$  represents the Laplace potential at the top of the barrier due to terminal biases and  $U_P$  is potential due to the mobile charge, at the top of the barrier.  $\alpha_G$ ,  $\alpha_D$ ,  $\alpha_S$  are control parameter for gate, drain and source respectively.  $C_{sum}$  represents the total terminal capacitance. The equation of  $\Delta N$  defined as,  $\Delta N = (N_S + N_D - N_0)$ .

The following algebraic equation define the self-consistent voltage  $V_{SC}$  which depends on the device terminal voltages and charges at terminal capacitances [16],[18], [19].

$$V_{SC} = -\frac{-Q_t + qN_S + qN_D + qN_0}{C_{sum}} \quad (15)$$

$$Q_t = V_G C_G + V_D C_D + V_S C_S \quad (16)$$

Where  $C_G$ ,  $C_D$ ,  $C_S$  are the gate, drain, and source capacitances correspondingly and the total terminal capacitance  $C_{Sum}$  represent as the sum of all capacitances.

$$C_{Sum} = C_G + C_D + C_S \quad (17)$$

The equation of control parameter of Laplace potential are given by [15],

$$\alpha_G = \frac{C_G}{C_{Sum}} \quad \alpha_D = \frac{C_D}{C_{Sum}} \quad \alpha_S = \frac{C_S}{C_{Sum}} \quad (18)$$

The equation of gate oxide layer is defined as [16],

$$C_{ox} = \frac{2\pi\epsilon_1\epsilon_0}{\ln\left(\frac{2t_{ox} + d_t}{d_t}\right)} \quad (19)$$

where  $d$  is the diameter of the carbon nanotube,  $t_{ox}$  is the thickness of the gate insulator and  $\epsilon_1$  is the relative permittivity of the gate.

Furthermore, capacitance between terminals are defined as [16],

$$C_G = C_{ox} \quad (20)$$

$$C_S = 0.097C_{ox} \quad (21)$$

$$C_D = 0.040C_{ox} \quad (22)$$

So final equation of self-consistent potential is

$$U_{scf} = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + U_C \Delta N \quad (23)$$

Where, Charging density,  $U_C = \frac{q^2}{C_{sum}}$

According to ballistic theory of carbon nanotube, the drain current developed by the non-equilibrium mobile charge can be calculated using the Fermi Dirac statistics.

$$I_{DS} = I_0 \left[ F_0 \left( \frac{U_{SF}}{kT} \right) - F_0 \left( \frac{U_{DF}}{kT} \right) \right] \quad (24)$$

where  $F_0$  represents the Fermi-Dirac integral of order 0 and the current  $I_0$  is expressed as

$$I_0 = \frac{2qkT}{\pi\hbar}$$

where  $k$  is Boltzmann's constant,  $T$  is the temperature and  $\hbar$  is reduced Planck's constant.

A closed-form approximation of the Fermi-Dirac integral can be used to avoid numerical integration [19],

$$F_0(x) = \log\left(1 + e^x\right) \quad (25)$$

So the final form of drain to source current induced by carbon nanotube is [18]

$$I_{DS} = \frac{2qkT}{\pi\hbar} \left[ \log\left(1 + e^{\left(\frac{U_{SF}}{kT}\right)}\right) - \log\left(1 + e^{\left(\frac{U_{DF}}{kT}\right)}\right) \right] \quad (26)$$

#### IV. RESULT AND DISCUSSION

The numerical simulation model of Carbon Nanotube Field Effect Transistor (CNTFET) considered the (13,0) zigzag CNT. The nanotube diameter and bandgap is calculated by the equation (2) and (4). The parameter gate oxide was used 1.5 nm in the simulation environment. Investigation of influence of the temperature on the electrical characteristics has been carried out with different dielectric constant of gate insulator. In this paper, temperature has been varied from 300

K to 600 K under different dielectric constant. In this studies, silicon Dioxide (3.9), Hafnium Silicate (11), Lanthanum oxide (30) is used as a gate dielectric to observe the performance of the CNTFET [20]. The ballistic transport of charge carriers of CNTFET is obtained from the equations discussed in the mathematical modeling part. In the ballistic modeling approach, the calculations are extremely fast [16]. In this study drain voltage are varies from 0 to 0.6 V and simultaneously measure the drain current for  $V_{GS}=0.4$  V, 0.5 V and 0.6 V.

Figure 4 describes the drain to source current characteristics at  $T=300$  K under different dielectric constant. Obviously the value of drain current should be higher for higher gate to source voltage for both condition. In this study gate to source is varied from 0.4 V to 0.6 V with a increment of 0.1 V. Generally, at low gate voltage drain current is very low compared to 0.4V. A specific threshold voltage is needed to make "ON" the device. Moreover, Fig. 4 gives an idea about the drain current behavior with respect to dielectric constant. In addition, high dielectric constant has an effect to improve the drain current for same temperature and voltage condition. So by increasing the dielectric constant  $I_{ON}/I_{OFF}$  should be increased. This phenomenon attributes to the superior control of gate voltage over the channel [3].

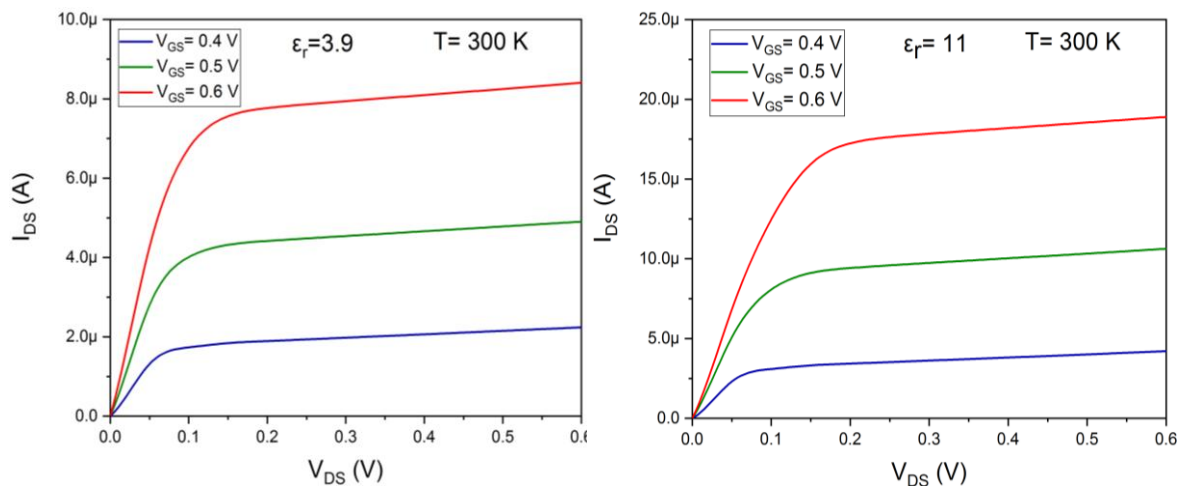


Figure 3: Electrical characteristics of CNFET at  $T=300$  K (a)  $\epsilon_r = 3.9$  (b)  $\epsilon_r = 11$

To understand the impact of temperature, it is necessary to analyse the Fig. 5,6 and 7. Figure 5,6,7 show the increasing pattern of drain with respect to temperature. With the dielectric constant,  $\epsilon_r = 3.9$ , the maximum saturation current for the device at  $T=300$  K is around  $2.2 \mu A$  for  $V_{GS}=0.4$  V, but for  $V_{GS}=0.6$  V the current goes to almost  $8.4 \mu A$ . On the other hand, from figure 6, With the dielectric constant,  $\epsilon_r = 11$ , the maximum saturation current for the device at  $T=300$  K is around  $4.2 \mu A$  for  $V_{GS}=0.4$  V, but for  $V_{GS}=0.6$  V the current goes to almost  $25.4 \mu A$ . Similar pattern is observed from figure 6, With the dielectric constant,  $\epsilon_r = 30$ , the maximum saturation current for the device at  $T=300$  K is around  $6 \mu A$  for  $V_{GS}=0.4$  V, but for  $V_{GS}=0.6$  V the current goes to almost  $27.5 \mu A$ .

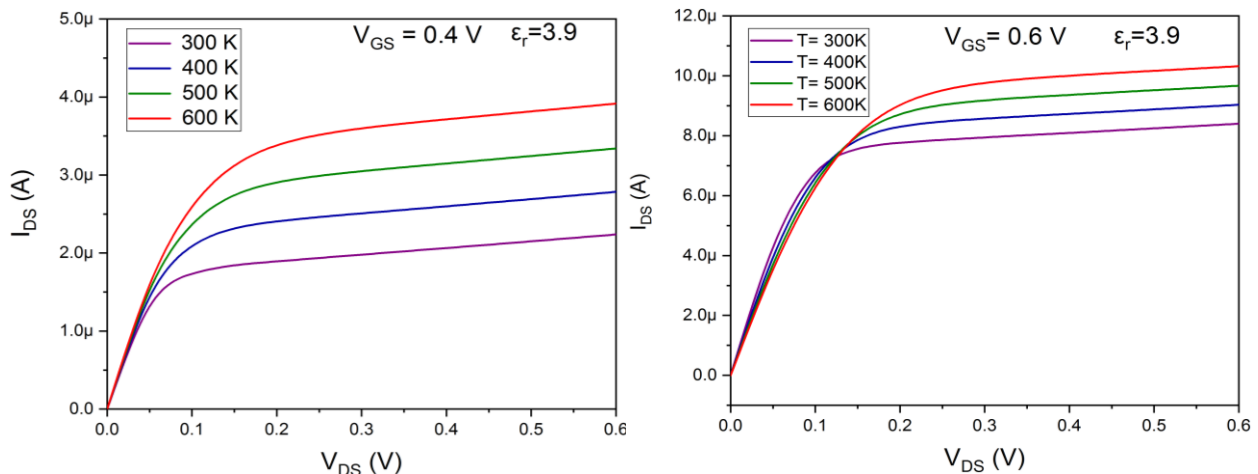


Fig. 4: Temperature dependent I-V characteristics with dielectric constant 3.9 (a)  $V_{GS}=0.4$  V (b)  $V_{GS}=0.6$  V

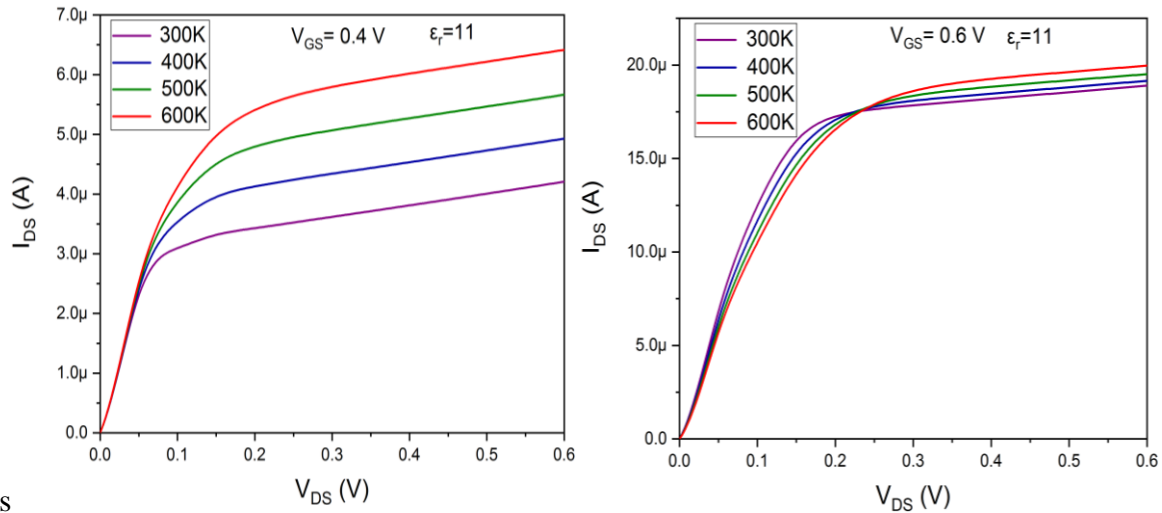


Fig. 5: Temperature dependent I-V characteristics with dielectric constant 11 (a)  $V_{GS} = 0.4$  V (b)  $V_{GS} = 0.6$  V

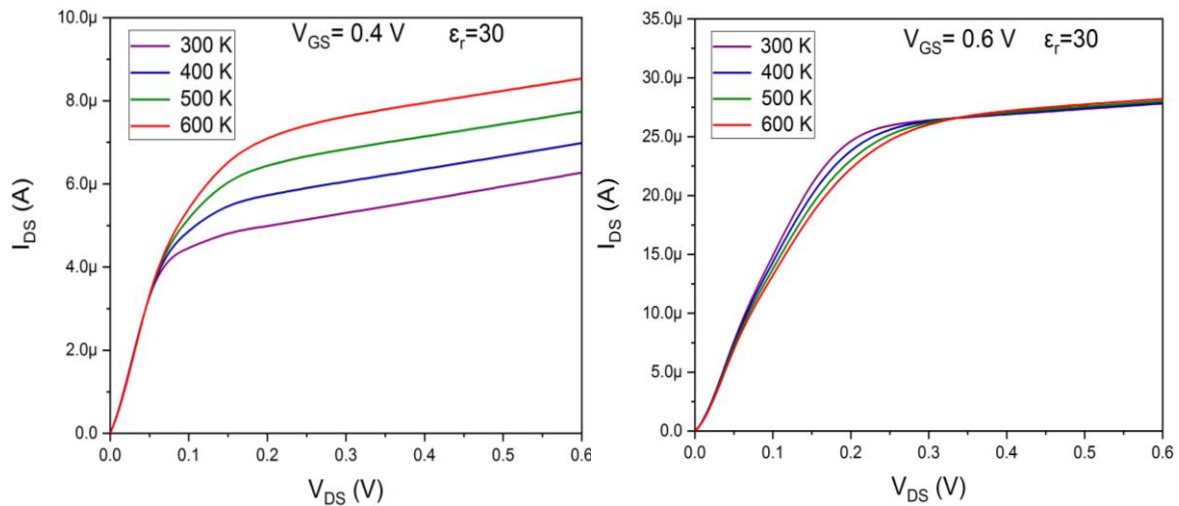


Fig. 6: Temperature dependent I-V characteristics with dielectric constant 30 (a)  $V_{GS} = 0.4$  V (b)  $V_{GS} = 0.6$  V

From the fig. 5,6 and 7, it can be seen that the drain current is increased due to the increasing behavior of the temperature. But for the value of  $V_{GS} = 0.4$  V, the increasing pattern is more prominent than the  $V_{GS} = 0.6$  V. So it is evident that, at higher gate voltage the drain current is weakly depend on the temperature. But at lower gate voltage, quantum tunnelling current has an effect on the temperature. The current increases with the temperature, but with different rates for different regions of operation [21], [22],[23],[24].

By analysing the fig. 6,7, and 8, it is observed that, temperature has also an impact for different dielectric constant. The drain current shows the proportionality behaviour with the dielectric constant. Higher dielectric constant lowers the energy for conduction and improved drain current. So high dielectric constant is an opportunity to increase the drain current of the CNTFET devices [3], [21],[25].

## V. CONCLUSION

This paper focuses on the impact of temperature on the electrical characteristics of CNTFET for different dielectric constant. The drain current is increases with increasing the gate dielectric constant. Furthermore, temperature have huge impact on the drain current characteristics in low gate voltage region, but it is weakly dependent on the drain current at high gate voltage region. So to get the optimized performance of the CNTFET it is necessary to fabricate the device with suitable dielectric constant and reasonable temperature environment.

**REFERENCES**

- [1]. P. Avouris, Z. Chen, and V. Perebeinos, "Carbon-based electronics," *Nat. Nanotechnol.*, vol. 2, pp. 605–615, 2007.
- [2]. A. P. and C. J., "Nanotube electronics and optoelectronics," *Mater. Today*, vol. 9, no. 10, pp. 46–54, 2006.
- [3]. R. Djamil, K. Aicha, A. Cherifa, and F. Djeflal, "Impacts of high-k gate dielectrics and low temperature on the performance of nanoscale CNTFETs," *J. Comput. Electron.*, vol. 15, no. 4, pp. 1308–1315, 2016.
- [4]. M. Shamim Sarker, M. Mainul Islam, M. Nur Kutubul Alam, and M. Rafiqul Islam, "Gate dielectric strength dependent performance of CNT MOSFET and CNT TFET: A tight binding study," *Results Phys.*, vol. 6, pp. 879–883, 2016.
- [5]. P. L. McEuen, M. S. Fuhrer, and Hongkun Park, "Single-walled carbon nanotube electronics," *IEEE Trans. Nanotechnol.*, vol. 1, no. 1, pp. 78–85, Mar. 2002.
- [6]. S. Tans, A. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature*, vol. 393, pp. 669–672, 1998.
- [7]. D. Akinwande, J. Liang, S. Chong, Y. Nishi, and H.-S. P. Wong, "Analytical ballistic theory of carbon nanotube transistors: Experimental validation, device physics, parameter extraction, and performance projection," *J. Appl. Phys.*, vol. 104, no. 12, p. 124514, Dec. 2008.
- [8]. A. Javey et al., "Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-k Gate Dielectrics," *Nano Lett.*, vol. 4, no. 3, pp. 447–450, Mar. 2004.
- [9]. A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic Carbon Nanotube Transistors," *Nature*, vol. 424, pp. 654–657, 2003.
- [10]. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 73, no. 17, pp. 2447–2449, 1998.
- [11]. J.-C. Charlier, X. Blase, & S. Roche, "Electronic & transport properties of nanotubes," *Rev. Mod. Phys.*, vol. 79, no. 2, pp. 677–732, May 2007.
- [12]. F. Molitor et al., "Electronic properties of graphene nanostructures," *J. Phys. Condens. Matter*, vol. 23, no. 24, p. 243201, Jun. 2011.
- [13]. A. B. Kaiser, "Conduction in Carbon Nanotube Networks," in *AIP Conference Proceedings*, 2003, vol. 685, pp. 160–163.
- [14]. S. M. Bachilo, "Structure-Assigned Optical Spectra of Single-Walled Carbon Nanotubes," *Science (80-. )*, vol. 298, no. 5602, pp. 2361–2366, Dec. 2002.
- [15]. A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1853–1864, 2003.
- [16]. T. J. Kazmierski, D. Zhou, B. M. Al-Hashimi, and P. Ashburn, "Numerically efficient modeling of CNT transistors with ballistic and nonballistic effects for circuit simulation," *IEEE Trans. Nanotechnol.*, vol. 9, no. 1, pp. 99–107, 2010.
- [17]. J. Guo, M. Lundstrom, and S. Datta, "Performance projections for ballistic carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 80, no. 17, pp. 3192–3194, 2002.
- [18]. T. J. Kazmierski, D. Zhou, and B. M. Al-Hashimi, "Efficient circuit-level modelling of ballistic CNT using piecewise non-linear approximation of mobile charge density," *Proc. -Design, Autom. Test Eur. DATE*, no. 1, pp. 146–151, 2008.
- [19]. T. J. Kazmierski, D. Zhou, and B. M. Al-Hashimi, "A fast, numerical circuit-level model of carbon nanotube transistor," *2007 IEEE Int. Symp. Nanoscale Archit. NANOARCH*, no. 2, pp. 33–37, 2008.
- [20]. J. Robertson, "High dielectric constant oxides," *Eur. Phys. JOURNALE*, vol. 28, pp. 265–291, 2004.
- [21]. S. C. N. Transistors, J. Guo, S. Member, S. Datta, and M. Lundstrom, "A Numerical Study of Scaling Issues for," vol. 51, no. 2, pp. 172–177, 2004.
- [22]. S. G. Shirazi and S. Mirzakhaki, "High on/off current ratio in ballistic CNTFETs based on tuning the gate insulator parameters for different ambient temperatures," *Appl. Phys. A Mater. Sci. Process.*, vol. 113, no. 2, pp. 447–457, 2013.
- [23]. A. Naderi, S. M. Noorbakhsh, and H. Elahipanah, "Temperature dependence of electrical characteristics of carbon nanotube field-effect transistors: A quantum simulation study," *J. Nanomater.*, vol. 2012, 2012.
- [24]. S. Gamal, M. El Sabbagh, and M. Ossamee, "Temperature dependence of carrier transport and electrical characteristics of Schottky-barrier carbon nanotube field effect transistors," *Micro Nano Lett.*, vol. 11, no. 2, pp. 114–117, 2016.
- [25]. A. Javey et al., "High-k dielectrics for advanced carbon-nanotube transistors and logic gates," *Nat. Mater.*, vol. 1, no. 4, pp. 241–246, 2002.