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Design of Power - Gated 8T SRAM Cell Design with Improved PDP

R.Sumithra[1], N.Vaijayanthi[2]

PG Scholar, Indra Ganesan College of Engineering, Trichy, Tamilnadu, India[1]

Professor, Department of ECE, Indra Ganesan College of Engineering, Trichy, Tamilnadu, India[2]

Abstract: The stability and power consumption of SRAM cell are the important factors in current technologies due to variability and voltage scaling. It has become a part of system-on-chip in modern VLSI designs. The existing SRAM cell designs are power hungry and have low performance for fast computing applications. In the proposed work a low power 8T SRAM cell is designed based on power gating mechanism. The Conventional 6T SRAM cell is very much prone to noise during read operation. To overcome the read SNM problem in 6T SRAM cell, configurations of 8T SRAM cells is proposed. 8T SRAM design also improves the cell stability but suffer from bitline leakage noise. Power gated VDD design technique have been employed to reduce the power consumed by the SRAM cell. The proposed design is compared with the conventional 6T SRAM cell. The results show that the gated based 8T SRAM cell is the best performer in terms of power consumption and power delay product. The power gated 8T SRAM cell consumes less power than the conventional 6T SRAM cell and also has a better power-delay-product.

Keywords: SRAM, Power Gating, PDP, SoC

I. INTRODUCTION

In modern system-on chips where SRAM is the main dominated part of the chip, the main problem is power consumed by the cell. As new devices are developed like smartwatches, small sensor nodes, wireless communication units, etc. energy efficient hardware architecture is required. Random Access Memory (RAM) chips are used virtually in every digital system and so energy efficient RAM architectures will have a positive impact on the overall system. Static Random Access Memory (SRAM) cells don't require constant refreshing to retain its contents as long as power is supplied to the cell. This major advantage of SRAM is the reason why it is preferred over Dynamic Random Access Memory (DRAM). SRAM's integration with standard CMOS technology gives it the opportunity to become the highest area consumer on System on Chips (SoCs). As the current technologies are scaling down to deep submicron levels, leakage power is becoming a major source of power consumption. Furthermore, majority of the transistors on a chip is in the SRAM unit. Since cache memory uses array architecture, power reduction in a single SRAM cell can contribute to huge power savings in the overall system. The conventional 6 Transistor (6T) SRAM cell is widely used primarily because of its simple design. The 6T SRAM cell is a good performer in terms of delay and power [1]. However, further analysis of the conventional 6T SRAM architecture shows a lot of room for improvement in terms of power consumption. Minimization in total power consumption can be achieved by reducing supply voltage VDD. Voltage scaling has some limitations such as degradation of static noise margin. Conventional 6T SRAM cell has a limitation of read disturbance during read operation. That results in poor read static noise margin. Many SRAM cell has been proposed to reduce power consumption as well as to improve read static noise margin. The basic idea to improve the read static noise margin is to totally disconnect the bit lines from the storing nodes [2].The standard 6T SRAM cell is not reliable to perform the operation at low voltage because of the voltage division between the access transistors and the pull-down transistors. There are also some constraints on the size of the access transistors and pull-up transistors which affects data stability and functions of the cell during read and write operations [3]. Furthermore, for improving the write margin and read stability of the conventional 6T SRAM cell, various read and write assist methods have been explored, such as virtual cell ground, adaptive cell-VDD, power gating and ground gating [4]. Extensive research has been performed on 6T SRAM cells to improve delay and power consumption so it can be adopted widely in industry. Even though [4] has analyzed various other SRAM architectures like 7T, 8T and a novel 9T design, the overall complexity of these circuits compared to the conventional 6T SRAM cell makes it more difficult to implement and ensure stable operation. Multi Threshold CMOS (MTCMOS) technique has been applied to a 7T SRAM cell achieving promising results in terms of power reduction [5]. In [6], a 10T SRAM cell is designed achieving high Static Noise Margin (SNM) and a 20.49% power reduction compared to the conventional 6T SRAM cell. The major drawback with this design is the increased area. When implementing this design in an array, due to the huge multiplying factor, the area of the overall memory chip increases considerably. [7] explores a 9T SRAM cell which includes Stacking and

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Dual Threshold voltage implementations to reduce leakage power. In [8], two SRAM cells are presented: one structure using NMOS pass transistors to reduce gate leakage current and the other structure using PMOS pass transistors. [9], [10], [11], and [12] present various power reduction techniques in CMOS circuits concluding MTCMOS as one of the best techniques to combat leakage power.

The rest of this paper is organized as follows: Section II briefly presents the 6T SRAM cell and its drawbacks. Section III presents the power gating logic. The proposed power gated 8T SRAM cell is explained in Section IV. The results are evaluated in Section V and Section VI concludes the paper.

II. CONVENTIONAL 6T SRAM DESIGN

The conventional 6T SRAM cell uses two cross coupled inverters and two access transistors as shown in Figure 1. The inverters are the storage element which holds the data bit within the cell as long as the power is supplied (VDD). P1, P2 are PMOS transistors and N1, N2, N3, N4 are NMOS transistors. N3 and N4 are the pass transistors connecting the cell to the Bit Lines (BL and BLB). The different modes of operation of the SRAM cell are as follows.

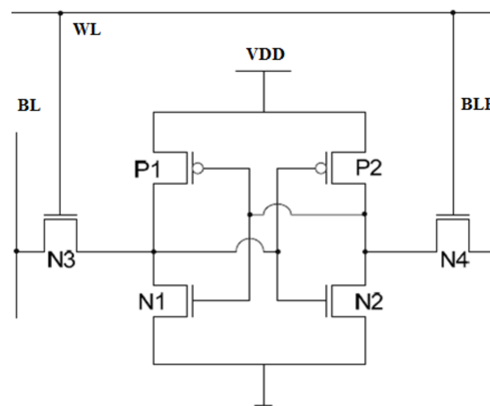

Fig.1. Conventional 6T SRAM cell

A. Standby/Hold Mode: When the Word Line (WL) is at logic ‘0’, the access transistors N3 and N4 disconnect the cell from the Bit Lines (BL and BLB). The two cross coupled inverters in the cell continue to hold the data bit present in the cell as long as power is supplied. The current flow in this mode from VDD is termed as standby current.

B. Write Mode: The cell ratio should be sufficiently high for a successful write operation to take place. Cell ratio is defined as the ratio of the strength (drive current) of the pass transistor (access transistor) to that of the pull up transistor. The value to be written into the cell is applied to the Bit Lines. Complementary Bit Lines are used, BL and BLB, on either side of the cell to ensure that the load to charge is reduced for each access transistor. This enables us to use smaller access transistors on each side rather than one single large access transistor. For a write operation, the Word Line (WL) is set to logic ‘1’ enabling the access transistors N3 and N4 thereby connecting the cell to the outside world (BL and BLB). The contents from the Bit Lines (BL and BLB) are then transferred.
However, the potential stability problem of this design arises during read and writes operation, where the cell is most vulnerable towards noise and thus the stability of the cell is affected. If the cell structure is not designed properly, it may change its state during read and write operation.

III. POWER GATING LOGIC

Power gating is the process to cut down supply when circuit is not in operation. Power Gating is an extremely effective scheme for reducing the leakage power of idle circuit blocks. The power (Vdd) to circuit blocks that are not in use is temporarily turned off to reduce the leakage power. When the circuit block is required for operation, power is supplied once again. During the temporary shutdown time, the circuit block is not operational it is in low power or inactive mode. Thus, the goal of power gating is to minimize leakage power by temporarily cutting-off power to selective blocks that are not active.

Power gating is implemented by a PMOS transistor as a top switch to shut off power supply to parts of a design in standby or sleep mode. NMOS bottom switches can also be used as sleep transistors. Inserting the sleep transistors splits the chips power network into two parts: a permanent power network connected to the power supply and a virtual

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power network that drives the cells and can be turned off. In addition, coarse-grain power gating results in a large switched capacitance, and the resulting rush current can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this. Finally, since power gates are made of active transistors, the leakage of the power gating transistor is an important consideration in maximizing power savings.

Principles of power gating design

Power gating consists of selectively powering down certain blocks in the chip while keeping other blocks powered up. Internal switches are used to control power to selected blocks. Fig.2 shows the block diagram of power gating architecture.

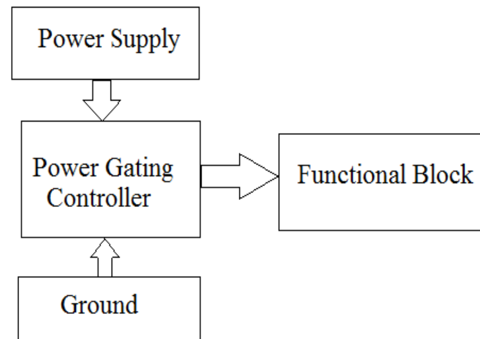

Fig.2. Power gating Architecture

Power switching network switches either VDD or VSS to the power gated block. One challenge for power gating design is that the output of power gated block may ramp off very slowly. The result could be that these outputs spend a significant amount of time at threshold voltage, causing large crowbar currents in the always powered. Isolation cells are designed so that when one of the inputs is at threshold, as long as the control input is off. Power gating controller provides this isolation control signal. For some power gated blocks, it is highly desirable to retain the internal state of the block during power down, and to restore this state during power up. Such retention strategy can save significant amount of time and power during power up. One way of implementing such retention strategy is to use retention register instead of normal flip -flops.

IV. PROPOSED 8T SRAM DESIGN

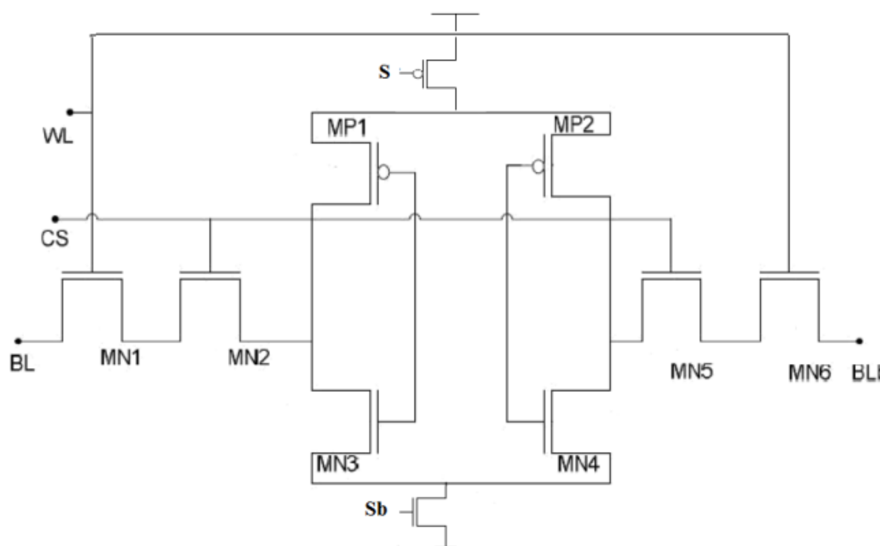

Fig.3. Proposed Power Gated 8T SRAM cell.

The architecture of new 8T SRAM cell is shown in Fig.3. It consists of two extra transistors MN2 and MN5 as compared to conventional 6T SRAM cell. Transistor MN2 is used to reduce gate leakage, while transistor MN5 is used to make cell SNM free in the zero state. Interestingly, transistor MN5 also helps in improving SNM when cell holds logic ‘1’. The sign WLB is the complement of wordline (WL) signal. In this work, the basic read/write operations of 8T SRAM cell are preformed using single ended sense amplifier.

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Write operation of 8T SRAM cell

In write '0' operation the bitline BT is pulled down to logic '0'. As soon as the signal WL rises from logic '0' to logic '1', transistor MNWL is turned OFF. The node starts discharging which turns ON transistor MP2 causing cell to flip and logic '0' is written into the cell. In write '1' operation, the bitline BL is pulled down to -Vt, where Vt is the threshold voltage of transistor MN4. The node XB starts discharging which turns ON transistor MP1. Once transistor MP1 is turned ON, the node is at logic '1' and hence logic '1' is written into the cell. In read operation, the bitlines BL and BLb are held at logic '1' by the precharged circuitry. In read '0' operation, the bitline BL starts discharging through transistors MN3 and MN1. Since the usage of SRAM cell is in cache memory, the single ended 8T SRAM circuitry is being used to store the required data. For generating a memory, there is a requirement of Address decoder, Data Write Circuitry and Data Read Operation. Since the proposed circuitry does not require precharge circuit, there is no elaboration of precharge circuitry as in 6T SRAM Cell. The selection of word-line represents the selection of a particular row.

Read operation of 8T SRAM cell

Read operation of 8T SRAM is initiated by pre-charging the read bitline to full swing voltage. After pre-charging read bitline, RWL is asserted that drives access transistor MN5 ON. If Q=0, then MN6 is ON & RBL discharges through transistors MN5 & MN6 to ground. This decrease in the voltage of RBL is sensed by the sense amplifier. During read "1" operation, when Q=1, MN6 remains OFF, so there will be no discharge current flow through the read path. In this situation, only a very small amount of leakage current flows, which is called bitline leakage. Write operation of 8T cell is similar to 6T cell, but the pre-charge circuitry at the bitlines is replaced by write driver.

V. EVALUATION RESULT

Table. I Comparison Result of 6T and 8T SRAM

SRAM TYPE	Power (nW)	Write Delay (ns)	Read Delay (ns)	PDP (nW/S)
6T SRAM	56.1	1.28	1.56	79.66
6T SRAM PG	26.5	0.72	0.96	22.26
8T SRAM	38.1	1.01	1.34	44.77
8T SRAM PG	22.4	0.67	0.84	16.912

Table I shows the comparison table of 6T and 8T SRAM cell with and without power gating technique. The average power consumption, write-delay, read-delay and power-delay-product are calculated for various SRAM cells: Conventional 6T SRAM cell, power gated 6T SRAM, 8T SRAM and power gated 8T SRAM. Schematics of the circuits are designed and simulated in 130nm technology with 1.2V VDD using Tanner EDA. The transistors are sized in a way to obtain equal delay for the pull up and pull down networks.

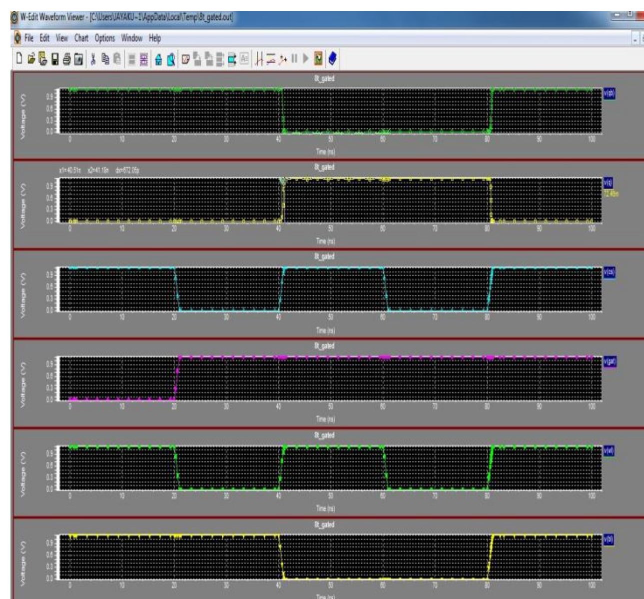

Fig.4 Simulation result of proposed 8T SRAM cell

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Average power consumed by the conventional 6T SRAM cell is 56.1nW, power gated 6T SRAM is 26.5nW, 8T SRAM is 38.1nW and power gated 8T SRAM is 22.4nW. Write and read delay is also analyzed for all the types and PDP also shows that the proposed power gated 8T SRAM results in optimized value at 16.912(nW/S). Fig.4 shows the W-edit output of proposed 8T SRAM cell. BL is the data in bit line and WL is the word line enable signal with Q and Qb is the stored data.

VI. CONCLUSION

The power gating method for 8T SRAM cells have been designed using 130nm technology is proposed. The proposed SRAM cell is more stable in comparison to conventional 6-T SRAM cell. The result shows that the proposed power gated 8T SRAM cell has lesser probability of read/write failure and worked efficiently during both read and writes operations. Although numbers of transistors and area are increased in comparison to those of conventional SRAM cell but low power dissipation and higher stability can easily dominate over this drawback. The proposed 8T SRAM cell achieves 60% power savings and 78.7% PDP when compared with the conventional 6T SRAM with very small transistor overhead.

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