IJIREEICE

ISSN (Online) 2321-2004
ISSN (Print) 2321-5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

Vol. 7, Issue 3, March 2019

Performance Analysis of Fully-Depleted Silicon-On-Insulator (SOI) G^4-FET and Gate-All-Around (GAA) MOSFETs

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Abstract: The performance of fully-depleted Silicon-On-Insulator (SOI) Four Gate Transistor (G^4-FET) and Gate-All-Around (GAA) MOSFETs are investigated. Threshold voltage, Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL), maximum drain current are calculated and compared.

Keywords: Silicon-on-Insulator (SOI), Four Gate Transistor (G^4-FET), Gate-All-Around (GAA), Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL)

I. INTRODUCTION

The continuous scaling of GAA silicon nanowire Field Effect Transistor (FET) [1], [2] illustrates better control of short channel effect over other structures [3] due to their gate controllability, low leakage, high on-off ratio and carrier transport property [4]. For better SS and DIBL, channel length, channel width, channel height, oxide thickness can be considered as important design parameters [5], [6]. The G^4-FET which is a double gate MOSFET consisting of two lateral junction-gates and it has a lateral double-gate MOS consisting of two vertical MOS gates (top-gate and bottom-gate). In GAA MOSFETs, the gate oxide and the gate electrodes wrap around the channel region. G^4-FET and GAA MOSFETs based circuits are feasible with a fully-depleted SOI process without requiring any additional fabrication steps. Drain current flows through the channel and the conducting channel surrounded by the depletion regions.

In this paper, threshold voltage, SS, DIBL, maximum drain current of G^4-FET and GAA MOSFETs are calculated and compared.

II. G^4-FET AND GAA MOSFETs DEVICE STRUCTURE AND SIMULATION

In this work, we demonstrate the 90-nm fully depleted SOI G^4-FET and GAA MOSFETs structures. Device simulations were performed by 3D SILVACO/ATLAS simulator. Device parameters of G^4-FET and GAA MOSFETs are given below:

Table I Device Parameters of G^4-FET and GAA MOSFETS

Device parameters	G^4-FET	Cylindrical GAA MOSFET	Cubical GAA MOSFET
Channel length	90 nm	90 nm	90 nm
Channel width/ Channel diameter	90 nm	90 nm	90 nm
Channel height	90 nm	-	90 nm
Gate oxide thickness/ surrounding gate oxide thickness	2 nm	2 nm	2 nm
Buried oxide thickness	2 nm	-	-
Top gate thickness/ surrounding gate thickness	20 nm	20 nm	20 nm
Bottom gate thickness	20 nm	-	-
Junction gates width	40 nm	-	-
Doping density of junction gates (p^+)	1×10^{20} cm^{-3}	-	-
Channel doping density (n)	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
doping density of drain and source (n^+)	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}

 DOI 10.17148/IJIREEICE.2019.7301

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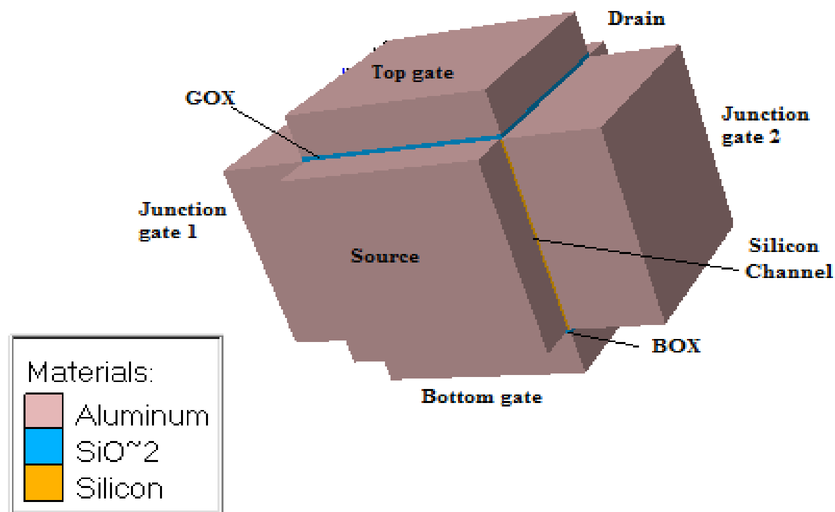

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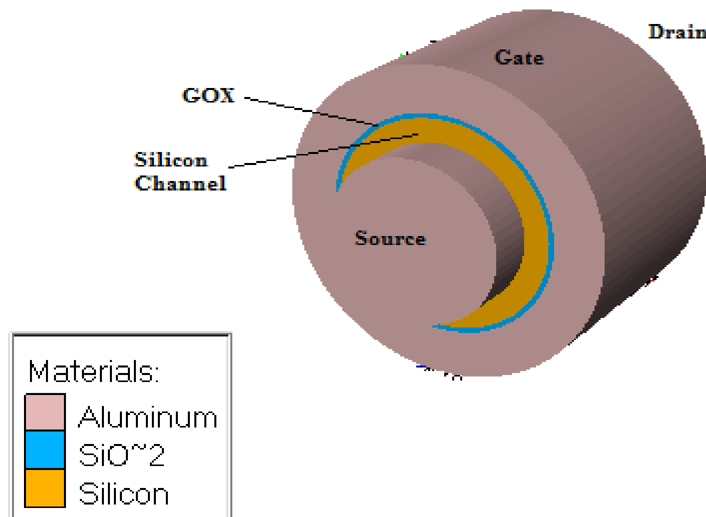

(b)

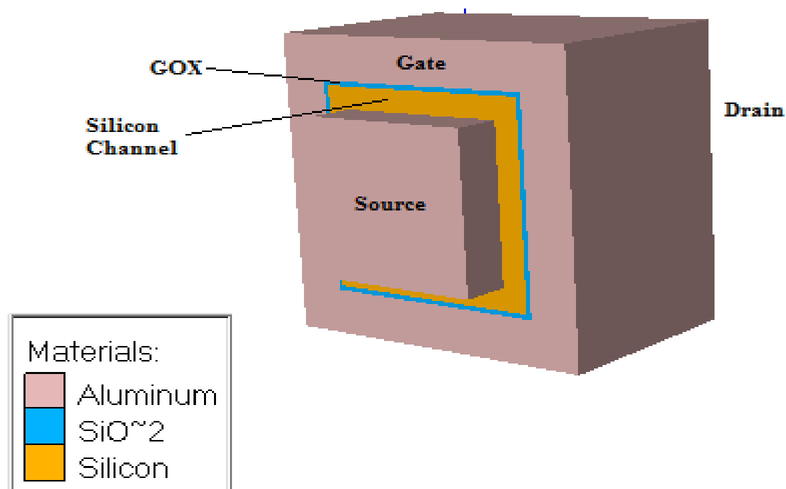

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Fig. 1 (a) G^4-FET structure, (b) Cylindrical GAA MOSFET structure, (c) Cubical GAA MOSFET structure

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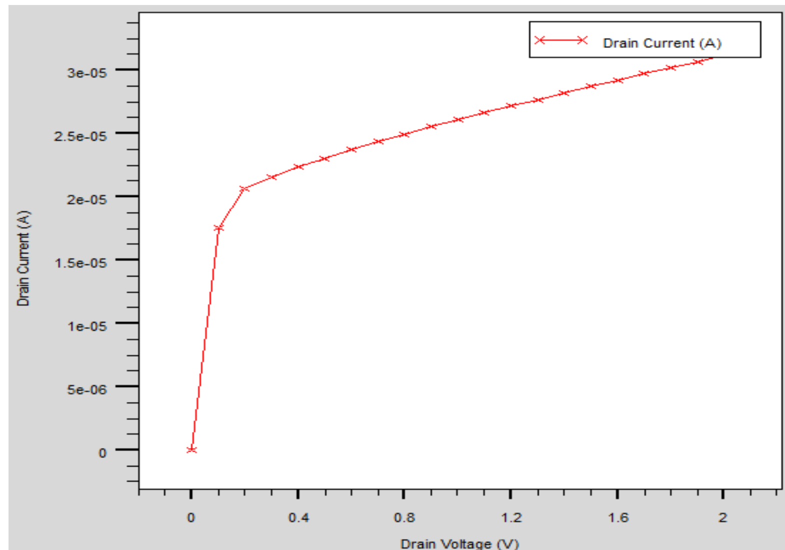
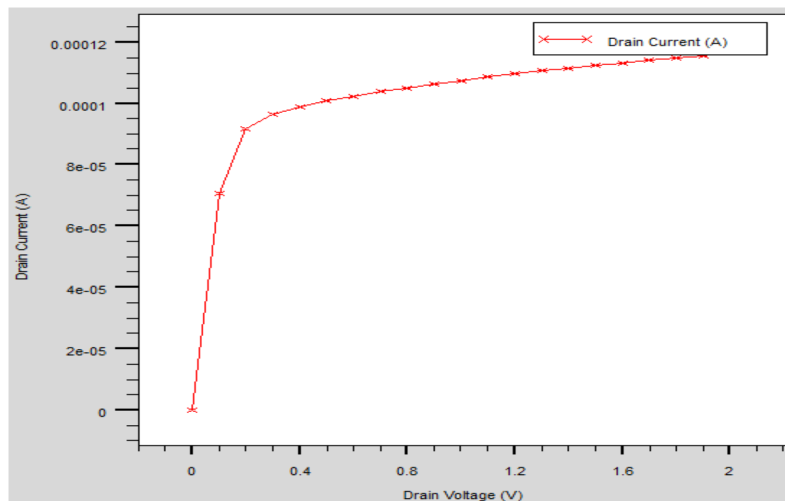


(a)



(b)

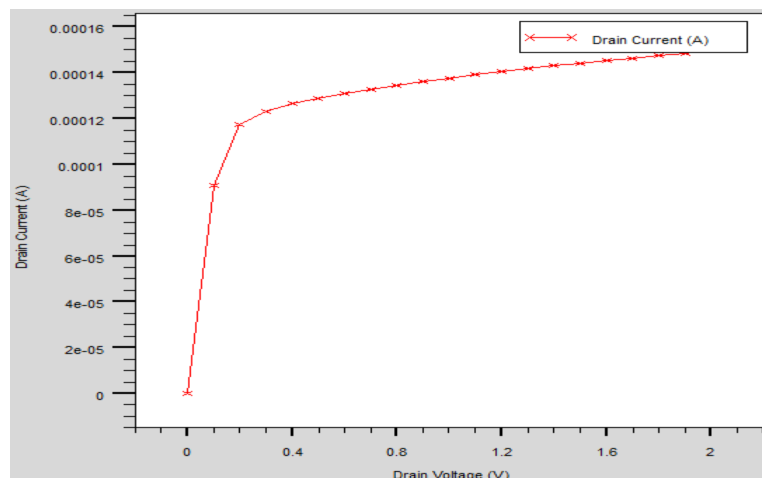


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Fig. 2 Current-Voltage characteristics at Vg= 0.2 V of (a) G^4-FET, (b) Cylindrical GAA MOSFET, (c) Cubical GAA MOSFET

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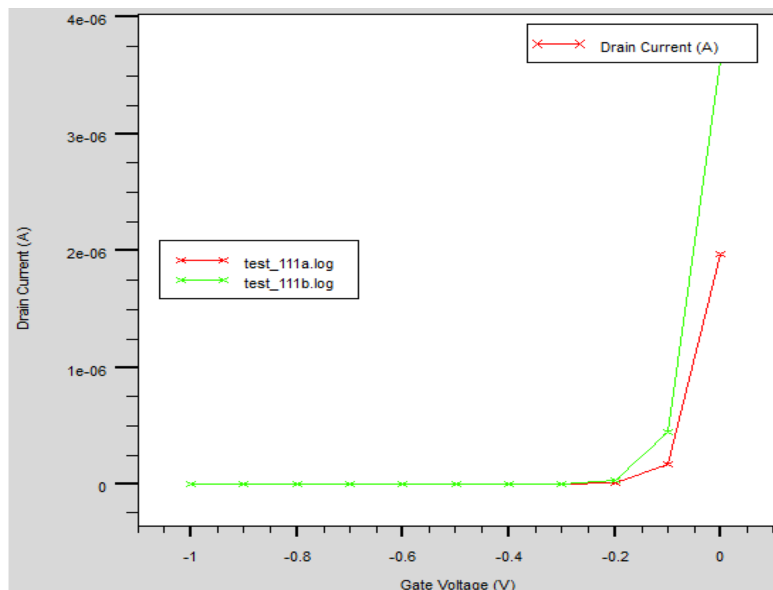
III. RESULTS AND DISCUSSIONS

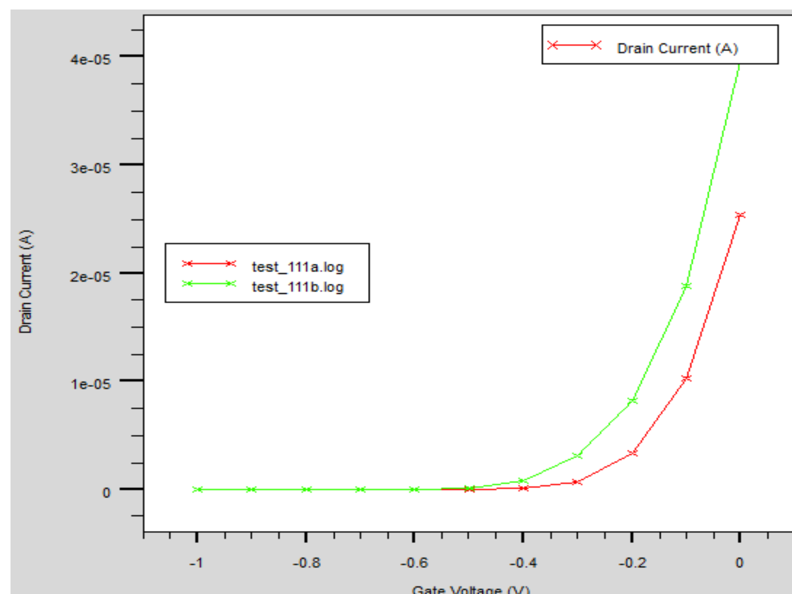
Fig. 2 shows the current-voltage characteristics of G^4-FET and GAA MOSFETs. Maximum drain current of cubical GAA MOSFET is larger than other two structures (Table II). DIBL was calculated as the difference in threshold voltage when the drain voltage was increased from 0.1 to 0.8 V. Fig. 3 shows the transfer characteristics of G^4-FET and GAA MOSFETs. Threshold voltage of cubical GAA MOSFET is smaller than other two structures. But SS and DIBL of G^4-FET are smaller than other two structures.

Table II Results of G^4-FET and GAA MOSFETs Simulations

Properties	G^4-FET	Cylindrical GAA MOSFET	Cubical GAA MOSFET
V_{TH}	-0.1095 V	-0.1676 V	-0.1682 V
SS	77.93 mV/dec	89.04 mV/dec	98.48 mV/dec
DIBL	6.66 mV/V	32.56 mV/V	37.02 mV/V
I_{max}	31.17 µA	116.4 µA	149.56 µA



(a)



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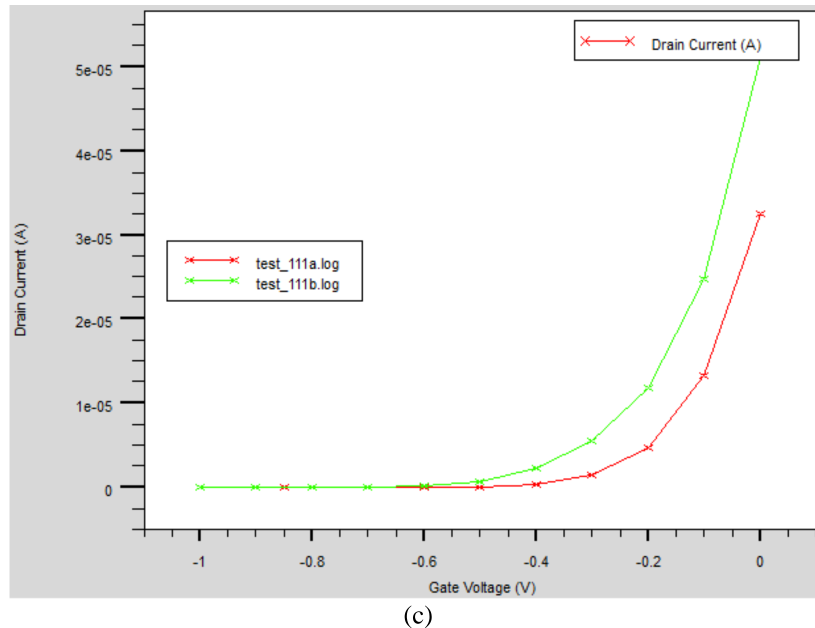

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Fig. 3 Transfer characteristics of (a) G^4-FET, (b) Cylindrical GAA MOSFET, (c) Cubical GAA MOSFET

CONCLUSION

We compared SOI G^4-FET and GAA MOSFETs through 3D SILVACO/ATLAS simulator. Threshold voltage, SS, DIBL, maximum drain current are calculated and compared. In the future these devices can be used in the fast switching circuits.

ACKNOWLEDGMENT

The authors acknowledge the contribution of the Department of Electrical and Electronic Engineering, Sonargaon University (SU) for the permission to use computing facilities.

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