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Comparative Study of Fault Detection Techniques in Digital Circuits

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Abstract: The integration level in today's word is continuously increasing in VLSI chips. So that complexity of testing is a major challenge. That is because the internal chip modules have become increasingly midcult to access. There is a significant amount of the testing cost as compared to the total manufacturing cost. Hence there is a necessity to reduce the testing cost. The main factor is the time required to test the circuitry that has the biggest impact on testing cost of a chip. This time can be decreased by reducing the number of tests required to test the chip. So, we simply need to devise a test set that should be small in size. There is one way to generate a small test set is to compact a large test set parameters. The main drawback of the compaction results on the quality of the original test set. This aspect of compaction has motivated the work presented here with some methods of fault detection and avoidance techniques to test the circuit for a fault-free environment.

Keywords: Test circuits, Physical redundancy, Time redundancy, Monotonic logic, Self-checking circuits

I. INTRODUCTION

There is a main aspect of the VLSI process is to analyse the failure that is the process of detecting the cause of failure of any chip. Once a chip has failed in a test, the important thing is to determine the cause of its failure as this can lead to improvement in the design of the chip and the manufacturing process. The first step in failure analysis is Fault detection in which by logical analysis we can find a list of likely defect sites or regions. Basically fault diagnosis or detection minuscule the effective testing area of the chip. Several fault categorization and positioning techniques have been propounded and they can be classified with systematic techniques. Fault categorization defines the type of fault on the fault levels in the system. There are different techniques introduced for the defect diagnosis in circuits.

II. LITERATURE SURVEY

It is already surveyed on the redundancy methods for error diagnosis. It includes various methods like resemblance with duality expression logic, time redundancy method, Self-checking circuits and memory arrays methods etc [1]. In [2], applications of very basic views and ideas, motivation, and methods of defect tolerance have been propounded. The topics include fault categorization, redundancy methods, reliability design, prospective of fault tolerance system and some methodologies to short out the fault tolerant challenges. In [3] introduces the different fault detecting methods for digital and analog integrated circuits. It includes the small test set method where fault can be detected in the minimum time. One more technique is introduced in this paper named as differential measurement technique. This technique is very helpful to catch whether the circuit is error free or not. In [4], introduces a testing simulator named as deductive fault simulator for digital circuits. It has ten gates and three inputs with one output set that generate comparison results by simulation encryption. This simulator justifies its adequacy for fault diagnosis by meticulous results and calculations. In [5] proposes a very strong and adaptable testing technique for single failure named as signature analysis. This technique is very effective and beneficial because of its reappearing quality. In [6] shows an error-diagnosis circuit. In this the error can be detected using the given encryption by putting 1 on the upper right. A register stores the first seven digits of the encryption consequently it is cycled with the feedback shift register. The 3 bits arrive at every seventh bit of the cycle. These three check bits should be zero, if these are non zero then there is a fault. In [7], the authors examined the techniques for error detection and test minimization in two levels combinational circuits. Here are total 11 techniques surveyed that varies from foundation to the modern fast adaptive techniques. Advantages and disadvantages of those techniques are examined here. Also in [8] shows that research area of software fault tolerance is an imperfect area of research. It is an unfledged area towards complex systems mainly in terms of the security based systems. It is suitable with the combination of hardware fault tolerance to resolve fabrication fault complications. Reference [9], proposes an error testing method named as Fault injection. It is used for the assessment of device metrics

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such as stability, security and fault treatment of the object system. Fault injection infuses error into the system and observes the system to examine its conducts towards faults.

A planning for a circuit synthesis may be unsuccessful at the level of verifications. It will demote the class of effects and decisions. There may be origins for the wrecks as
a. Verification was not right.
b. The synthesis process was incorrect.
c. The circuit plan was inaccurate.
d. The requirements were improper the function of verification is much valuable to discover whether something proceeding incorrect. On the other hand the position of diagnosis is also much essential to decide precisely what is going fallacious seeing as accuracy and usefulness of verification is very seminal for the grade of creations.

III. PROPOSED DEFECT DETECTION TECHNIQUES

Here are five proposed techniques for detection and location of faults present in a circuit.
A. Duplication with complementary logic with the use of dual expression.
B. Permanent fault detection using time redundancy.
C. Self-checking circuit technique.
D. Monotonic logic technique.
E. Boolean Difference technique.

A. Duplication With Complementary Logic Techniques

In complementary logic one function is designed using positive logic as **F** and the other function is designed using negative logic as $\mathbf{F_d}$. The outputs must be complementary to each other if the operation is correct. In positive logic, higher voltage represents logic 1 and lower voltage represents logic 0. In negative logic, lower voltage represents logic 1 and higher voltage represents logic 0.If we know function **F** realized in positive logic, than we can determine function realized in negative logic by computing the dual of F. Dual of F can be obtained as follows (1):

(i) Replace AND with OR, and OR with AND
(ii) (ii) replace 0 with 1, and 1 with 0.

Let function F be $\mathbf{F = xy2 + z}$ then after using complementary logic we would get $\mathbf{Fd = (x + y2)z.}$

Use of dual complementation forces the use of separate masks for two modules – decrease the probability of common-mode faults.* Corresponding lines in two modules are always at different voltage levels – a short between two such line results in one line having error, and another – not, i.e. fault will be detected according to XOR gate logic.

Table: 1: Truth Table For XOR gate

a	b	c
0	0	0
0	1	1
1	0	1
1	1	0

Only when F and F_d will be complementary to each other the result will be high as 1, otherwise there may be a fault if output is 0, from this we can detect the fault in the circuit. Moreover this technique of testing can be done using half subtractor circuit. Fig 1 shows the half subtractor circuit and its complementary module circuit which is tested by the XOR gate using MATLAB software.

For any input given to this circuit the result is that the first xor gate gives 1 and second XOR gate gives 0, So if there is any fault is in the circuit then result of anyone of XOR gate may change or both the result of XOR gate may change.
In such a way the fault can be detected in the circuit. It is a very good and a simple technique of fault detection but it has some drawbacks also that it cannot detect the location of fault exactly. Only fault detection is possible by this technique. Second drawback is complexity issue. Circuit testing would be more cost effective with the increase of complexity in this technique.

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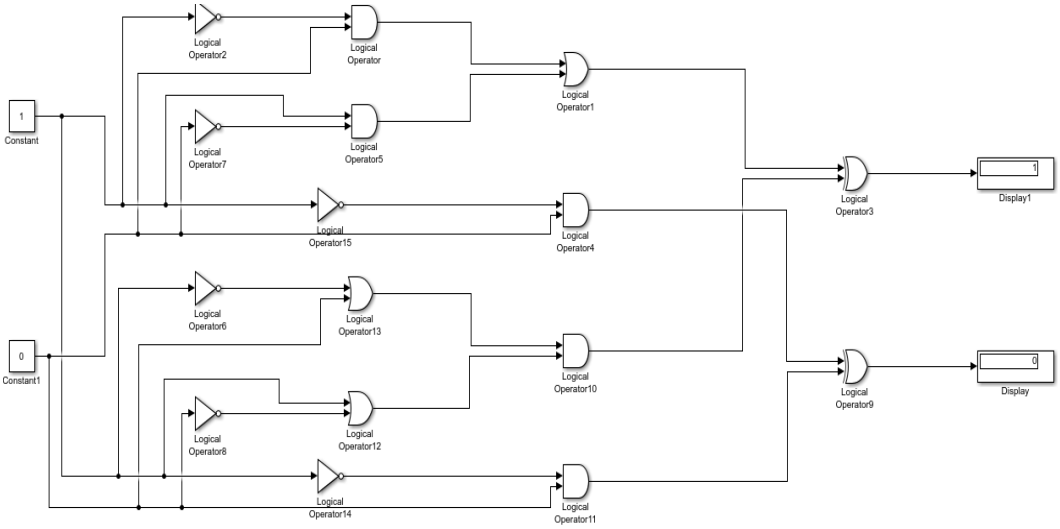

Figure1. Half subtractor circuit implementing duplication with complementary logic

B. Permanent Fault Detection Using Time Redundancy-

Time redundancy is great technique which minimizes the error diagnosis hardware by taking some additional time. The main abstraction of time redundancy is to reproduce operations in a way both transient and permanent faults can be easily detected. Fig 5.3 is showing the method to detect transient fault. The data must be reformed when it is executed the next time to detect permanent faults using this technique. At the last the stored results are compared by the comparator. Consequently it detects faults by the comparison of stored results. This technique is all depends upon reformation of operation with time.

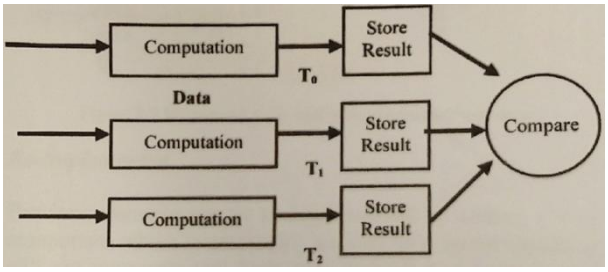

Figure2. Time redundancy block diagram

The major drawbacks of this techniques are time, cost and delay. In this technique due to the duplicate and compare approach the all loss and penalty paid an extra hardware.

C. Monotonic Logic-

A circuit is monotonic if it implements a monotonic function – e.g. a monotonically increasing function increases of stays unchanged when the input value increases. Any circuit composed of AND and OR gates is monotonic. Any single stuck-at fault will cause only unidirectional errors on the output.

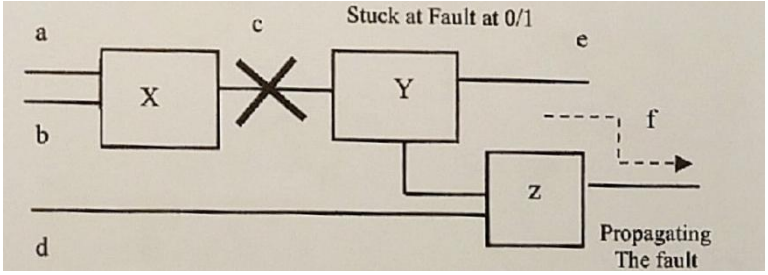

Figure. 3 Monotonic logic circuit at stuck at fault

Suppose there is a single stuck at fault 0/1 error at the C, output of the circuit X .There may be chances of faults at the output f because the C is faulty input for circuit Y. Now z would propagate the fault from C to total circuit output f.

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This is also a fault detection technique by monotonic logic. The best part of this technique is that the fault can be avoided by re-implementing the circuit using another approach.

Re-Implementation Of Monotonic Logic Circuit

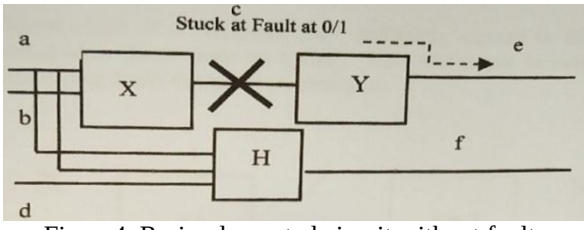

Figure4. Re-implemented circuit without fault

Re-implementation of the circuit introduced a new circuit part H which is an extra circuit for inputs a and b. Therefore the signal c cannot propagate its error. That is the best way to avoid the fault by this technique. This technique is done in half subtractor circuit with stuck at fault error. There is the fault at the one output and fault is propagating through another circuit that is why other output also found faulty. In this case LEDs cannot blink due to the fault in the circuit.

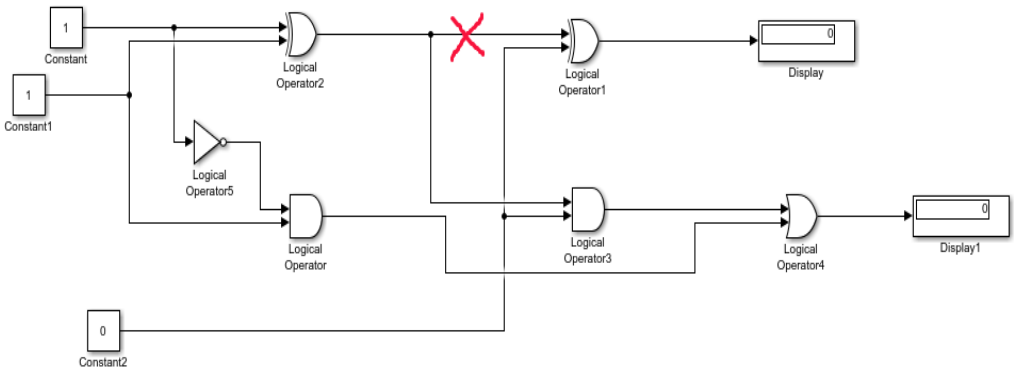

Figure5. Monotonic logic half subtractor circuit at stuck at fault

For this circuit whatever be the given input the output will not change because the there is stuck at fault 0 (denoted by the cross sign) in the circuit due to which the result will remain the same which is zero.

Re-Implemented Monotonic Logic Half Subtractor

Previous example can be re-implemented by adding a new component which is associated directly to original inputs. It will not propagate any fault even if fault is present in any other component. This technique of fault avoidance can avoid at least one fault in the circuit and the remaining circuit can work properly.

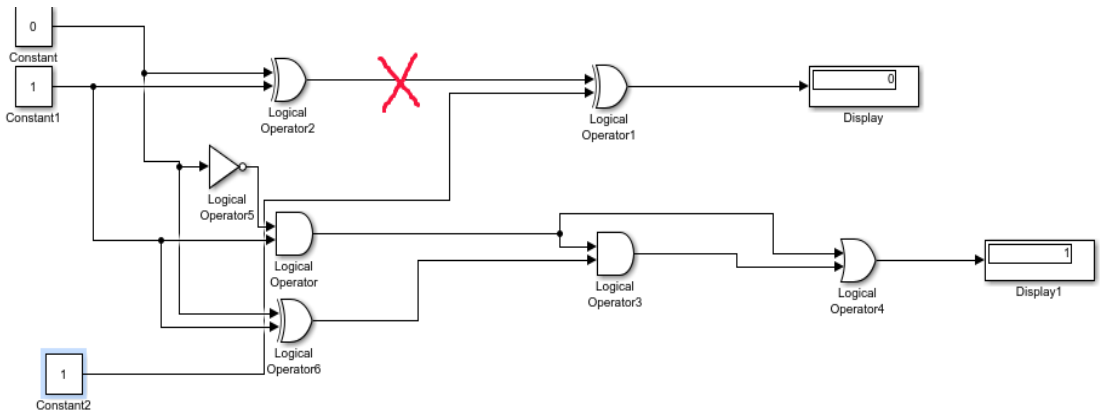

Figure6. Monotonic logic half subtractor re-implemented circuit.

After reimplementation of the previous circuit, the fault can now be successfully avoided by bypassing through another way and thus the result can be produced from giving desired input.

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D. Self-Checking Circuits-

A Self checking circuit is an approach that promptly detects error by comparing input of circuit to the output of reverse circuit. Consider there is a circuit H whose input is X and output is Z. Another circuit present here is H-1 which is inverse of the previous circuit H. It is confirmed if Z is the input of the circuit H-1, the output would be X only.
Meanwhile if it happens then definitely circuit is fault free otherwise there may be a fault. This technique is called self checking fault detection technique.

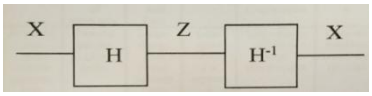

Figure7. Time redundancy block diagram

Half subtractor circuit also can execute by the self checking circuit verification using inverse abstraction.

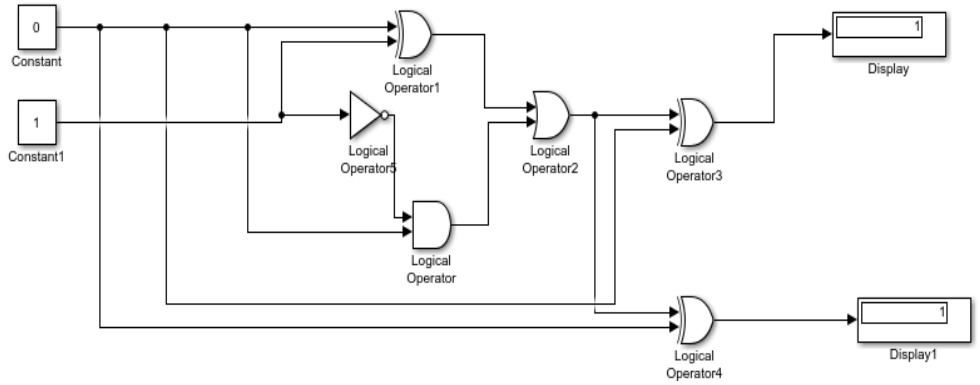

Figure8. Half subtractor circuit executed as self checking circuit

A self checking circuit is an approach that promptly detects error by comparing input of circuit to the output of reverse circuit.

Table: 2: Truth Table For Half Subtractor

INPUT		OUTPUT	
X	**Y**	**D**	**B**
0	**0**	**0**	**0**
0	**1**	**1**	**1**
1	**0**	**1**	**0**
1	**1**	**0**	**0**

Table: 3: The Inverse of Table 2

INPUT		OUTPUT	
X	**Y**	**D**	**B**
0	**0**	**0**	**0**
0	**1**	**1**	**1**
1	**0**	**0**	**0**
1	**1**	**1**	**1**

E. Boolean difference technique-

The Boolean difference is a well-known mathematical concept which has found significant application in the single fault analysis of combinational logic circuits. One of the primary attributes of the Boolean difference in such situations is its completeness. This technique is very attractive as it makes many problems quite simple to solve. Anyone who has attempted to solve problems by changing inputs 0 to 1 to analyse the consequences will appreciate this technique.

Let there be a logic function that has one output F and n inputs $x1, x2, x3, \ldots\ldots xn$, so that $F(x) = F(x_1, x_2, x_3, \ldots\ldots x_n)$. If one of the input of the logic function is in error, let input xi, then the output would be $F(x) = F\left(x_1, x_2, x_3, \underset{xi}{\leftarrow} \ldots\ldots x_n\right)$. To analyze the action of the logic circuit when an error occurs, it is desirable to know under what circumstances the two outputs are the same. For this purpose, the Boolean difference of F (x) with respect to x. is defined as follows. (It is to be noted here that this is not a derivative. The notation is used because it is convenient.).

$\frac{dF(x)}{dxi} = F(x_{1,\ldots} x_i, \ldots x_n) \oplus F(x_{1,\ldots} \bar{x}_i, \ldots x_n)$

Where the sign + appears it means Exclusive OR. Based on above definition, a set of important operation properties can be derived as follows:

a) $\overline{\frac{dF(x)}{dx_i}} = \frac{dF(x)}{dx_i}$ b) $\frac{dF(x)}{dx_i} = \frac{dF(x)}{d\bar{x}_i}$ c) $\frac{d}{dx_i}\left(\frac{dF(x)}{dx_i}\right) = \frac{d}{dx_i}\left(\frac{dF(x)}{dx_i}\right)$

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d) $\frac{d\,F(x)G(x)}{dx_i} = F(x)\left(\frac{dG(x)}{dx_i}\right) \oplus G(x)\left(\frac{dF(x)}{dx_i}\right) \oplus \frac{dF(x)}{dx_i} \cdot \frac{dG(x)}{dx_i}$

e) $\frac{d\,F(x)+G(x)}{dx_i} = \overline{F(x)}\left(\frac{dG(x)}{dx_i}\right) \oplus \overline{G(x)}\left(\frac{dF(x)}{dx_i}\right) \oplus \frac{dF(x)}{dx_i} \cdot \frac{dG(x)}{dx_i}$

These properties can be derived in a straightforward manner and are useful in calculating the Boolean difference.
The most important property of the Boolean difference is that it is equal to 1 when the logic outputs are different for normal and erroneous setting of input $x_{i,}$ and equal to zero if the logic output is same for both normal and erroneous setting of input x_i. This is the basis for the use of the Boolean difference in the analysis of errors. A Boolean function F (x) is said to be independent of X. if and only if F(x) is logically invariant under complementation of x. If now F(x) is an output function, then we say F(x) is independent of switch x_i if and only if for any position of other switches the output F(x) is independent of position of x. This implies a very important point, namely that an error in x. will not affect the final output F(x).
It can be easily proved that a necessary and sufficient condition that a function F (x) be independent of x_i is that

f) $\frac{dF(x)}{dx_i} = 0$

And thereby the following additional properties can be derived very easily

g) $\frac{dF(x)}{dx_i} = 0$

If F(x) is independent of $x_{i.}$

h) $\frac{dF(x)}{dx_i} = 1$

If F(x) depends only on $x_{i.}$

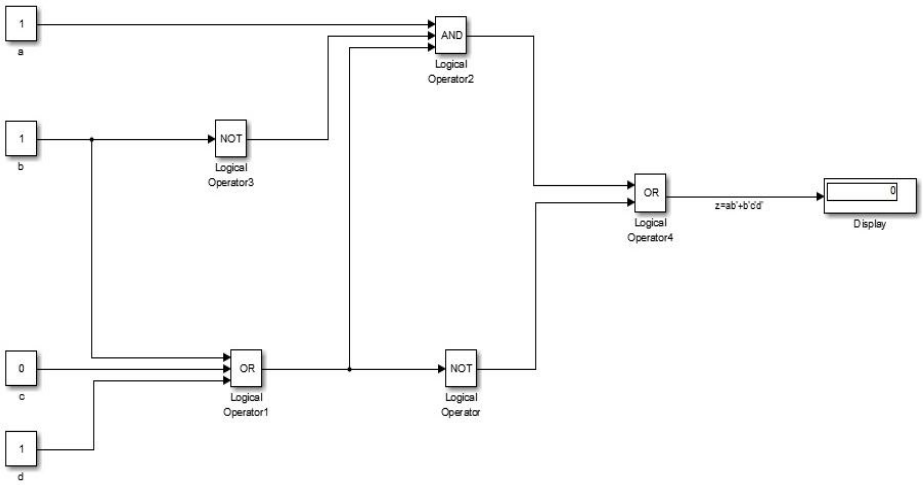
i) $\frac{d\,F(x)G(x)}{dx_i} = F(x)\frac{dG(x)}{dx_i}$

If F(x) is independent of $x_{i.}$

j) $\frac{d\,F(x)+G(x)}{dx_i} = \overline{F(x)}\frac{dG(x)}{dx_i}$

If F(x) depends only on $x_{i.}$

The above idea has been generalized for multiple error case.
Despite substantial success in improving circuit reliability in recent years, there is growing interest in techniques for detecting and locating failures in complex digital networks. There are two basic approaches to testing digital systems: functional and structural. In functional testing the aim is to verify that the unit under test behaves as required, by determining whether it executes its task properly. The tests based on structural considerations, on the other hand, are designed to assure that the individual hardware constituents of a unit are operating correctly.
For The Boolean difference techniques we are taking one examples:



From the above figure it is clear that

$z = a\bar{b}(b + c + d) = a\bar{b}(c + d) + \bar{b}(\bar{c}\bar{d})$
$= \bar{b}a(c + d) + \bar{c}\bar{d} = \bar{b}a + \bar{c}\bar{d}$

Now the condition for a sensitive path from lead "a" through the AND gate to the output are all the independent inputs that satisfy the following expression:

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$$\frac{dz}{da} = (\bar{b} + \bar{b}\bar{c}\bar{d}) \oplus \bar{b}\bar{c}\bar{d} = \bar{b}c + \bar{b}d = 1$$

To provoke the fault lead "a" stuck at 1, it is required that a=0, hence a=l. This condition together with the one that assures a sensitive path is met by the solutions to which comprises the set of all tests for lead "a".

$$\bar{a}(\bar{b}c + \bar{b}d) = 1$$

IV. RESULTS & DISCUSSION

Table: 4: Comparison Matrix For Different Fault Detection Techniques

Method	Speed of detection	Area and Cost	Delay	Power consumption	Coverage
Duplication with complementary logic with the use of dual expression.	Fast as per gate delay.	Large due to dual circuit addition cost high.	Less same circuitry is repeated.	Large due to effective large effective area.	Good all manifest errors are detected.
Permanent fault detection using time redundancy	Slow every stored value and compare or take different times	Large due to redundant hardware cost low.	Large every redundant component provides delay.	Very high due to redundant hardware	Very good transient fault and permanent fault can be detected.
Self-checking circuit technique.	Medium depend upon the circuit complexity.	Medium depend upon the logic gate required. Cost less.	Less- inputs and outputs would be same.	Medium depend upon the logic gate required.	Medium not practical for all type of functionality
Monotonic logic technique.	Fast as per gate delay.	Small-depends upon the circuit. Cost very low.	Medium depend upon the circuit complexity.	Medium depend upon the circuit complexity.	Good-multiple faults are avoided.
Boolean Difference technique	Fast as per gate delay	Small-depends upon the circuit. Cost very low.	Medium depend upon the circuit complexity	Medium depend upon the circuit complexity.	Very good transient fault and permanent fault can be detected.

From the results of above table, different types of errors could be categorized and positioned on the circuit with strong fidelity. This shows that the suggested methods are capable to provide satisfactory precision in both of the fault categorization, and fault evaluation.

CONCLUSION

The current work accomplished in this paper comprised of the review of different techniques used for detecting errors in combinational digital circuits with representative examples. VLSI permits us to integrate maximum circuitry in compact and more trust worthy collection. Fault detection and fault location can now be contributed inside the IC level. VLSI performs the feasibility for enhancing the design performance of fault tolerant systems by using some class of techniques all through the system. The consequent works will be to explore the nature of the different fault detection techniques and originate the model depending on the present work findings.

REFERENCES

[1]. P. N. Kandasamy, "Defect Tolerance in VLSI Circuits ∗," pp. 1– 10, 1989.
[2]. A. Avizienis, "Fault-Tolerant Systems," vol. C, no. 12, pp. 1304– 1312, 1976.
[3]. R. H. Khade and D. S. Chaudhari, "a review of methodologies for testing and locating faults in integrated circuits," vol. 3, no. 6, 239–241, 2014.
[4]. A. K. Jameil, "a new single stuck fault detection algorithm for digital circuits," vol. 3, no. 1, pp. 1050–1056, 2015.
[5]. P. R. H. Khade and S. Gourkar, "Fault Testing of CMOS Integrated Circuits Using Signature Analysis Method," vol. 2, no. 5, pp.73, 2013.
[6]. E. Engineering and S. Exchange, "digital logic - Error-Detection Circuit -- How does this work ? - Electrica ... minute : Error- Detection Circuit — How does this work ?," pp. 12–13, 2016.
[7]. S. M. Thamarai, K. Kuppusamy, and T. Meyyappan, "Fault Detection and Test Minimization Methods for Combinational Circuits - A Survey," vol. 2, pp. 140–146, 2011.
[8]. D. Embedded, S. Spring, and C. Inacio, "Abstract : Related Topics : Contents :," pp. 1–9, 2016.
[9]. C. Science and S. Engineering, "Fault Injection and Its Techniques," vol. 4, no. 4, pp. 970–974, 2014.