Design and Implementation of Dual Core and Quad Core Processor in Vertex 6 FPGA Using Pipelined RISC Architecture

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Abstract: This paper describes the design of a dual and quad core pipelined Reduced Instruction Set Computer (RISC) processor using Verilog HDL and its implementation in vertex 6 FPGA. Dual and quad core processor consumes less power with high efficiency. The processor has instruction and data memory spaces are both physically and logically separate called Harvard memory architecture. Single core have 5 bit opcode, 23 set of instructions and it is designed by using the pipelining which increase speed of processor. The processor design is done by using RISC architecture which involves Registers (General purpose), Arithmetic and Logical Unit (ALU), Memory (Data and program) with pipeline techniques. Load and Store instructions used to access memory. The comparison of dual and quad core RISC architecture in terms of structure and power consumption is explained in paper with design summary.

Keywords: RISC characteristics, Pipelining, Memory, Load and Store, dual core processor, quad core processor

I. INTRODUCTION

The Processor is a logic circuitry (programmable) that takes in input, performs arithmetic or logical operations based on the program stored in memory and then produces output. Processor is also an electronic circuit that functions as the Central Processing Unit (CPU) of a computer, which controls complete computational tasks. The simple design technology and the decreasing cost of the integrated circuit leads RISC processor is most used in every area. The simple design gives higher performance, less cost, compatible systems. This technology is most used in many applications such as data processing, scientific and engineering applications and real-time control. In the present work, the design of dual core and quad core processor is presented. Each core is having design of a 4-bit data width Reduced Instruction Set Computer (RISC) processor. It has a complete instruction set, program and data memories, general purpose registers and a simple Arithmetical Logical Unit (ALU) for basic operations. In electronics, a HDL is a specialized computer language used to program the structure, design and operation of electronic circuits, and most commonly, digital logic circuits. Verilog is a Hardware Description Language; a textual format for describing electronic circuits and systems. Verilog is intended to be used for verification through simulation, for timing analysis, for test analysis and for logic synthesis. It means that by using HDL one can describe any hardware at any level. HDL's allows the design to be simulated earlier in the design cycle in order to correct errors or experiment with different architectures. Some of the advantages of HDL are technology-independent, easy to design and debug, and are usually more readable than schematics, particularly for large circuits. The dual core and quad core designed and synthesized with the help of Verilog HDL by considering RISC architecture which leads high efficiency, simple design and simulated using Modelsim. The design machine cycle instructions allow the processor to handle several instructions at the same time, so processor work at a high clock frequency, yields higher speed. The RISC architecture follows single-cycle instruction execution.

II. RISC ARCHITECTURE

RISC processors use a small and limited number of instructions and it consume less power and has high performance. Each instruction is very simple and consistent also it use simple addressing modes with uniform fixed length instructions. RISC processors use large number of Registers for passing arguments and holding the local variables. In a RISC machine, the instruction set is based upon a load store approach. Only load and store instructions access memory. RISC is a type of microprocessor architecture that uses highly-optimized set of instructions. RISC reducing the cycles per instruction at the cost of the number of instructions per program Pipelining is one of the unique features of RISC. It is performed by overlapping the execution of several instructions in a pipeline fashion. It has a high performance advantage over CISC. The speed of the operation can be maximized and the execution time can be minimized. The block diagram of general RISC architecture is shown in figure 1.
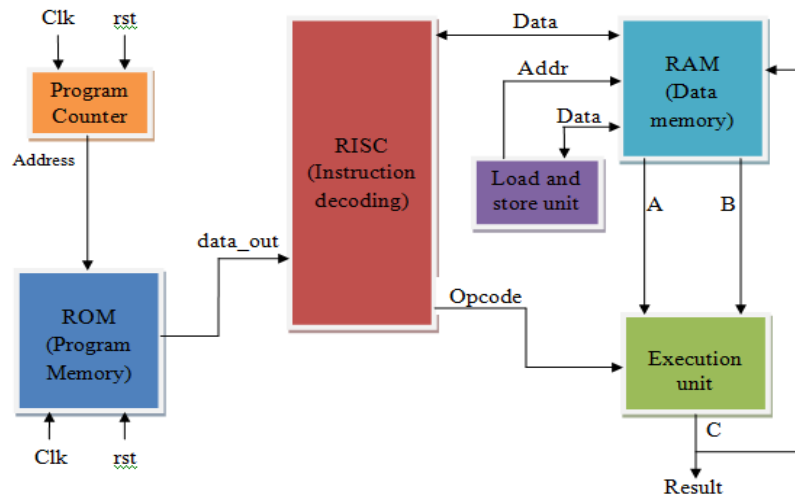
Figure 1: Block diagram of RISC architecture

Pipelining used to improve both Cycle per Instruction and system performance. Pipelining allows a processor to work on different steps of the instruction at the same time leads many instructions can be executed in a small period of time. RISC designed by using four stages of pipeline techniques such as Fetch, Decode, Execute, and Store result. In Fetch Stage the content of the Program Counter is used to access memory and fetch the next instruction to be executed. In Decode Stage the instruction is decoded and the required operands are retrieved from the general purpose registers. In Execute Stage any calculations are performed. This includes effective address calculation for Load or Store instructions. The subsequently Program Counter value is also calculated during this stage of the pipeline so that branches, can be executed. In Store, the results of the calculation from the Execute stage, or the memory load from the Memory access stage, are updated into the general purpose registers. The instruction format is of register type and instruction of 17 bit with opcode 5bit and three operands of each 4 bit are shown in figure 2.
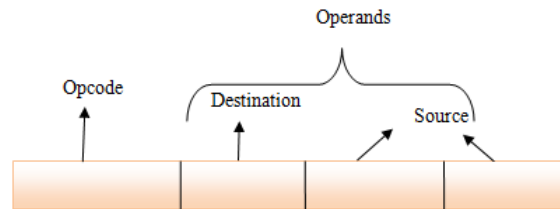

Figure 2: instruction format

Program Memory is implemented as a ROM consists of 23 set of instructions which is accessed by CPU during operation. Data Memory is implemented as RAM. Memory model pre-loads initial data from the Register file and dumps its content into file after the simulation is finished. If the instruction is a load, then read from memory using the effective address computed in the previous cycle. If the instruction is a store, then the data from the second register read from the register file is written into memory using the effective address.

III.   DUAL AND QUAD CORE ARCHITECTURE

A multi-core processor is a single computing component with two or more independent processing units called cores, which read and execute program instructions. The instructions are ordinary CPU instructions but the single processor can run multiple instructions on separate cores at the same time, increasing overall speed for programs amenable to parallel computing. In this architecture, special load and store instructions are used to move data between the processor's internal registers and memory

i.   Dual Core: Dual core is a CPU that has two distinct processors that work simultaneously in the same integrated circuit. This type of processor can function as efficiently as a single processor but can perform operations up to twice as quickly because the operating system is able to handle most of the tasks in parallel. The block diagram of dual core processor which having two cores (works parallel) designed using RISC architecture is shown in figure 3.
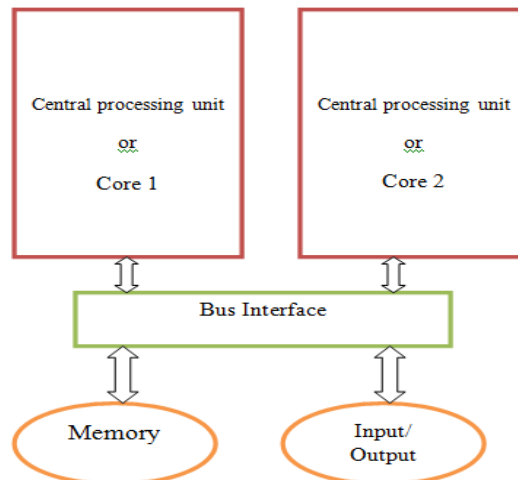
Figure 3: Dual core RISC architecture

ii.   Quad Core: Quad core is a CPU that has four distinct processors that work simultaneously in the same integrated circuit can perform operations up to four times as quickly because the operating system is able to handle most of the tasks in parallel. The block diagram of quad core processor which having four cores (works parallel) designed using RISC architecture is shown in figure 4.
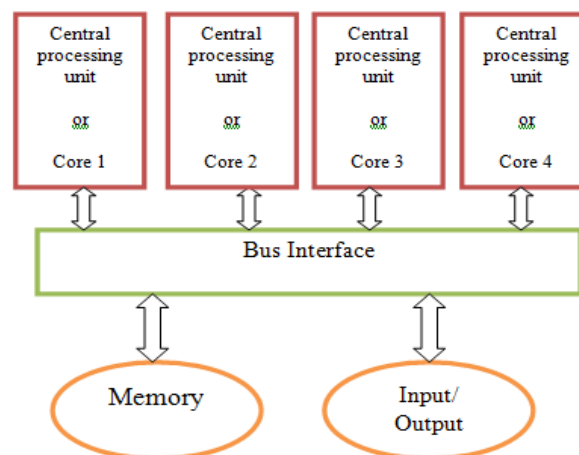

Figure 4: Quad core RISC architecture

More cores also lead to higher power consumption by the processor. When the processor is switched on, it supplies power to all the cores, not just one at a time. But a quad core processor will draw more power. So in this paper new method is used for quad core design and it reduces the power consumption in an effective way. The computer with a Quad Core has more computational power versus the Dual Core computer. If one will be using this personal computer for highly intensive tasks, the Quad Core processor can be beneficial in many ways. Multitasking with different applications and programs on a Quad Core will be more seamless due to its ability to distribute the workload to the multiple processors.

IV.   VERTEX 6 FPGA

The Virtex-6 family is a 40nm process technology for compute-intensive electronic systems. Virtex-6 FPGAs deliver higher performance clocking and advanced power management technology while lowering cost, risk and power consumption. The Virtex series of FPGAs are based on Configurable Logic Blocks (CLBs), where each CLB is equivalent to multiple ASIC gates. Each CLB is composed of multiple slices, which differ in construction between Virtex families. Virtex FPGAs include an I/O Block for controlling input/output pins on the Virtex chip, that support a variety of signalling standards. All pins default to input mode (high impedance). I/O pins are grouped into I/O Banks, where each Bank can support a different voltage.

V.   RESULT

In this paper the design of dual core and quad core processor is shown with power analysis. RISC architecture is used to design the core. The designed cores are implemented in one of the FPGA board called Vertex 6.

i.   Dual Core Processor: The figure 5 shows schematic diagram of dual core RISC processor which has two cores in single chip.

Figure 5: schematic diagram of dual core

The summary of power analysis of dual core RISC processor is shown in figure 6.

Figure 6: power analysis table for dual core

The device utilization summary with estimated values for dual core processor is shown in figure 7.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	128	93120	0%
Number of Slice LUTs	431	46560	0%
Number of fully used LUT-FF pairs	100	459	21%
Number of bonded IOBs	68	240	28%
Number of Block RAM/FIFO	1	156	0%
Number of BUFG/BUFGCTRLs	4	32	12%
Number of DSP48E1s	2	288	0%

Figure 7: Device utilization summary for dual core

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ii.   Quad Core Processor: The figure 8 shows schematic diagram of quad core RISC processor which has two cores in single chip.

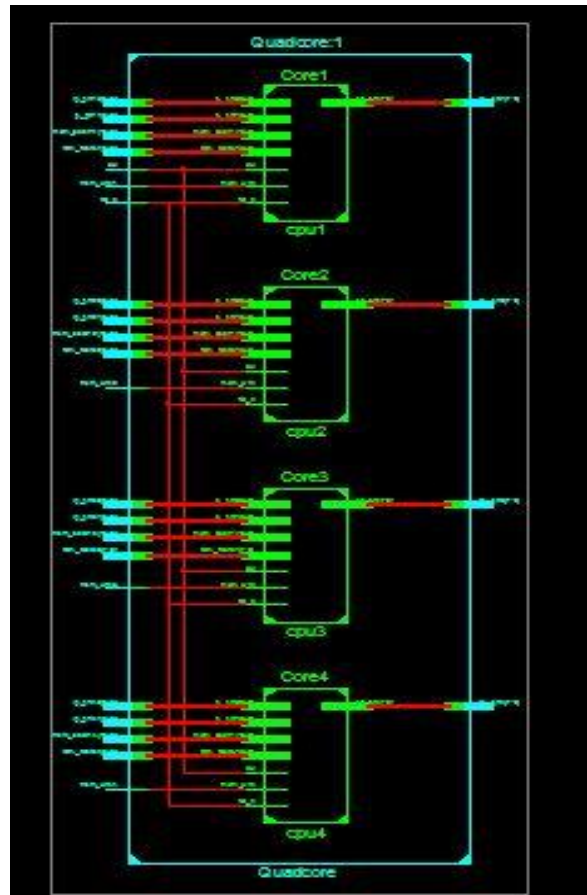Figure 8: schematic diagram of quad core

The summary of power analysis of quad core RISC processor is shown in figure 9.

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device			On-Chip	Power (W)	Used	Available	Utilization (%)		Supply Summary		Total	Dynamic	Quiescent
Family	Virtex6		Clocks	0.028	21	--	--		Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc6vlx75t		Logic	0.002	696	46560	1		Vccint	1.000	0.667	0.045	0.623
Package	ff484		Signals	0.004	1069	--	--		Vccaux	2.500	0.045	0.000	0.045
Grade	C-Grade		BRAMs	0.006	*	*	*		Vcco25	2.500	0.001	0.000	0.001
Process	Typical		DSPs	0.001	4	288	1		MGTAVcc	1.000	0.303	0.000	0.303
Speed Grade	-2		IOs	0.004	125	240	52		MGTAVtt	1.200	0.213	0.000	0.213
			Leakage	1.296									
Environment			Total	1.341							Total	Dynamic	Quiescent
Ambient Temp (C)	50.0								Supply Power (W)		1.341	0.045	1.296
Use custom TJA?	No												
Custom TJA (C/W)	NA				Effective TJA	Max Ambient	Junction Temp						
Airflow (LFM)	250		Thermal Properties		(C/W)	(C)	(C)						
Heat Sink	Medium Profile				2.9	81.0	54.0						
Custom TSA (C/W)	NA												
Board Selection	Medium (10"x10")												
# of Board Layers	8 to 11												
Custom TJB (C/W)	NA												
Board Temperature (C)	NA												

The Power Analysis is up to date.

Figure 9: power analysis table for quad core

The device utilization summary with estimated values for quad core processor is shown in figure10

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	242	93120	0%
Number of Slice LUTs	750	46560	1%
Number of fully used LUT-FF pairs	182	810	22%
Number of bonded IOBs	125	240	52%
Number of Block RAM/FIFO	2	156	1%
Number of BUFG/BUFGCTRLs	5	32	15%
Number of DSP48E1s	4	288	1%

Figure 10: Device utilization summary for quad core

The dual core and quad core designed using Verilog HDL is implemented in vertex 6 FPGA. The table 1 shows some of the important parameters values for both dual and quad core processors

	Dual core	Quad core
Device	xc6v1x75t-3-ff484	xc6v1x75t-3-ff484
Speed grade	-3	-3
Minimum period	3.713ns (Maximum Frequency: 269.347MHz)	3.713ns (Maximum Frequency: 269.347MHz)
Min i/p arrival time before clock	1.145ns	1.195ns
Max o/p required time after clock	0.572ns	0.572ns
Maximum combinational path delay	-	-
Clock period	3.713ns (Frequency: 269.347MHz)	3.713ns (Frequency: 269.347MHz)
Total number of path/destination port	1362/276	7516/544
Autotimespec constraints for clock net, clk BUFGP	Worst case slack: 0.092ns	Worst case slack: 0.090ns
	Best case achievable: 4.032ns	Best case achievable: 4.932ns
Number of register	132	264
Vccint	0.00276W	0.00478W
Vccaux	0.00001W	0.00001W
Vcco onchip thermal	0.00013W	0.00025W
Optimization goal	Speed	Speed
Total power for 100MHz clock frequency	1.323	1.348

Table 1: parameter values for dual core and quad core

VI. CONCLUSION

In this paper the design of dual core and quad core processor is shown with the help of RISC architecture. The designed cores are implemented in Vertex 6 FPGA. The Xilinx ise 14.4 is used with Verilog code. This is very helpful to reduce power consumption, cost with high efficiency and speed. In future this can be extended to more cores and also can be implemented in other FPGA technology. And more instructions can be added in RISC architecture.

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BIOGRAPHY

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