IJIREEICE
ISSN (Online) 2321-2004
ISSN (Print) 2321-5526
International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering
Vol. 6, Issue 11, November 2018

Power Quality Analysis of Single Phase Full Bridge Rectifier Fed DC Motor Drive

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Abstract: This paper provides a power quality analysis of single phase full bridge rectifier fed DC motor drive. A single phase full bridge rectifier is generally used in low voltage distribution system. It is necessary to analyse harmonic level and power factor. Here, DC motor is considered as the rectifier's load. The THD and power factor analysis is done for different loading conditions. The first analysis is based on variation of delay angle and its effect on THD and power factor. The second analysis is based on variation of torque or the changes in mechanical load done in the motor while maintaining the delay angle as constant. These analyses are useful in quantizing the THD and power factor at various conditions. FFT analysis on the input current provides the information about the various harmonics present in the waveform. The overall analysis is done using MATLAB software.

Keywords: Thyristor (SCR), DC motor, Total harmonic distortion (THD), Power factor (PF), MATLAB software

I. INTRODUCTION

In full bridge rectifier the power quality analysis is done as similar to the diode bridge rectifier (DBR), the DBR with capacitor is connected in parallel to improve the power quality and to maintain the harmonic level as per IEEE standard [1]. In some circumstances, the active and passive components are used to improve the power factor and the active as well as passive power factor correction is done for large capacitance at output side [2]. The harmonic level of any converter decides its efficiency, fast time domain method is used to eliminate voltage and current distortion [3].
Solution to overcome the deterioration of voltage and current waveform is to improve the harmonic level and to attain unity power factor. Harmonic stress on the bus as well as grid limited to a standard value, the origin of current and voltage harmonics are mainly due to power converters. The capacitor bank at each bus generates reactive power and achieves unity power factor at grid side as well as bus bar [4].
On considering the various loading effects, the power quality analysis can be carried out and the remedy to be taken to improve the conversion efficiency by reducing the distortion levels in current waveform [5]. The Fuzzy based technique implementation for determining the power quality parameters. Updated neuro-fuzzy techniques are used for diagnosing and analysing the power quality issues, thereby monitoring the required data of power quality issues can be done easily [5-6].
Based on various PWM techniques, the higher order harmonic can be eliminated to reduce the losses and to improve the efficiency, an Adaptive Feed-Forward Cancellation control technique which is a discrete time control, it improves the performance and robustness of system [8].
The voltage at each level of conversion is analysed and in case of line commutated converters, the voltage and current stress of a power semiconductor devices can be eliminated with a help of LCL filter [7]. In order to eliminate low power factor and current harmonic distortion in diode bridge rectifier, the passivity based control is implemented. The active rectifier with passivity control technique eliminates the non-linearity and dynamic loads at steady state performances can be improved [9]. The non-linearity and source of harmonic affects the system performances. The time domain model gives out the precise calculation results for the AC side harmonic current [10]. The paper deals with FPGA based controller to generate PWM signal for the conducting switches of rectifier to reduce input side current harmonics [12].
Need of perfect output at the DC stage during continuous conduction requires low THD and high input power factor at AC input side [27]. Luo topology of AC to DC conversion is used for power quality improvement with hysteresis controller to achieve high power factor along with supply current harmonic distortions of less than 5% [13]. THD analysis for various load conduction of AC to DC three level converter with a help of different controller tuners such as PI, Fuzzy tuned PI controller, the comparative results for each controller provides optimised result [11].
The presence of bulk capacitances and other filtering measures in diode bridge rectifier won't reduce lower order harmonics, and creates problem of low power factor at input AC side, thus, this can be eliminated by providing controllers such as proportional integral controller etc., Also the problem such as increased electromagnetic interference, losses due to distortion in line voltage can be appropriately minimized to a level [26].

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II. OPERATING PRINCIPLE

Fig 1 (a) shows the circuit diagram of a single phase full bridge rectifier fed dc motor drive. It is the most popular converter circuit and is widely used in the speed control of separately excited dc machines. Indeed, the R–L–E load shown in this figure may represent the electrical equivalent circuit of a separately excited dc motor. The single phase fully controlled bridge converter is obtained by replacing all the diode of the corresponding uncontrolled converter by thyristors which is a controlled one with a help of firing angle.

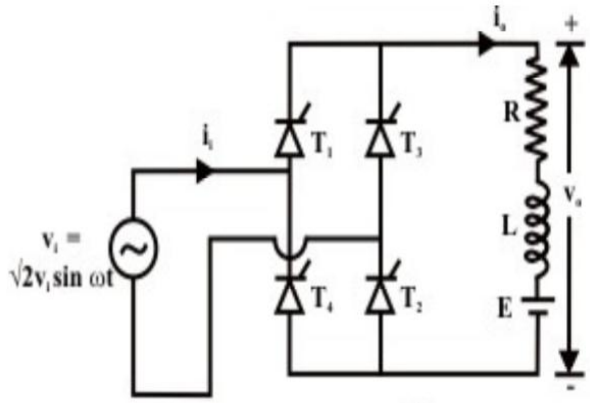

Fig. 1(a) Circuit Diagram

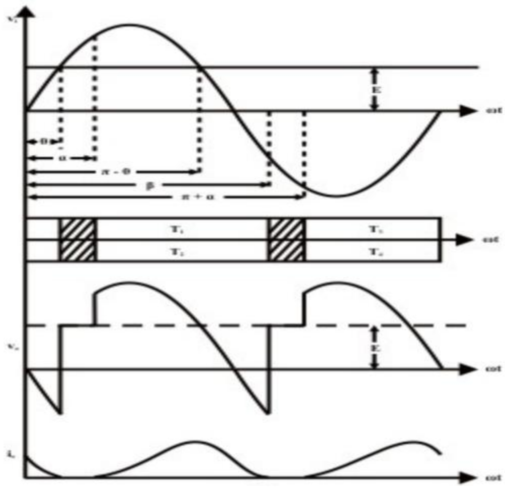

Fig. 2(b) Expected Waveform

III. MODES OF OPERATION

Thyristors T_1 and T_2 are fired together while T_3 and T_4 are fired 180º after T_1 and T_2 is fired. From the circuit diagram of Fig 10.3(a) it is clear that for any load current to flow at least one thyristor from the top group (T1, T_3) and one thyristor from the bottom group (T_2, T_4) must conduct. It can also be argued that neither T_1T_3 nor T_2T_4 can conduct simultaneously. That is, whenever T_3 and T_4 are in the forward blocking state and a gate pulse is applied to them, they turn ON and at the same time a negative voltage is applied across T_1 and T_2 commutating them immediately. Similar argument holds for T_1 and T_2. For the same reason T_1T_4 or T_2T_3 cannot conduct simultaneously. Therefore, the only possible conduction modes when the current i_0 can flow are T_1T_2 and T_3T_4. Hence, it is possible that at a given moment none of the thyristors conduct. This situation will typically occur when the load current becomes zero in between the firings of T_1T_2 and T_3T_4. Once the load current becomes zero all thyristors remain off. In this mode the load current remains zero. Consequently the converter is said to be operating in the discontinuous conduction mode. Fig 10.3(b) shows the voltage across different devices and the dc output voltage during each of these conduction modes. It is to be noted that whenever T_1 and T_2 conducts, the voltage across T_3 and T_4 becomes v_i. Therefore T_3 and T_4 can be fired only when v_i is negative i.e., over the negative half cycle of the input supply voltage. Similarly T_1 and T_2 can be fired only over the positive half cycle of the input supply. The voltage across the devices when none of the thyristors conduct depends on the off state impedance of each device. Under normal operating condition of the converter the load current may or may not remain zero over some interval of the input voltage cycle. If i_0 is always greater than zero then the converter is said to be operating in the continuous conduction mode. In this mode of operation of the converter T_1T_2 and T_3T_4 conducts for alternate half cycle of the input supply. However, in the discontinuous conduction mode none of the thyristors conduct over some portion of the input cycle. The load current remains zero during that period.

IV. CIRCUIT ANALYSIS

It is noted that the dc voltage waveform is periodic over half the input cycle. Therefore, it can be expressed in a Fourier series as follows,

$$I = \frac{a_0}{2} + \sum_{1}^{n} A_n \cos(n\omega t) + \sum_{1}^{n} B_n \sin(n\omega t),\ n = 1,2,3,4,5..... \quad (1)$$

RMS value of the nth harmonics $V_{0nRMS} = \frac{1}{\sqrt{2}}\sqrt{{V_{an}}^2 + {V_{bn}}^2}$ (2)

RMS value of v_0 can be given as,

$$V_{0RMS} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_0{}^2 d\omega t} = V_i \quad (3)$$

Fourier series expression of v_0 is important because it provides a simple method of estimating individual and total RMS harmonic current injected into the load as follows: The impedance offered by the load at nth harmonic frequency is given by,

$$Z_n = \sqrt{R^2 + (2n\omega L)^2} \quad (4)$$

$$I_{0nRMS} = \frac{V_{0nRMS}}{Z_n} \quad (5)$$

$$i_0 = Ie^{-\left(\frac{\omega t-\alpha}{\tan\varphi}\right)} + \frac{V_i\sqrt{2}}{Z}\left[\sin(\omega t-\varphi) - \frac{\sin\theta}{\cos\varphi}\right] \quad (6)$$

Where,

$$Z = \sqrt{R^2 + (\omega L)^2}, \quad \tan\varphi = \frac{\omega L}{R}, \quad E = \sqrt{2}\, V_i \sin\theta, \quad R = Z\cos\varphi$$

The input current displacement factor defined as the cosine of the angle between input voltage (vi) and the fundamental component of input current (ii1) waveforms is cosα (lagging). It can be shown that,

$$I_{ilRMS} = \frac{2\sqrt{2}}{\pi} I_0 \quad (7)$$

$$I_{iRMS} = I_0 \quad (8)$$

$$\text{Input current distortion facor} = \frac{I_{ilRMS}}{I_{iRMS}} = \frac{2\sqrt{2}}{\pi} \quad (9)$$

$$\text{Input power factor} = \frac{\text{Actual Power}}{\text{Apparent Power}} = \frac{V_i I_{ilRMS}\cos\alpha}{V_i I_{iRMS}} = \frac{2\sqrt{2}}{\pi}\cos\alpha \quad (10)$$

Therefore, the rectifier appears as a lagging power factor load to the input ac system. Larger the 'α' poorer is the power factor. The input current i_i also contain significant amount of harmonic current (3rd, 5th, etc) and therefore appears as a harmonic source to the utility. Exact composition of the harmonic currents can be obtained by Fourier series analysis of i_i and is left as an exercise.
Percentage THD,

$$\%THD = \frac{\sqrt{H_2^2 + H_3^2 + H_4^2 ... + H_n^2}}{\sqrt{H_1^2 + H_2^2 + H_3^2 + H_4^2 ... + H_n^2}} \times 100 \quad (11)$$

V. SIMULATION ANALYSIS

The simulation analysis of single phase controlled rectifier fed DC Motor Drive has been implemented in MATLAB/Simulink which is shows in figure 2 (a).

Figure 2(b) shows the source voltage, output voltage and output current. It can be seen that there is a step in output voltage because of the motor(R-L-E) load. At that time, the output current becomes zero. The current drawn by the motor load at the input side is contaminated by harmonics (mainly 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, etc).

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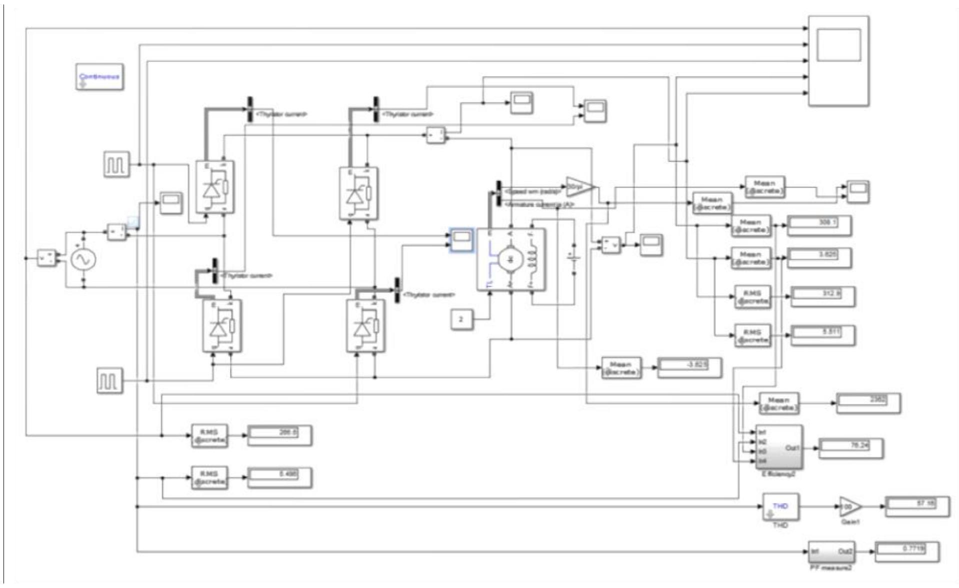


Fig. 2(a) Simulation of Single phase controlled rectifier fed DC Motor Drive

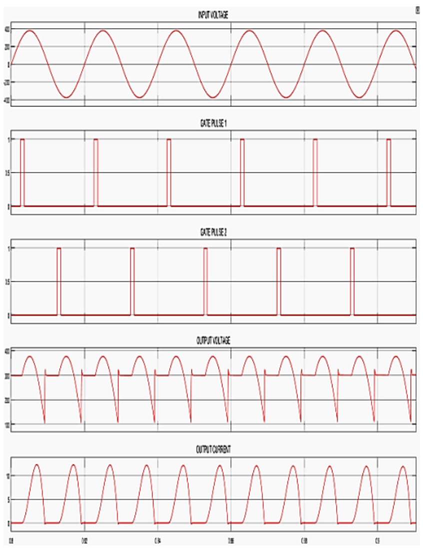


Fig. 2(b) Output voltage & current waveform

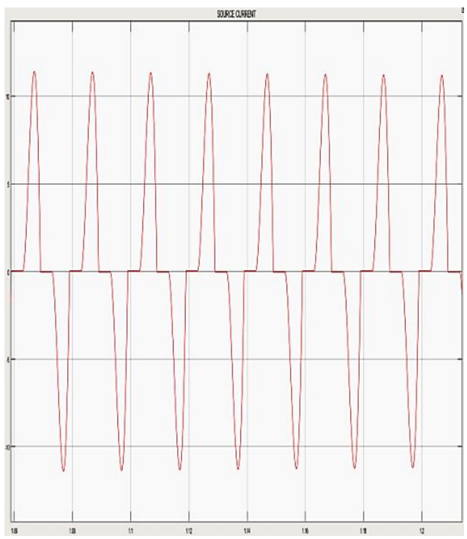
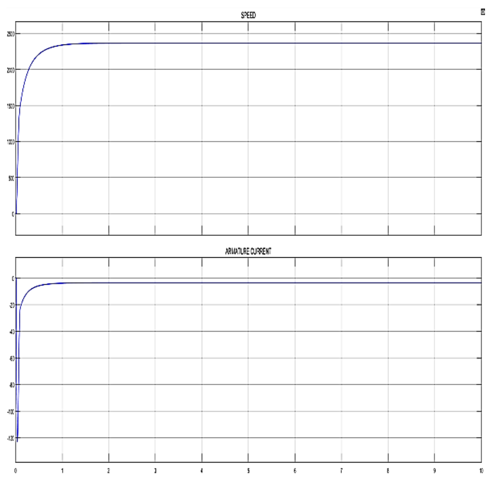


Fig.2(c) Source Current waveform



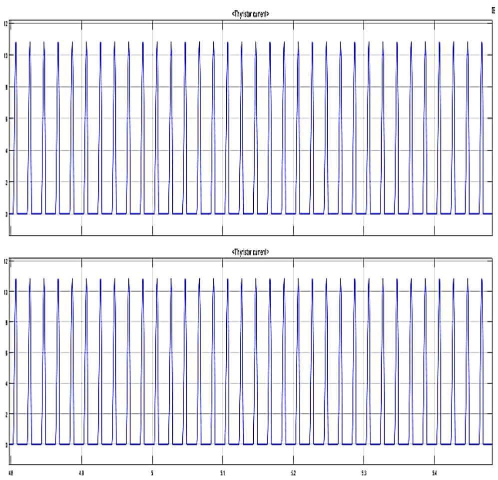


Fig. 3 (a) Speed and Armature Current waveform Fig. 3 (b) Current through Thyristors (T1,T3)&(T2,T4)

At the starting stage of the motor, the armature current dips down and motor draws a very large current. The motor speed slowly increases in this period. The current regains its constant value when the motor starts running at the rated speed for the given torque. The thyristor current is similar to source currents as shows in figure 3(b).

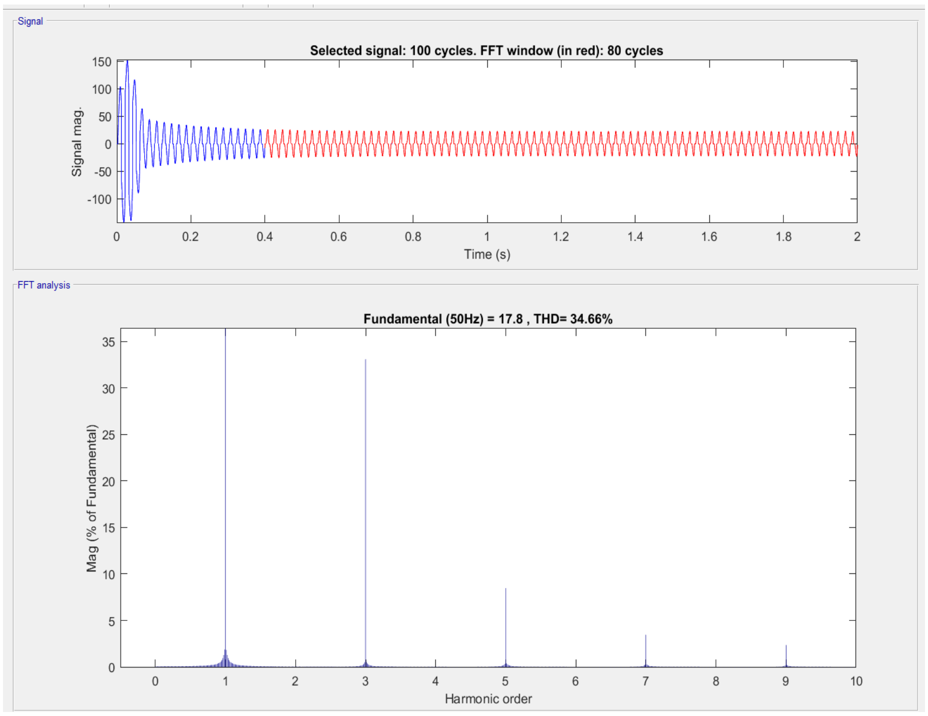


Fig. 4 FFT analysis of Source Current

The FFT analysis (fig. 4) reveals the information about the various harmonics present in the source current. The figure clearly shows the presence of third, fifth, seventh, ninth, (triplen harmonics).

Table I Duty Ratio Variation

S.NO	ALPHA(DEG)	P_{AC}(W)	P_{DC}(W)	EFFICIENCY(%)	THD(%)	PF	SPEED (RPM)
1	30	2460.45	1876.52	76.65	44.04	0.777	2168
2	45	2246.37	1717.64	76.47	46.34	0.777	2206
3	60	2263.4	1689.07	74.61	47.96	0.7592	2176
4	75	2298.09	1543.38	67.3	53.32	0.6875	2029
5	90	2300.75	1287.44	56.11	59.56	0.5774	1755

Table III Load Variation

S.NO	TORQUE(Nm)	I_{in}(A)	P_{AC}(W)	P_{DC}(W)	EFFICIENCY(%)	THD(%)	PF	SPEED (RPM)
1	2	5.51	1468.96	1118.04	76.24	57.16	0.7772	2382
2	4	7.47	1991.50	1523.74	76.51	49.42	0.7771	2254
3	6	9.37	2498.04	1903.30	76.31	43.62	0.7769	2161
4	8	11.22	2991.25	2267.92	75.81	38.97	0.7736	2078
5	10	13.04	3476.46	2610.27	75.11	35.11	0.7681	2001

CONCLUSION

The analysis of single phase rectifier fed DC motor drive shows for different duty cycle as well as different load, the efficiency and THD value varies. When the duty cycle is varied, the efficiency , THD and PF decreases as the α value is increased. When the load is varied, the efficiency and PF remains the same, but the THD decreases as the load is increased. This shows at full load the THD will be at its lowest.

IJIREEICE

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